Think fast.

Inphi Corporation® IN010C50-MD02 Porrima™ 400 Gbps 8:4 PAM-4 DSP

Datasheet

Applications

- Low power PAM-4 DSP IC with form factor suitable for QSFP-DD and OSFP 400G modules
- Supports four lanes of 106.25 Gbps Line side datastreams with PAM-4 modulation
- Supports the following data rates:
  - 8 x 25G NRZ to 4 x 50G PAM4
  - 8 x 50G PAM4 to 4 x 100G PAM4
  - 4 x 25G PAM4 to 2 x 50G PAM4
  - 4 x 50G PAM4 to 4 x 50G PAM4

Product Features (Sheet 1 of 2)

- Host Receivers
  - Octal OIF-56G-VSR, PAM-4 and NRZ capable receiver with adaptive CTLE/AGC able to equalize 9dB loss channels + up to 4dB total package loss
  - Digital feedback equalizer (DFE) for trace reflection cancellation
  - Independent CDR in each lane with full-rate LC VCO
  - Independent PLL per lane pairs
  - Independent power down control for each lane
  - SNR monitor
  - Loss of Lock (LOL) indication
  - PAM-4 inverse gray coding, Polarity inversion, PAM-4 decoding, PAM-4 MSB/LSB swap
  - Implements the following diagnostic features:
    - PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q checkers
    - PRBS auto-polarity detection
    - Continuous identical symbol detection
    - Clock monitor – any two internal clocks can be counted simultaneously
- Host Transmitters
  - Octal PAM-4 and NRZ capable transmitters
  - Output swing ~800mVpp differential
  - DSP and DAC based architecture. DSP implements Linear FIR and LUT for driving the Tx DAC.
  - Independent control of PAM-4 inner eye levels
  - Host retimer capability (shallow host loopback)
  - PAM-4 gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swap
  - Tx squelch control
  - Test pattern generator per lane:
    - Supports PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q
    - Square wave, JP03A, JP03B, transmitter linearity test patterns
    - SSPRQ support
    - CID jitter tolerance pattern
    - Error injection
  - Continuous identical symbol detector

Product Features (Sheet 2 of 2)

- Line Receivers
  - Line receiver inputs have integrated on-chip DC block capacitors
  - Independent PLL per lane pairs
  - Four ADC/DSP-based Line side receivers each operating at 106.25Gbps (53.125GBd) data rate
  - Equalizer is a combination of digital FFE, DFE (optional), Reflection canceller (optional) and MLSD (optional)
  - Supports optional SNR monitor and slicer histogram generation
  - Supports slicer threshold adjust for each PAM4 level
  - PRBS Checker per lane either on the entire data width, or per even/odd bits
  - PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q checkers
  - PRBS auto-polarity detection
  - Loss of Signal (LOS) indication
- Line Transmitters
  - Independent PLL per lane pairs
  - Quad-λ 106.25Gbps (53.125GBd) Transmit data streams with PAM-4 modulation or Quad 26.5625Gbps Transmit data streams with either PAM-4 or NRZ modulation
  - Up to 800mV differential output swing
  - Fine PAM-4 inner eye amplitude programmability
  - High-speed clock monitor supporting up to 7GHz differential clock rate
  - PAM-4 gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swap
  - Squelch Control
  - Test pattern generator per lane:
    - Supports PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q
    - Square wave, JP03A, JP03B, transmitter linearity test patterns
    - SSPRQ support
    - CID jitter tolerance pattern
    - Error injection
  - Continuous identical symbol detector
- Other Features:
  - IEEE P802.3 Clause 45 MDIO interface
    - Ball-programmable MDIO PHY address
    - Supports MMD08 discovery registers (device identifier, ability registers, etc)
    - Implements frame structure extension and timing characteristics per Clause 45
    - Implements Clause 83.6 PMA MDIO function mapping
    - Supports MDIO rates up to 25 MHz
  - Supports I^2C interface
    - Standard-mode with a bit rate up to 100 kbps
    - Fast-mode with a bit rate up to 400 kbps
    - Fast-plus mode with a bit rate up to 1.0 Mbps
  - Incorporates on-chip micro-controller that enables real-time adjustments to host-side and line-side receiver parameters to optimize the available link budget
  - ESD:
    - ESD-HBM 1kV on HS pins and 2kV on LS pins
    - ESD-CDM 250V on all pins
  - Firmware code can be loaded in from an external EEPROM/Flash device connected directly to the transceiver through the SPI interface to configure the DSP parameters to the optimum settings
  - Available in 10.0mm x 13.0mm package with 0.5 mm ball pitch

Inphi Corporation Proprietary and Confidential—Under NDA

Revision History

Revision B Revision Date: 01 August 2019
Production release.

Revision A Revision Date: 06 November 2018
First preliminary release of this document from Inphi Corporation.

Contents

List of Figures

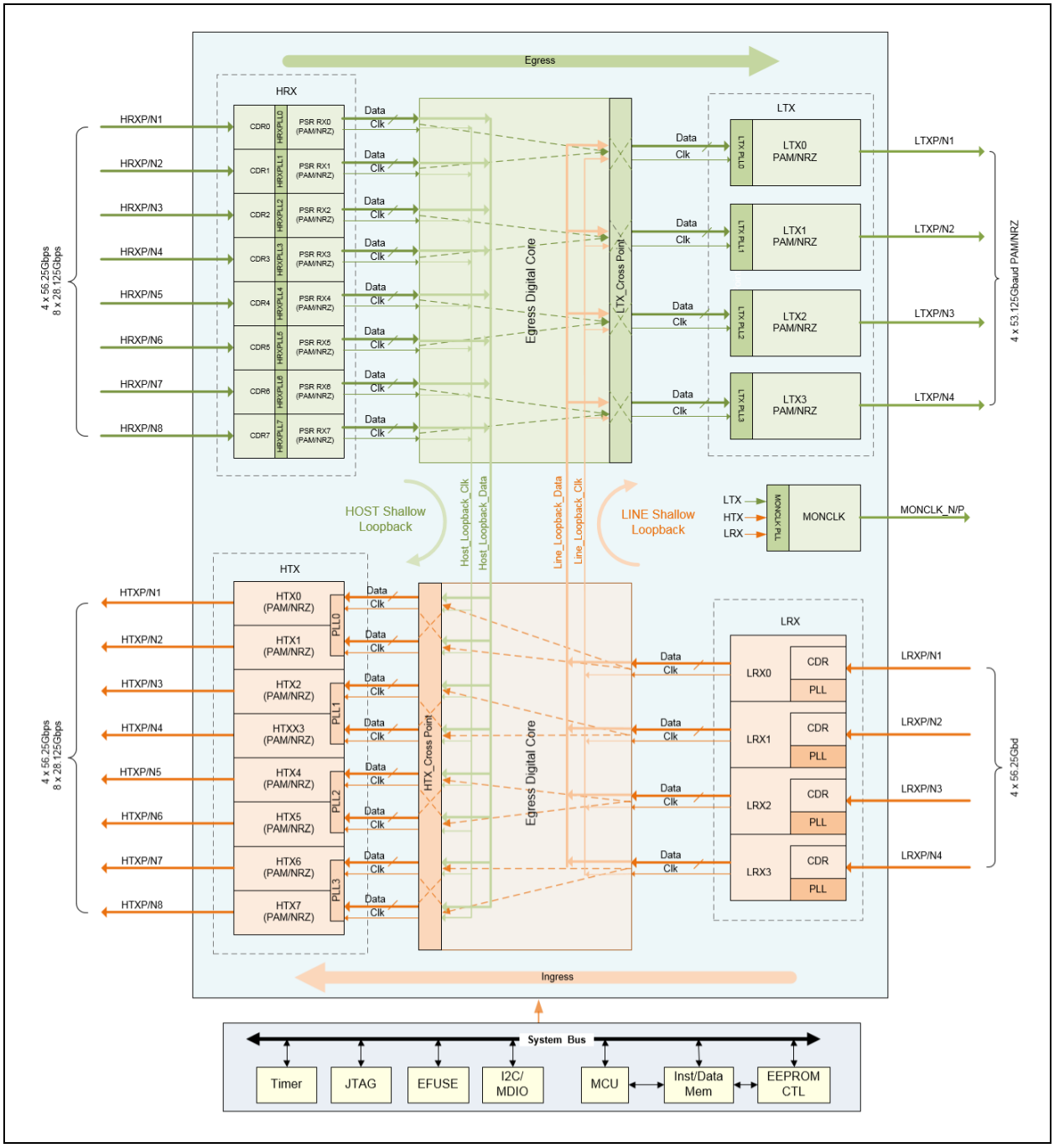
List of Tables

1.0 Introduction

The Porrima 400G DSP is a 8:4 PAM-4 DSP for PAM-4 signals interfacing between optics and a host device. The Porrima 400G DSP supports a high-performance DSP including DFE/FFE, MLSD, breakout mode support, and reflection canceller. The IEEE 802.3 CDAUI Host I/O supports OIF CEI-56G-VSR, CDAUI-8 and CAUI-4. In addition, The Porrima 400G DSP provides the following test and diagnostic features: FFE tap scan, SNR monitor and histograms, Host/Line shallow loopbacks, as well as various pattern generators and checkers. The architecture of the Porrima 400G DSP is shown in Figure 1.

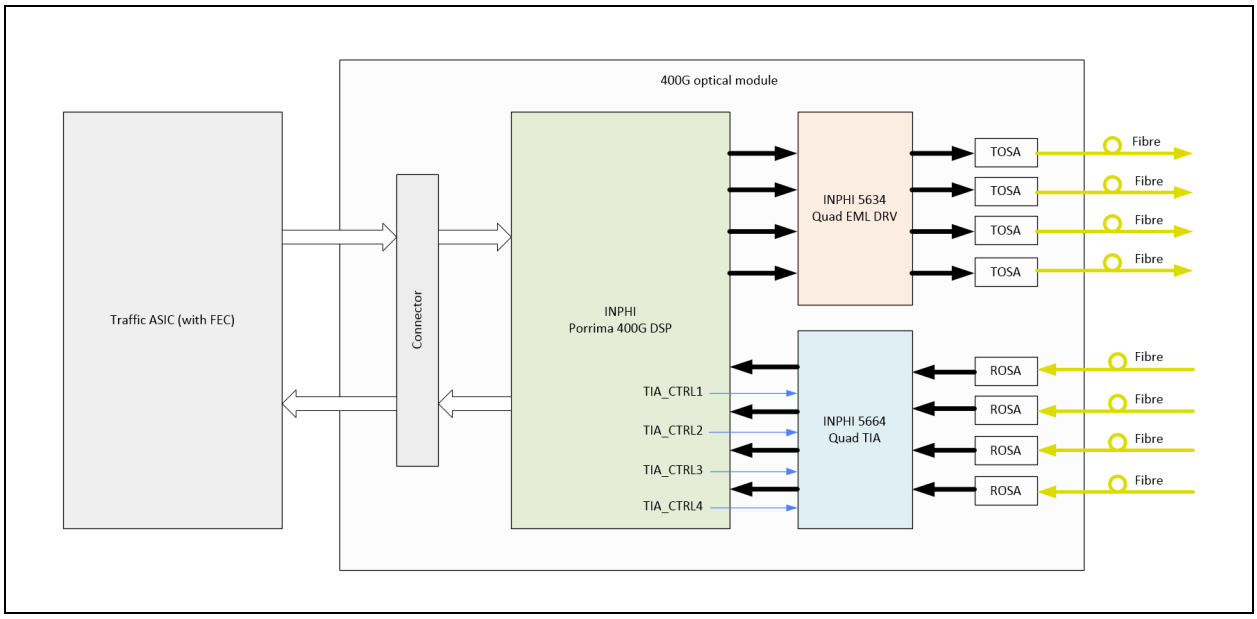
1.1 Block Diagram

Figure 1 Block Diagram



1.2 Typical Application

Figure 2 Typical Application



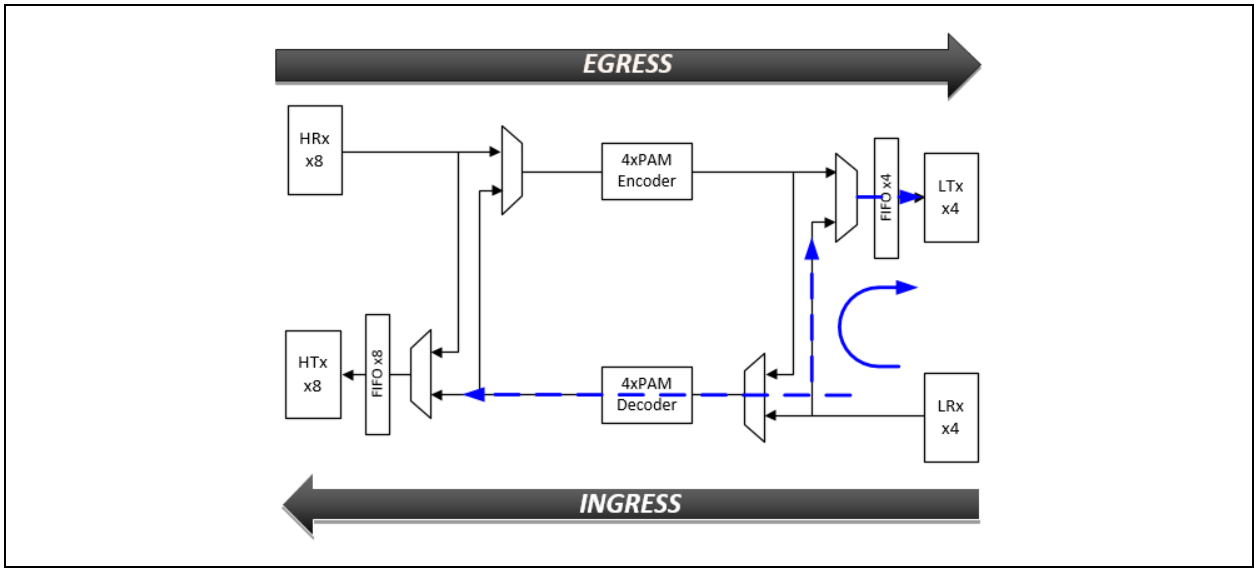
1.3 Diagnostic Modes

The Porrima 400G DSP supports shallow loopback on both Host and Line interfaces to aid in system diagnostics.

1.3.1 Line Retimer Mode (Shallow Line Loopback)

Figure 3 illustrates the datapath when configured as line retimer. The PAM-4 data received on the Line side Line receivers is looped back in the digital to the Line transmitters. Optionally, the receive data can also be forwarded to the host transmitters to be transmitted as it would be in mission mode.

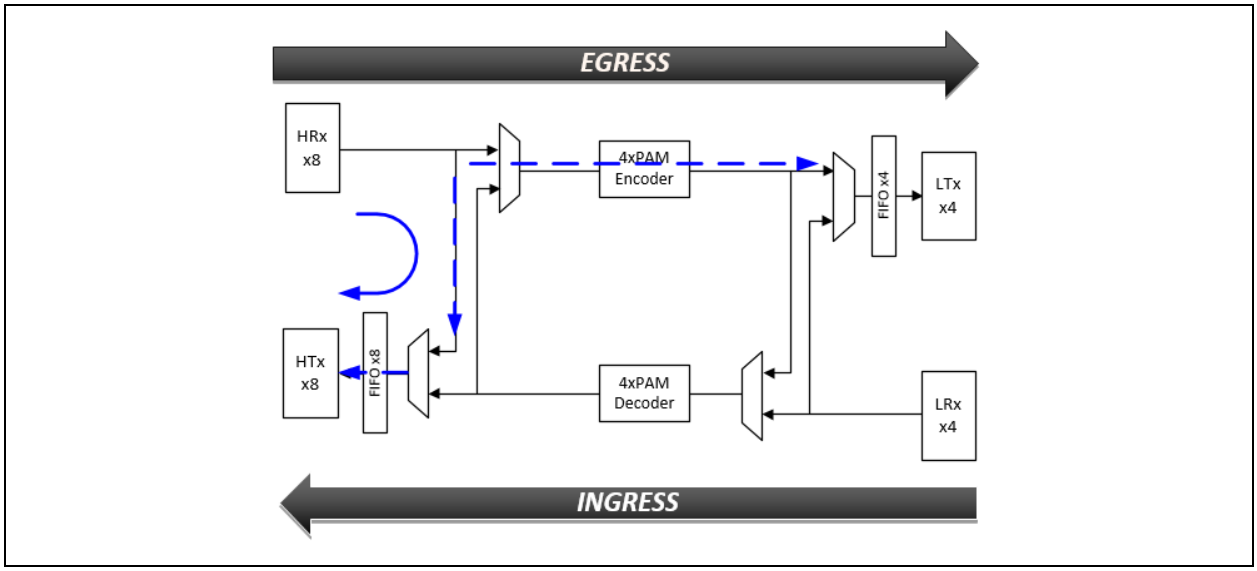
Figure 3 Line Retimer Mode (Shallow Line Loopback)



1.3.2 Host Retimer Mode (Shallow Host Loopback)

Figure 4 illustrates the datapath when configured as Host retimer. The PAM-4 data is received on the Host side; Host receivers are looped back digitally to the Host transmitters. Optionally, the receive data can also be forwarded to the Line side transmitters as in mission mode to be transmitted as PAM-4.

Figure 4 Host Retimer Mode (Shallow Host Loopback)



1.3.3 Clocking

The Porrima 400G DSP requires an external crystal oscillator to provide clock reference for internal PLLs and provides clock source for diagnostic functions. For REFCLK specifications, see Table 21, *REFCLK Specifications*, on page 41 for details.

1.4 Supported Data Rates

The device supports the following standard data rates: Quad-λ 106.25 Gbps (53.125 GBd) Transmit data streams with PAM-4 modulation or Quad 26.5625 Gbps Transmit data streams with NRZ modulation.

1.5 Latency

Table 1 Latency

	Notes	Latency (ns)
Measured	DR4 FEC Bypass - roundtrip total	75

2.0 Management Interface

The Porrima 400G DSP can be configured/monitored via either a MDIO or I^2C interface. The device supports IEEE802.3 Clause 45 MMD30 space and a small subset of the MMD08 space. The remaining MMD08 registers are accessible via API.

2.1 Broadcast Support

2.1.1 Register Broadcast

To increase configuration speed and efficiency the register broadcast feature allows simultaneous access to multiple lanes. There is an additional, virtual, lane that acts as the broadcast lane; all writes to this lane write the same data to all lanes. Reads from this broadcast lane return data from physical lane 1.

A broadcast mask defines the lanes that are part of the broadcast operation.

2.1.2 Device Broadcast

As many applications use multiple phy devices, Porrima includes a broadcast feature that enables writes to multiple devices in parallel. This is accomplished by temporarily assigning the same slave address to the devices that are part of the broadcast operation so that all writes to that slave address will be accepted by all participating devices. Reads are not supported in broadcast mode.

Important note: Using device broadcast for operations that change the power consumption of the device can cause a significant change in the total system power supply demand as all devices participating in the broadcast change their power demand at the same time. The system design must accommodate this quantum change in power demand.

2.2 MDIO

MDIO interface timing, frame structure and electrical characteristics comply with IEEE802.3, Clauses 22 and 45.

2.2.1 MDIO Frame Formats

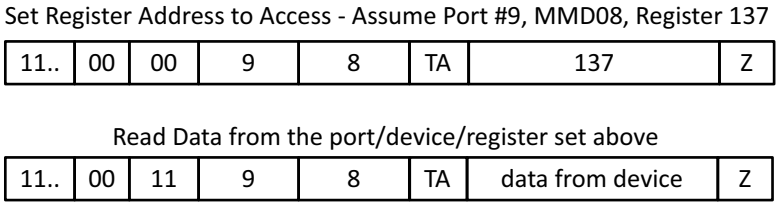
Figure 5 illustrates the MDIO frame format and defines the terminology. Figure 6 shows examples of the different frame types (as distinguished by the 2-bit OP code).

Figure 5 Basic MDIO Frame Structure

Table 2 MDIO Field Definitions

Field	Definition
PRE	Preamble, 32-bits of consecutive 1's
ST	Start of frame, 2-bits of 0
OP	Operation Code, 2-bits: • 00 - Address frame: D/A field contains the target address inside the device • 01 - Post-Read Increment Data Frame: D/A field contains data read back from the device. The address is auto-incremented after the read. • 10 - Write Data Frame: D/A field contains the data to be written to the device • 11 - Read Data Frame: D/A field contains data read back from the device.
PRTAD	Port Address, 5-bits. MDIO supports up to 32 devices on a single bus; this is the bus address of the target device. For devices with fewer than 5 Port Address bits, the unused, upper address bit should be set to 0.
DEVAD	Device Address. MDIO supports the concept of multiple Devices inside a single Port (PRTAD). Usually referred to as MMDxx, this is the address of the target Device. MMD08 and MMD30 are the most common Device addresses
TA	Turn Around field. Provides a buffer of two bit-times to reverse the bus (MDIO) direction during a Read operation.
D/A	Data/Address field. 16-bits long, this is the field that contains the address of the target register in the device during the address frame. In read operations it contains the date read from the device. In write operations it contains the data to be written to the device.
Z	Bus tri-stated (High-Z). Partners in the MDIO transaction release the MDIO (data) signal.

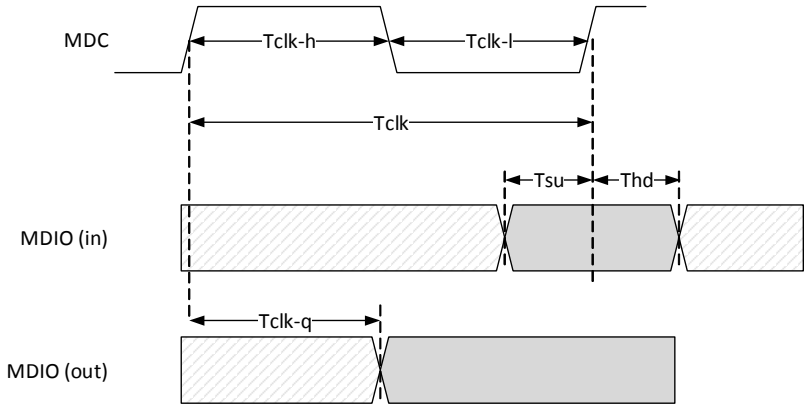
Figure 6 MDIO Frame Examples



2.2.2 MDIO Timing

The maximum operating frequency of the MDIO interface is limited to 25MHz with the constraint that the Porrima 400G DSP internal clock frequency is greater than 40MHz. If the internal reference clock is less than 40MHz, the maximum MDIO operating frequency is reduced.

Figure 7 MDIO Timing



Parameter	Symbol	Min	Max	Units
MDC Clock Period	Tclk	0	40	ns
MDC Clock High Time	Tclk-h	16	-	ns
MDC Clock Low Time	Tclk-l	16	-	ns
MDIO In Setup to MDC Rise	Tsu	10	-	ns
MDIO In Hold to MDC Rise	Thd	10	-	ns
MDC Rise to Data Out[1]	Tclk-q	0	Note 1	ns

Notes:
1. The actual clock to data out valid is dependent upon the capacitance and pull-up on the MDIO line and the speed of operation.

2.3 I2C

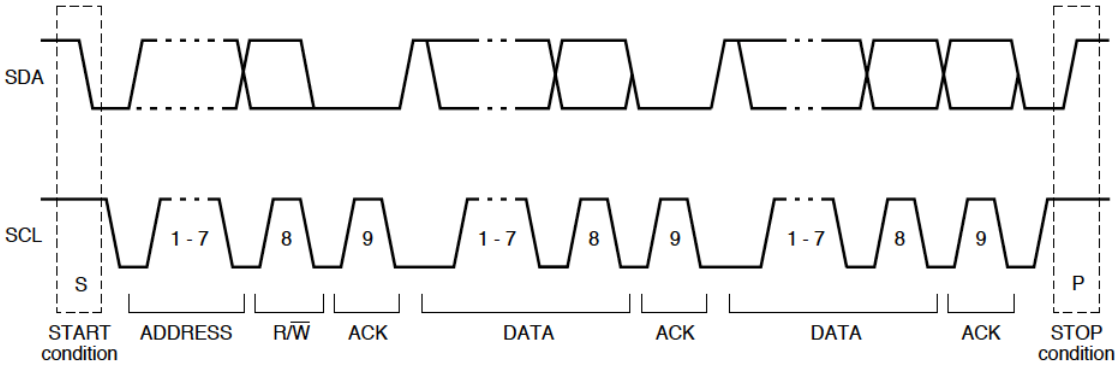
The Porrima 400G DSP supports Standard-mode, Fast-mode and Fast-mode Plus I2C timing modes. The main distinction between the modes is the data rate. In Standard mode, the maximum data rate is 100 kbps; in Fast mode, the maximum data rate is 400 kbps while in Fast Mode Plus the maximum data rate is 1 Mbps.

I2C operation is selected by connecting I2CSEL I/O through a 4.7kΩ resistor to VDDMDIO_1P2.

2.3.1 I2C Transactions

I2C transactions follow the format shown in Figure 8. Data transfers are signaled with a START condition and terminated with a STOP condition.

Figure 8 General 1²C Transaction



The first 8 bits transmitted following a START condition compromises of the ADDRESS field and the R/W bit. Figure 9 below, illustrates how these bits are interpreted by the Porrima 400G DSP.

I²C Frame Formats

Figure 10 below depicts the various I²C data formats supported by the Porrima 400G DSP.

Figure 9 I²C Address Encoding

Table 3 I²C Field Definitions

Field	Definition
PRTAD	Port Address, 5-bits. MDIO supports up to 32 devices on a single bus; this is the bus address of the target device. For devices with fewer than 5 Port Address bits, the unused, upper address bit should be set to 0.
DEVAD	Device Address. MDIO supports the concept of multiple Devices inside a single Port (PRTAD). Referred to as MMDxx, this is the address of the target Device inside the selected Port. MDIO-over-I2C supports two Devices: MMD08 and MMD30. 0 = MMD08 1 = MMD30
R/W A/D	Address/Data and Read/Write controls, 2-bits R/W : A/D • 00 - Address frame: D/A field contains the target address inside the device • 01 - Write Data Frame: D/A field contains the data to be written to the device • 10 - Post-Read Increment Data Frame: D/A field contains data read back from the device. The address is auto-incremented after the read. • 11 - Read Data Frame: D/A field contains data read back from the device.
D/A	Data/Address field. 16-bits long, this is the field that contains the address of the target register in the device during the address frame. In read operations it contains the date read from the device. In write operations it contains the data to be written to the device.

Figure 10 I2C Transaction Examples

Set Register Address to Access - Assume Port #9, MMD08, Register 137

9	0	0	0	137

Read Data from the port/device/register set above

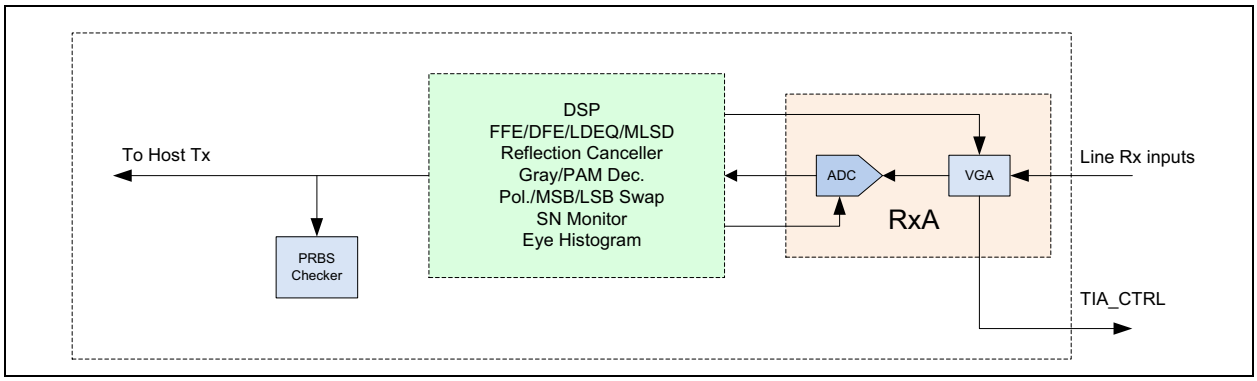
9	0	1	1	D/A

3.0 Module Descriptions

3.1 Line Receive Interface

Figure 11 shows a high level block diagram of the Line side (optical) receiver module on Porrima 400G DSP. The module consists of a quad lane receiver with a common reference PLL.

Figure 11 Line Receive Block Diagram



3.1.1 Line RxA

The Rx analog front-end consists of programmable VGA and the ADC that samples the input signal.

- The VGA is a wide bandwidth gain block with a ±2dB total range. It is controlled by the line receiver DSP.
- TIA_CTRL is an output control signal for use with Inphi TIA only.
- The ADC digitizes the preconditioned Rx analog signal into the digital, DSP section of the receiver.

3.1.2 Line RxD

The Line RxD macro is the high speed Digital Signal Processing (DSP) section of the datapath. It supports the following features:

FFE

The FFE with gain and DC offset compensation, provides the necessary equalization. Using LMS algorithm, it is fully adaptive.

PAM4 DFE

Optional PAM4 DFE with nonlinear adaptive feedback in the datapath.

PAM4 1+D Decoder

In the DFE mode, in order to overcome DFE Error propagation, 1/(1+D) pre-coder is employed on the Tx Driver and on the Rx end, the final DFE decisions are passed through (1+D) filter to cancel the effect of pre-coder.

PAM4 Reflection Canceller

Optional PAM4 Reflection Canceller to reduce group-delay effects

PAM4 Level Dependent Equalizer

Optional level dependent equalizer used to equalize the two inner levels of the PAM-4 eye.

PAM4 Slicer

The PAM4 Slicer block compares the FFE output data with the thresholds {Tn, Tm, Tp}, and produces the PAM4 decisions. The thresholds {Tn, Tm, Tp} are also adaptive to compensate for the level-dependent noise nature of optical channels, e.g. due to RIN.

SNR Monitor

This block estimates the mean square error of the of the recovered, DSP-processed PAM signal.

PAM Histogram

The histogram block collects the number of 'hits' at each of 160 amplitude levels in the recovered, DSP-processed PAM signal. Once the count at any particular level reaches 2^20 'hits' the block halts data collection and retains the collected data until the block is reset. The user can access the Histogram data through an API call.

MLSD

Maximum Likelihood Sequence Detection (MLSD) is used for achieving higher detection SNR in LRX.

3.1.3 Diagnostic Features

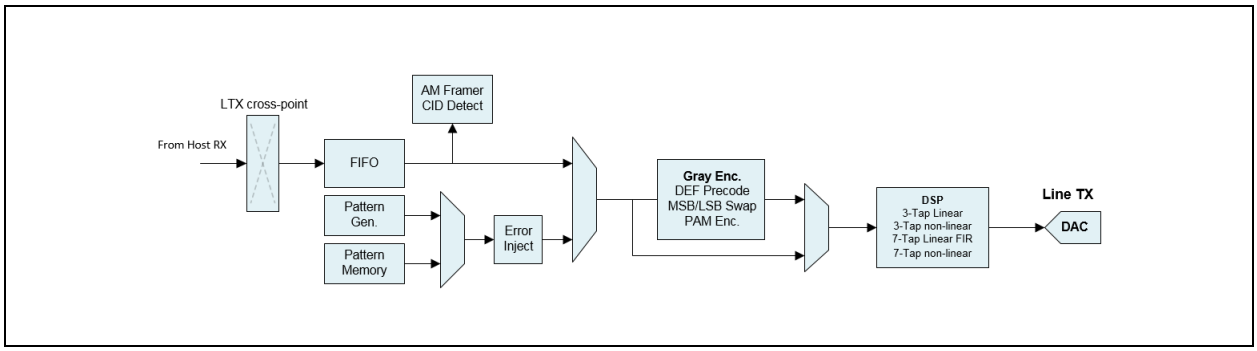
The Line receiver supports the following diagnostic features:

- PRBS Checker per lane either on the entire data width, or per even/odd bits
  - Supports PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q
  - Auto lock mode which scans through all PRBS patterns
  - PRBS stay in lock mode
  - Programmable threshold and duration for lock declaration
  - Counters support snapshot or individual read mode
- LOS indication for every lane
- SNR (Signal to noise Ratio) at the slicer is available for every lane through an API call
- Eye Histogram available for every lane, one at a time, through an API call.
- Rx FFE tap coefficients can be accessed via API

3.2 Line Transmit Interface

Figure 12 shows a high level block diagram of the Line side transmitter module on the Porrima 400G DSP. There are four identical transmit interfaces supporting 4-lanes of NRZ or PAM4 signaling. The datapath receives up to four lanes of PAM-4 data from the core and prepares them for optical transmission. A summary of the Egress transmit datapath is described below.

Figure 12 Line Transmit Block Diagram

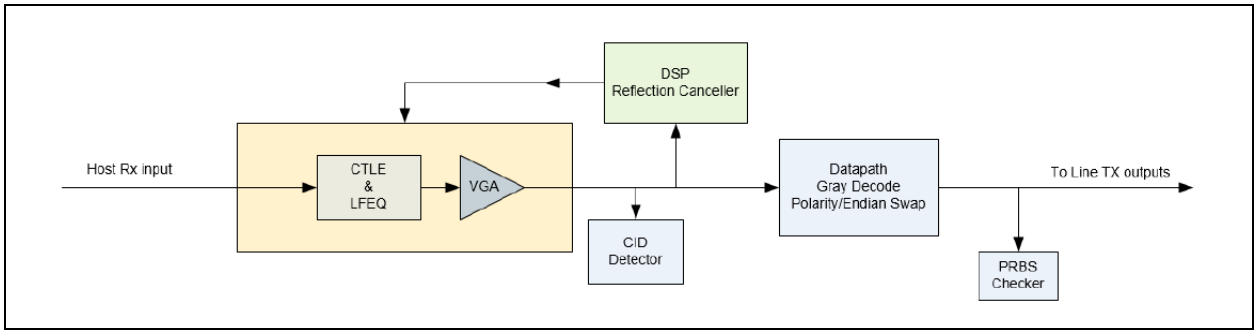


- Quad-Lambda Transmit data streams with PAM-4 or NRZ modulation
- Four independent transmit PLLs for each lane of transmit lanes
- Receive to transmit shallow loopback (PAM-4 to PAM-4)
- PAM-4 gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swap
- Squelch Control
- Synchronous cross-point allowing any of the receive data streams to be transmitted on any of the lanes
- 3-Tap and 7-Tap non-linear FIR allows for independent pre/main/post tap adjust combined with asymmetric eye adjust for inner PAM4 eye levels. The 3-tap option provides lower power than the 7-tap option.
- Test pattern generator per lane:
  - Supports PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q
  - PRBS can be generated independently on PAM-4 MSBs and LSBs
  - SSPRQ Support
  - 2 x 64 bit programmable-repeatable fixed pattern
  - Square wave, JP03A, JP03B, transmitter linearity test patterns
  - CID jitter tolerance pattern
- Test pattern memory:
  - LTX lanes 1 through 4 have *independent* test pattern memories that can generate repeating patterns up to, and including:131,072 bits in binary mode or 16,384 UI in linear mode.
- Error injection
- Continuous identical symbol detector (CID)

3.3 Host Receive Interface (Host RX)

Figure 13 shows a high level block diagram of the host side receiver module on the Porrima 400G DSP. The module consists of an eight-lane receiver supporting PAM-4 or NRZ datastreams. A summary of the Egress receive datapath is described below.

Figure 13 Host Receive Block Diagram

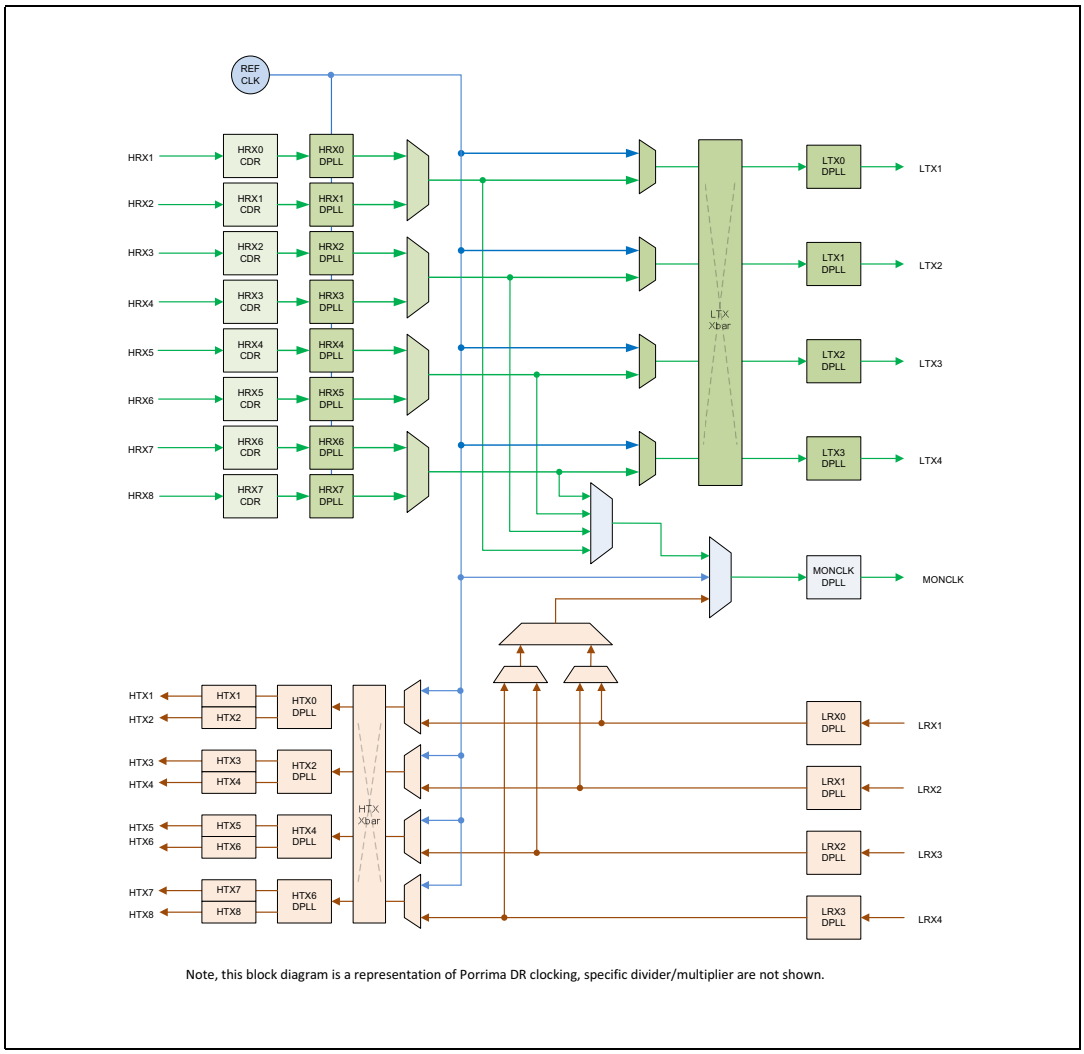


3.3.1 Host RXA

The Host RXA macro is the high speed Analog Front End (AFE) section of the datapath. Eight macros are instantiated each handling up to 53.125 Gbps of PAM-4 data. Each receiver supports the following features:

- Attenuator, a front end analog attenuator provides 3 levels of settings: 0dB, 3dB and 6 dB respectively.
- Adaptive CTLE able to equalize 9dB loss channels + up to 4dB total package loss. CTLE has a 10dB range and is automatically controlled by the Host DSP.
- LFEQ provides programmable low frequency gain. The range is 0-3dB and is controlled by the Host DSP.
- AGC: Adaptive with 9dB range, controlled by Host DSP
- Independent CDR in each lane with full-rate LC VCO
- Independent power down control for each lane
- Independent PLL in each lane for break-out mode support. A representative clocking diagram is illustrated in Figure 14.

Figure 14 Clocking Block Diagram



3.3.2 Receive Datapath

The RX datapath supports the following features:

- PAM-4 inverse gray coding
- Polarity inversion
- PAM-4 decoding
- PAM-4 MSB/LSB swap

3.3.3 Receive DSP

The Host DSP contains the following features:

- Reflection canceller control
- Calibration and adaptation for: CTLE, AGC gain, sampler offsets, thresholds

- SNR monitor
- Loss of Lock (LOL)

3.3.4 Diagnostic Features

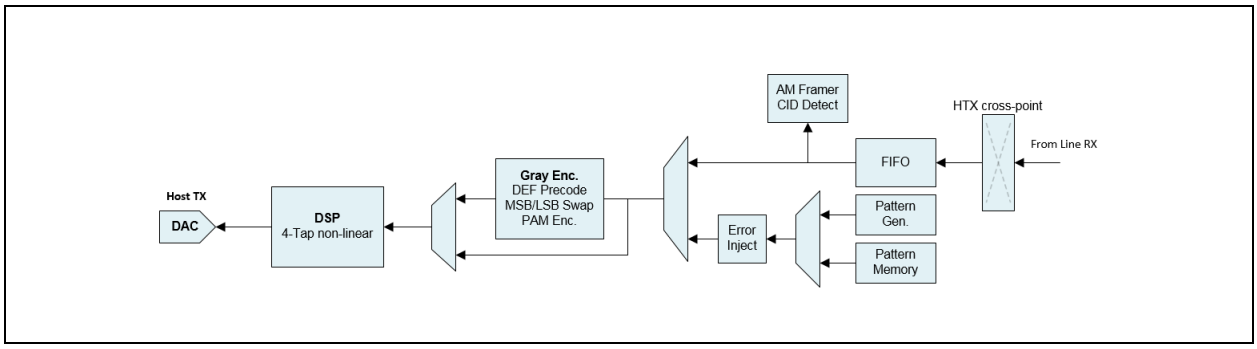
The Host receive interface implements the following diagnostic feature:

- PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q checkers
- PRBS can be checked independently on PAM-4 MSB or LSB or over full word
- PRBS auto-polarity detection
- Fixed pattern of any 64-bit pattern repeated continuously
- Continuous identical symbol detection
- Clock monitor – any two internal clocks can be counted simultaneously

3.4 Host Transmit Interface

Figure 15 shows a high level block diagram of the host side transmitter module on the Porrima 400G DSP. The module consists of a quad lane transmitter supporting PAM-4 or NRZ datastreams. Four PLLs service the eight transmit lanes allowing for four independent output frequencies. A summary of the Ingress transmit datapath is described below.

Figure 15 Host Transmit Block Diagram



- Eight transmit data streams with either PAM-4 or NRZ modulation
- Receive to transmit shallow loopback (PAM-4 to PAM-4)
- PAM-4 gray coding, polarity inversion, PAM-4 encoding, PAM-4 MSB/LSB swap
- Squelch Control
- Synchronous cross-point allowing any of the receive data streams to be transmitted on any of the lanes
- 4-Tap non-linear FIR allows for independent pre/main/post tap adjust combined with asymmetric eye adjust for inner PAM-4 eye levels.
- Test pattern generator per lane:
  - Supports PRBS7/9/11/13/15/16/23/31/58, their inverse and PRBS13Q
  - PRBS can be generated independently on PAM-4 MSBs and LSBs
  - 2 x 64 bit programmable-repeatable fixed pattern

  - Square wave, JP03A, JP03B, transmitter linearity test patterns
  - CID jitter tolerance pattern
- Test pattern memory:
  - Binary mode: up to 32,768 bits for four transmitter lanes, each transmitter can have a unique pattern with identical lengths
  - Linear mode: up to 16,384 UI (each 8-bits) on one transmitter lane. In this mode the 8-bit value is sent directly to the output DAC.
- Error injection
- Continuous identical symbol detector (CID)

3.5 General Purpose Input Output (GPIO) Interface

The General Purpose Input Output (GPIO) Interface provides a flexible method of collecting status from outside the device, or conveying status points from within the device to the outside world without using the register interface.

The Porrima 400G DSP supports up to 7 GPIOs, 2, GPIO_3P3, LOL0_N, LOL1_N, LOL2_N, LOL3_N and INTR_N. There is no functional difference between the pins other than their name and default configuration. For the rest of this section whenever GPIO is mentioned it implicitly includes the LOL and INTR_N pins as well unless specifically stated otherwise.

Depending upon the package option, either all or only a subset of GPIOs may be present.

Note: GPIO3 is a special pin in the Porrima 400G DSP and cannot be used as a regular GPIO. It is a dedicated debug mode select pin.

3.5.1 GPIO Default State

By default, after device reset, the GPIOs are configured as follows:

- GPIO_0 to GPIO_6, GPIO_0_3P3, GPIO_1_3P3 are by default configured as inputs
- LOL0_N, LOL1_N, LOL2_N, LOL3_N and INTR_N are by default configured as outputs
- All GPIOs have an internal (weak) pull-down resistor

Any or all of these default states can be reconfigured after reset through the MDIO/I^2C interface.

3.5.2 GPIO Input Interrupt

A maskable interrupt register latches any change (either on a low-to-high or high-to-low transition) on any of the GPIO inputs. The interrupt can be enabled onto either the device top level interrupt (MMD30_INTH) or the core interrupt of the MCU Interrupt input.

3.5.3 GPIO Toggle Output

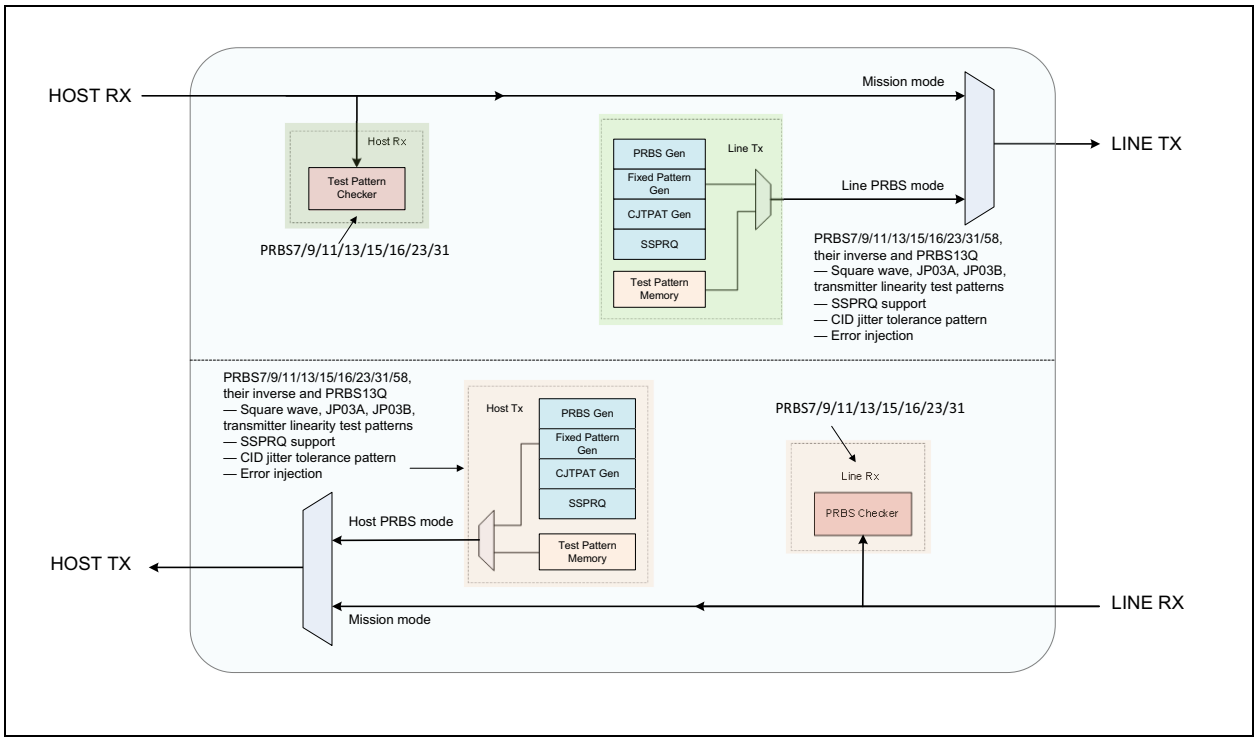
There are three GPIO toggle counters available which can be output from any of the GPIOs. Each GPIO toggle counter is clocked off a 1ms ‘tick’ counter. The toggle counter is 16-bits wide allowing for a toggle rate from 1ms to (2^{16}-1) ms (65 seconds).

3.6 Diagnostic Features

3.6.1 Pattern Generators/Checkers

Figure 16 below provides an overview of all the pattern generators and checkers available.

Figure 16 Location of Pattern Generators/Checkers



3.7 Microcontroller (MCU) and Software Considerations

Inphi PAM phys are highly integrated System-On-Chip (SOC) devices that include Host and Line interfaces, Protocol processing logic and a full featured DSP. The superior performance of these PAM devices is the result of a high performance analog front-end, and DSP/embedded microcontroller that execute firmware provided by Inphi to support link operations. Embedded firmware further simplifies device operation by reducing tasks to C-based API calls compiled in the end user's application. The high level of functionality precludes configuration of the phy through simple, direct register reads and writes. Inphi support is provided for phy operation with Inphi firmware and API exclusively.

3.7.1 Firmware and API

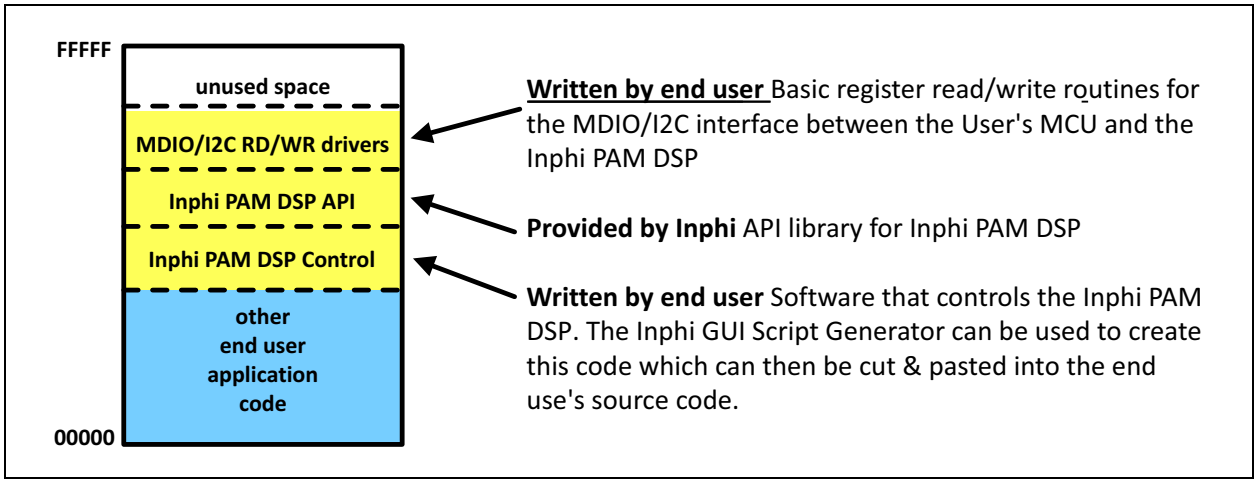
The current Firmware and API are always available on the Inphi website: www.inphi.com. The API distribution contains the API source code to be included in the application, extensive, detailed, HTML-based User's Guide, a copy of the latest Firmware, usage examples and a Quick Start Guide for configuring the software development environment. API are provided for all functions required by for all applications of the phy:

- Firmware download to the DSP
- Initialization of the DSP

- DSP status query
- Service provisioning of the DSP for all supported modes of operation
  - Mission Mode (retimer or DSP as applicable)
  - Diagnostic Loopback Modes
  - External Loopback Modes
- Link Status queries including extended statistics such as link SNR, Histogram and BER
- API for basic register R/W access.

Inphi also provides an Evaluation system with GUI to assist in DSP application development. The GUI includes C-code generation capability using the standard Inphi API to support all modes of DSP operation. This code can be used directly in the end-user's application software.

Figure 17 Typical Code Memory Map of User MCU



3.7.2 Firmware Size, Storage Options and External Memory Configurations

The user needs to provide 2M-bits of storage for the entire firmware image in the User MCU for direct download or a 2M-bit, external memory for boot from EEPROM or Flash option. Firmware code can be loaded in from an external EEPROM/Flash device connected directly to the Inphi PAM4 DSP devices through the SPI interface to configure the DSP parameters to the optimum settings. This application note provides a list of EEPROM and Flash memory devices that are compatible.

There are differences in SPI interfaces supported by different EEPROM/Flash vendors. The compatible devices have the option to program Page from 1 to N bytes (usually 256). The one with One Byte Program only is currently not supported. Flash devices have verified as listed below for references:

- On Semiconductor: LE25U40
- Adesto: AT25SF041

All options are shown in Figure 18 and Figure 19.

3.7.3 Firmware Download Options and Load Times

The time required from EEPROM/Flash download into DSP can be estimated with the following:

The MCU operates at approximately 250MHz on Porrima; the divided clock ratio is as follows:

SPI = 250/32 = 7.8125MHz

SPI = 250/16 = 15.625MHz

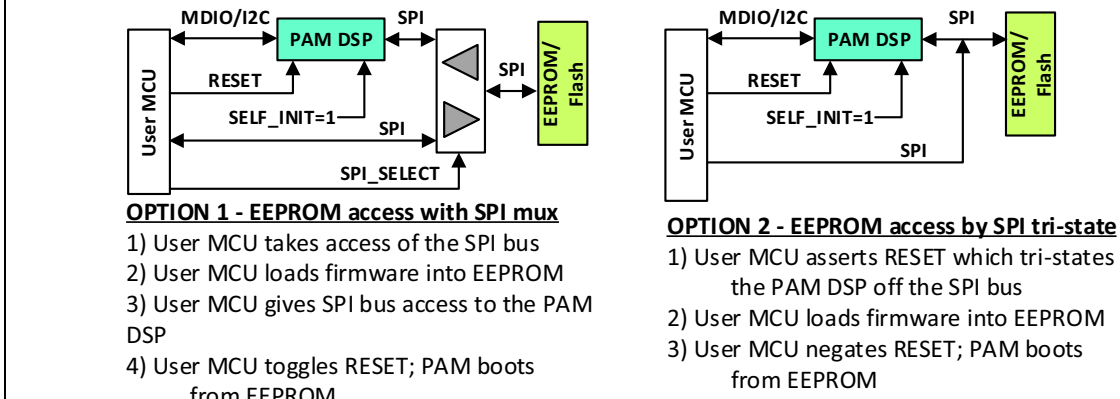
SPI = 250/8 = 31.25MHz

For example, when SPI clock speed is @7.8125MHz, download time can be estimated with FW size (Mbit)/SPI clock frequency, assuming the final Porrima FW size is approximately 2Mbit. Therefore:

= 2Mbits/7.8125MHz

= 256ms

Figure 18 Configurations with User MCU Sharing SPI Interface



OPTION 1 - EEPROM access with SPI mux

1) User MCU takes access of the SPI bus
2) User MCU loads firmware into EEPROM
3) User MCU gives SPI bus access to the PAM DSP
4) User MCU toggles RESET; PAM boots from EEPROM

OPTION 2 - EEPROM access by SPI tri-state

1) User MCU asserts RESET which tri-states the PAM DSP off the SPI bus
2) User MCU loads firmware into EEPROM
3) User MCU negates RESET; PAM boots from EEPROM

Figure 19 Configurations with User MCU Not Connected to the SPI Interface

OPTION 3 - Load EEPROM through PAM DSP

1) User MCU sets SELF_INIT = 0
2) User MCU loads firmware into EEPROM through the PAM DSP
3) User MCU sets SELF_INIT = 1
4) User MCU toggles RESET; PAM boots from EEPROM

OPTION 4 - Direct Download Mode

1) User MCU negates RESET
2) User MCU loads firmware directly into the PAM DSP program memory

3.7.4 SPI Interface Timing

Figure 20 SPI Interface Timing

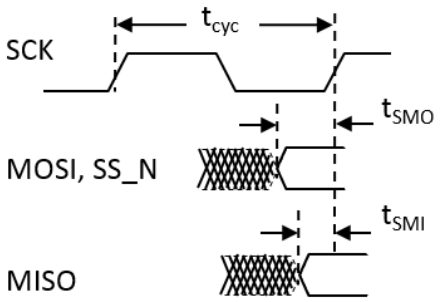


Table 4 SPI Interface Timing

Symbol	Parameter	Min	Max	Unit
t_{CYC}	SPI clock cycle	40	—	nsec
t_{SMO}	Master output signal valid to clock rising edge	10	—	nsec
t_{SMI}	Master input data valid to clock rising edge	5	—	nsec

3.7.5 Device Memory Map by Block

Table 5 Top MDIO Space Level Memory Map

Block	MDIO/I²C Address	Description
MMD08	21'h08_0000	MMD08 registers
MMD30_Core	21'h1E_0000	MMD30 Core and Efuse registers
LRX	21'h1E_2000	Optical Line Receive registers
LTX	21'h1E_4000	Optical Line Transmit registers
HRX	21'h1E_6000	Host Receive registers
HTX	21'h1E_8000	Host Transmit registers
MCU	21'h1E_A000	MCU Configuration registers
MCU_RXMBOX	21'h1E_A400	Receive mailbox
MCU_TXMBOX	21'h1E_A800	Transmit mailbox
RSVD	21'h1E_AC00	Reserved
TTC0	21'h1E_B000	Timer 0 IP, it includes timer [2:0].
TTC1	21'h1E_B100	Timer 1 IP, it includes timer [5:3].
TTC2	21'h1E_B200	Timer 2 IP, it includes timer [7:6].
WDT	21'h1E_B300	Watchdog Timer IP
SPI	21'h1E_B400	Serial Peripheral Interface Master

4.0 Design for Test

The Design for Test (DFT) structures have been inserted in the device to allow for structural slow & at-speed testing of digital logic, memories and IO pins using scan, memory BIST and boundary scan respectively.

4.1 JTAG Test Access Port

The device JTAG ports connects directly to the Test Access Port (TAP) controller. The TAP can perform a number of functions depending on the instruction shifted into the TAP's 4-bit instruction register. The TAP instructions are summarized in Table 6. The BYPASS, SAMPLE/PRELOAD, EXTEST, HIGHZ, CLAMP and IDCODE instructions conform to the IEEE 1149.1 standard and permit boundary scan testing. The device also supports IEEE 1149.6 AC JTAG on all the high speed interfaces.

The JTAG ports are also shared with the TAP controller inside the MCU. By default, after reset, the DFT TAP is selected and the MCU TAP is deselected. The selection can be switched a the configuration bit. This register bit protected in scan mode so it will always be selecting the DFT TAP during scan testing.

Table 6 TAP Instruction Set

Instruction Name	Description
BYPASS	Select the single-bit bypass register, creating a single-bit shift register path from the TDI pin, to the bypass register, and to the TDO pin.
SAMPLE/PRELOAD	This instruction provides two separate functions: • Obtains a sample of the signals present at the input pins. The sampled data can be observed by shifting it through it through the boundary scan register to the TDO output. • Initializes the boundary scan register before selecting EXTEST or CLAMP.
EXTEST	Forces all output balls (and bi-directional balls configured as outputs), to the preloaded fixed values (with the SAMPLE/PRELOAD instruction).
EXTEST_PULSE	Causes data produced by drivers to be inverted on the first falling edge of TCLK after entering the *Run-Test/Idle* TAP control state. IEEE 1149.6 instruction. All DC pins will perform as if the IEEE 1149.1 EXTEST instruction is operating.
EXTEST_TRAIN	Causes data produced by drivers to be inverted on the first falling edge of TCK after entering the *Run-Test/Idle* TAP controller state, and to be subsequently toggled on each falling edge of TCLK. IEEE 1149.6 instruction. All DC pins will perform as if the IEEE 1149.1 EXTEST instruction is operating.
HIGHZ	All outputs and bi-directional ball are tri-stated.
CLAMP	Holds boundary scan register data for subsequent scan out.
IDCODE	Scan out the manufacturer ID code.
USER_DATA_REG	Access the x-bit user data register.

5.0 Pinout

The pinout for the Porrima 400G DSP is described in the following sections.

5.1 Analog High Speed Serial Interfaces

Table 7 Analog High Speed Serial Interfaces

Signal	Rate	Type	Description
Line Side Interface			
LRXP/N1...4	53.125 Gbaud	Analog Input	100Ω, Line Differential Receiver, lanes 1...4
LTXP/N1...4	53.125 Gbaud	Analog Output	100Ω, Line Differential Transmitter, lanes 1...4
Host Side Interface			
HRXP/N1...8	26.56 Gbaud	Analog Input	100Ω, Host Differential Receiver, lanes 1...8
HTXP/N1...8	26.56 Gbaud	Analog Output	100Ω, Host Differential Transmitter, lanes 1...8
Note: 1. For proper lane mapping refer to "Lane Mapping Application Note" in Appendix A			

5.2 Analog Rx Reference Clocks

Table 8 Analog Rx Reference Clocks

Signal	Rate	Type	Description
REFCP/N	156.25MHz	Analog Input	100Ω, Reference Clock Input.

5.3 Analog Test Pins

Table 9 Analog Test Pins

Signal	Rate	Type	Description
ATB_P/N	Analog	Output	Analog test bus output for monitoring/testing and trimming.
MONCKP/N	Analog	Output	Test clock out.

5.4 Supplies

Table 10 Supplies

Signal	Rate	Type	Description
AVDDR_LTX_DRV	DC	Supply	1.05V Analog Supply for TX driver
AVDDR_TX			1.05V Analog Supply for the TX interface
AVDDR_LRX			1.05V Analog Supply for Line Rx interface
AVDDR_HRX			1.05V Analog Supply for Host Rx interface
AVDDR_PLL			1.05V Analog Supply for Line PLL
AVDDR_PLL_HRX			1.05V Analog Supply for Host PLL
VQPS			GND
VDDMDIO_1P2			1.05V digital I/O supply.
VDDMDIO_3P3			3.3V digital I/O supply.
VDD			0.65V digital supply
VSS			GND

5.5 Management Interface

Table 11 Management Interface (Sheet 1 of 2)

Signal	Rate	Type/ Output Drive (mA)	Description
Management Interface			
RESET_N	DC	Input PD	Asynchronous, active low, reset. No clock relationship is assumed. Minimum assertion time of 1 ms.
I2CSEL	DC	Input PD	Select management interface mode of operation: 0 = MDIO Mode 1 = I2C Mode
MDIO (SDA)	25MHz (MDIO mode) 1MHz (I2C)	I/O PU 16mA	MDIO mode: Management Data Input/output Bidirectional pin used to pass management data into or out of the device. MDIO is synchronous to MDC. I2C mode: Serial Data Input/Output. Bidirectional pin used to pass management data into or out of the device. SDA should only be change changed whilst SCL is low, except for START and STOP conditions. This output is only ever driven low. When driving a one, the output is disabled and the required external pull-up pulls the signal high. Operates off the VDDMDIO_1P2 supply. This I/O is only active when MDIO_SEL is low.
MDIO_3P3	25MHz (MDIO mode) 1MHz (I2C)	I/O PU 16mA	As above, but operates off the VDDMDIO_3P3 supply. This I/O is only active when MDIO_SEL is high.
MDC (SCL)	25MHz (MDIO mode) 1MHz (I2C)	Input PD	Management Data clock (MDIO mode) or I2C Serial Clock Pin used to clock management data into or out of the device. Operates off the VDDMDIO_1P2 supply. This I/O is only active when MDIO_SEL is low.

Table 11 Management Interface (Sheet 2 of 2)

Signal	Rate	Type/ Output Drive (mA)	Description
MDC_3P3	25MHz (MDIO mode) 1MHz (I2C)	Input PD	As above, but operates off the VDDMDIO_3P3 supply. This I/O is only active when MDIO_SEL is high.
PHYADR0 PHYADR1 PHYADR2	DC	Input PD	PHYADR0-2 are configuration pins that provide the 3-bit PHY address that the device will respond to. I2C Mode: Corresponds to bits [7:3] of the 7b device address that the device will respond to. If left unconnected, the MDIO PHYADR will be 5'b00000, and the 7b I2C device address will be 0x00.
SPI Interface			
SCK		Output 8mA	SPI Serial Clock. NOTE: SCK, SS_N, MOSI and MISO are on the 3.3V supply rail (VDDMDIO_3P3)
SS_N		Output PU 8mA	SPI Chip Select. Active low.
MOSI		Output 8mA	SPI Master data output.
MISO		Input	SPI Master data input.
WPN		Output 8mA	SPI Write Protect. Active low.Do not use.
SELF_INIT	DC	Input PD	SPI Self Initialization enable. This input pin when set, causes the MCU to start downloading the Application code from the External EEPROM/Flash into the internal memory (iRAM)

5.6 Test Interface

Table 12 Test Interface

Signal	Rate	Type	Description
TRST_N	DC	Input PD	Test Reset, Active low. If not being used, ensure that this pin is tied low.
TCK		Input PD	Test Clock used for JTAG operations.
TMS	DC	Input PD	Test Mode Select. Controls TAP state. Sampled synchronously to the rising edge of TCK.
TDI		Input PD	Test Data In. Serial input data. Sampled synchronously to the rising edge of TCK.
TDO		Output 16mA	Test Data Out. Serial Output Data. Changes state synchronously to the falling edge of TCK.

5.7 Miscellaneous

Table 13 Miscellaneous

Signal	Rate	Type	Description
INTR_N	DC	Output (Inout) PU 12mA	Interrupt output, Active low. Can also be reconfigured as a GPIO.
LOL_0N		Output (Inout) PU 12mA	Loss of lock output for Lambda-0. Active low. Can also be reconfigured as a GPIO.
LOL_1N		Output (Inout) PU 12mA	Loss of lock output for Lambda-1. Active low. Can also be reconfigured as a GPIO.
LOL_2N		Output (Inout) PU 12mA	Loss of lock output for Lambda-2. Active low. Can also be reconfigured as a GPIO.
LOL_3N		Output (Inout) PU 12mA	Loss of lock output for Lambda-3. Active low. Can also be reconfigured as a GPIO.
GPIO_0 GPIO_1 GPIO_2 GPIO_3		Inout PD 8mA	General Purpose I/O. By default, are configured as inputs. Note GPIO_3 is a dedicated input used for debug clock functionality and has no usage as GPIOs.
GPIO_0_3P3 GPIO_1_3P3		Inout PD 8mA	As above, but operates off the VDDMDIO_3P3 supply.
MDIO_SEL	DC	Input PD	Selects either 1P2 V or 3P3 V operation for MDIO and MDC. When low selects 1.2V operation. When high selects 3.3V operation.

5.8 Digital I/O Drive

All the digital I/O have programmable output drive strengths. Maximum operating frequency at VDDIO = 1.05V is 40MHz and the max, load capacitance is 20pF. The default drive strengths are listed in the pin list tables in the previous tables, but can be changed any time after reset via register programming.

5.9 Low-Speed Signals

Table 14 Low Speed Signals

Signal Name	VDDGPIO_1P2 1.05V	VDDMDIO_1P2 1.05V	VDDMDIO_3P3 3.3V (1)	Type if used as input (2)	Drive as output. Value is register programmable
GPIO_0	X			pull-down	8mA
GPIO_1	X			pull-down	8mA
GPIO_2	X			pull-down	8mA
GPIO_3	X			Must be GND	-
GPIO_4	X			pull-down	8mA
GPIO_5	X			pull-down	8mA
GPIO_6	X			pull-down	8mA
MDIO_SEL	X			pull-down	-
TCK	X			pull-down	-
TDI	X			pull-down	-
TDO	X			-	16mA
TMS	X			pull-down	-
TRST_N	X			pull-down	-
I2CSEL		X		pull-down	-
INTR_N		X		pull-down	12mA (3)
LOL_0-3N		X		pull-down	12mA (4)
MDC(SCL)		X (5)		pull-down	-
MDIO(SDA)		X (5)		pull-up	16mA
PHYADR0,1,2,3,4		X		pull-down	-
TIA_CTRL0		X			
TIA_CTRL1		X			
TIA_CTRL2		X			
TIA_CTRL3		X			
RESET_N		X		pull-down	-
SELF_INIT		X		pull-down	-
WP_N			X	-	8mA
GPIO_0_3P3			X	pull-down	8mA
GPIO_1_3P3			X	pull-down	8mA
MDC(SCL)_3P3			X (5)	pull-down	-
MDIO(SDA)_3P3			X (5)	pull-up	16mA
MISO			X	input	-
MOSI			X	-	8mA
SCK			X	-	8mA
SS_N			X	pull-up	8mA

Notes:

1. If 3.3V MDIO is not used, connect VDDMDIO_3P3 to VDDMDIO_1P2
2. Pull-down and pull-up are internal, weak terminations - >10K-Ω
3. To simplify multi-phy applications, INTR_N is open-drain. All other outputs are push/pull.
4. For ease of use, under firmware control, LOL for all lanes can be configured to output on LOL_0N
5. Only one MDIO (I2C) interface can be used at a time; either the 1.05V or the 3.3V

6.0 Electrical Specifications

The Porrima 400G DSP meets all functional requirements when operated over the specified timing, electrical, and temperature ranges in the correctly configured mode.

6.1 Absolute Maximum Ratings

The absolute maximum ratings, as specified in Table 15, are those ratings beyond which the device's lifetime and reliability may be impaired. Functional operation and meeting of electrical specifications is not guaranteed when the device is subjected to the absolute maximum ratings.

Table 15 Absolute Maximum Ratings

Symbol	Parameter[1]	Min	Max	Units
VDDMDIO_1P2 VDDGPIO_1P2 AVDDR	Positive 1.05V Power Supply	-0.3	1.15	V
VDDMDIO_3P3	Positive 3.3V Power Supply	-0.3	3.6	V
VDD	Positive 0.65V Power Supply	-0.3	.85	V
Tj	Absolute maximum junction temperature under bias: Short term Long term	 -40 0	 125 110	C
TSTG	Storage temperature	-40	150	C
Vout	Voltage at any low-speed output Voltage at any high-speed output			V
Vin	Voltage at any low-speed input Voltage at any high-speed input			V
Iout	Current at any output	-20	20	mA
Iin	Current at any input	-20	20	mA
-	Lead free soldering temperature (10 sec)	n/a	260	C
ESD	Electrostatic discharge Human Body Model (HBM) (100pF, 1.5kΩ): All pins > 5Gbps All pins < 5Gbps Charge Device Model (CDM): All pins	 — — -250	 1k 2k 250	V
Latchup	Latchup current	-100	100	mA

1. All voltages measured relative to VSS balls.

6.2 Recommended Operating Conditions

The operating ranges shall be in accordance with the following table.

Table 16 Recommended Operating Conditions

AC Noise					
Power Supply Rail	**Nominal Voltage (V)**	**0.1MHz-5MHz**	**>5MHz**	**Total AC Noise**	**DC level**
VDDMDIO_3P3	3.3	-	-	35mVp-p	±5%
VDDMDIO_1P2	1.05	-	-	35mVp-p	±5%
AVDDR_PLL		5mV p-p			±2.5%
AVDDR_PLL_HRX					
AVDDR_HRX					
AVDDR_LRX					
AVDDR_TX					
AVDDR_LTX_DRV					
VDD	0.65	-	-	35mVp-p	

Notes:
1. AC noise is measured at the balls of the part, after filtering
2. AVDDR_PLL requires a ferrite bead to reduce noise

Figure 21 Recommended Filtering

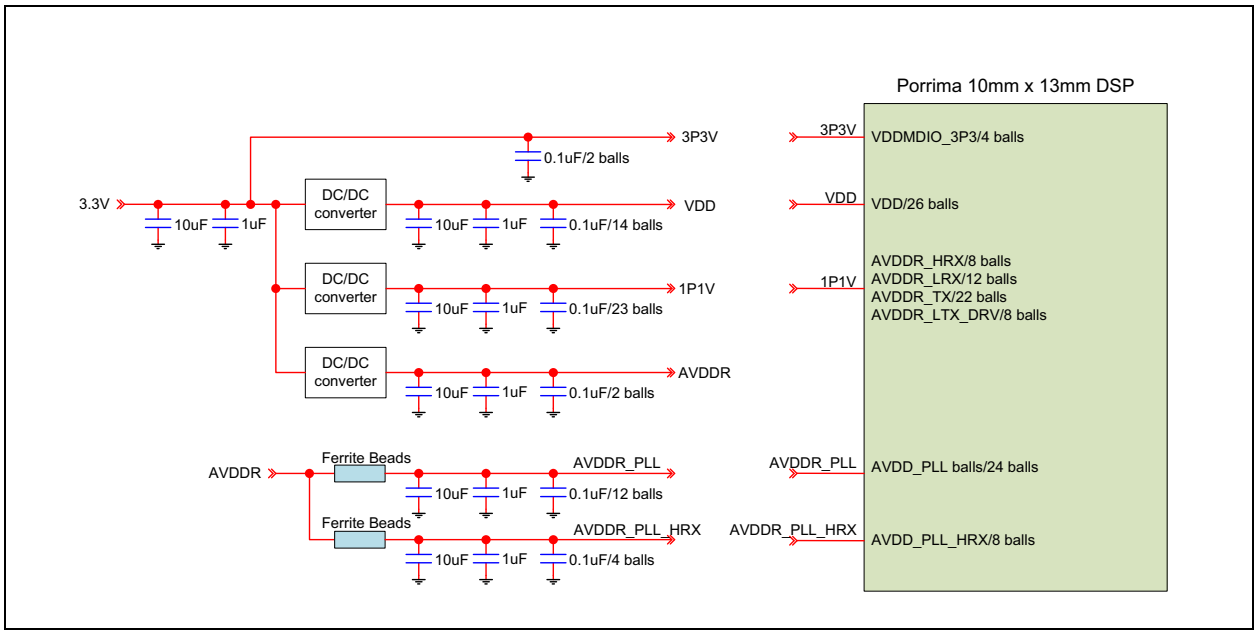


Figure 22 AVDDR Power Filter Diagram

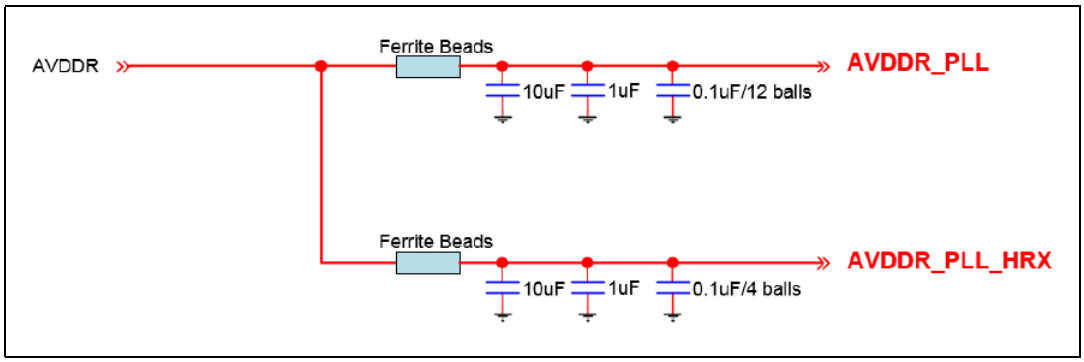
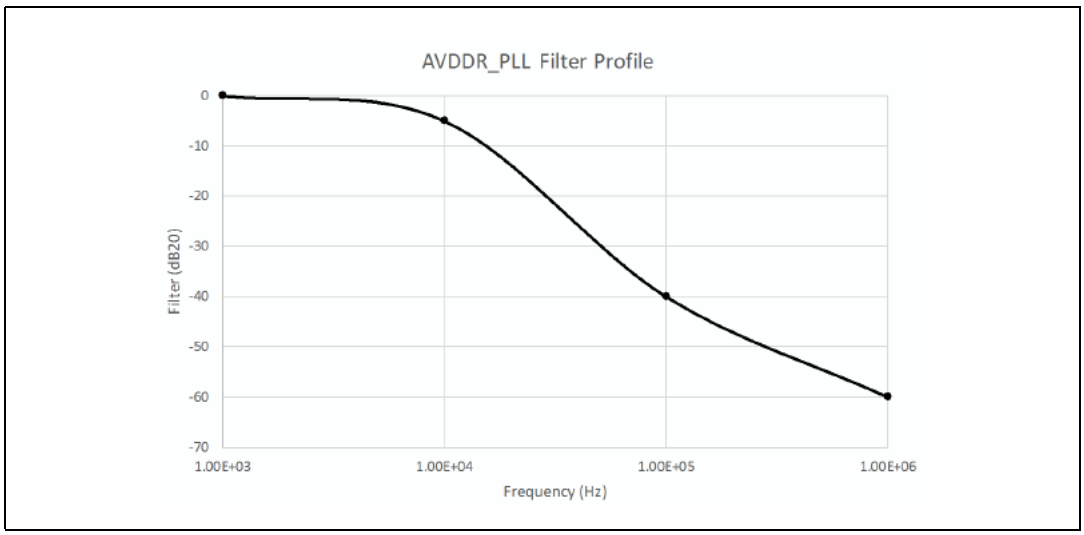


Figure 23 AVDDR Power Filter Plot



The VDD and 1.05V AVDDR supplies are common to all applications. VDDMDIO3P3 is required if either the SPI (EEPROM/Flash) or 3.3V Compatible MDIO/I2C interfaces are used.

Power regulators should be designed with a minimum of 50% overhead (above operating max. power). Regulators designed to operate at maximum efficiency provide this overhead because max. regulator efficiency is achieved at less than 60% of max. regulator current.

6.3 Porrima 400G DSP Power Sequencing

The power sequence should bring up the 3.3V supply first, then the rest of the supplies sequenced from low (0.65V) to high.

6.4 Power Dissipation

Power dissipation and supply current numbers are provided in Table 17 and Table 18 respectively. Number are quoted per lane.

Table 17 Porrima 400G DSP Power Dissipation

Mode	Typical Power[1]
Simple Retimer Mode with Slicer	4900mV

Note:
1. Typical power is quoted at nominal supplies with a Tj=50C, and for a “typical” manufacturing process. Power varies based on operating mode and features selected.

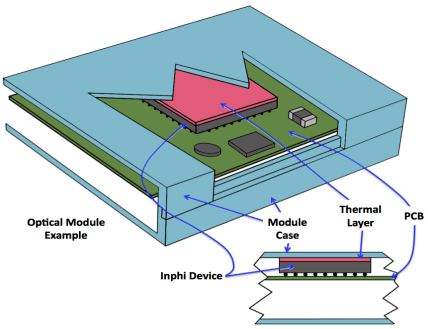
6.5 Thermal Characteristics

Table 18 Thermal Characteristics

Parameter	Value	Units
ThetaJC	2.23	^{o}C/W
ThetaJB	2.39	^{o}C/W
Tcase(max)	85	^{o}C

6.6 Mechanical Pressure Limits

Figure 24 Typical Application



Description	Value (Max)	Units
Since short Term Pressure for heatsink attach	5.582	kgf
Constant long term pressure	1.907	kgf

Table 19 1.05V I/O DC Characteristics

Parameter		Min.	Norm.	Max.	Units
VDD	Core Voltage	0.634	0.65	0.667	V
VDDMDIO_1P2 VDDGPIO_1P2 AVDDR	IO Supply Voltage	1.023	1.05	1.077	V
VDD ramp-up slew	Ramp-up slew for VDD	—	—	0.018	V/us
VDDIO ramp-up slew	Ramp-up slew for VDDIO	—	—	0.018	V/us
ViL	Input Low Voltage	—	—	0.7	V
ViH	Input High Voltage	0.8	—	—	V

Table 19 1.05V I/O DC Characteristics

Ii	Input Leakage Current @ Vo=1.05 or 0V	—	—	±10µ	A
Loz	Tri-state Output Leakage Current @Vo=1.05V or 0V	—	—	±10µ	A
RPU	Pull-up Resistor	56k	90k	168k	Ω
RPD	Pull-down Resistor	60k	91k	168k	Ω
VOL	Output Low Voltage	—	—	0.2	V
VOH	Output High Voltage	0.9	—	—	V

Table 20 3.3V I/O DC Characteristics

Parameter		Min.	Norm.	Max.	Units
VDDMDIO_3P3	IO Supply Voltage	3.14	3.3	3.46	V
VDD ramp-up slew	Ramp-up slew for VDD	—	—	0.018	V/us
VDDMDIO_3P3 ramp-up slew	Ramp-up slew for VDDIO	—	—	0.018	V/us
ViL	Input Low Voltage	-0.3	—	0.825	V
ViH	Input High Voltage	1.85	—	3.3	V
VT	Threshold Point	0.81	1	1.23	V
VTPU	Threshold Point with Pull-up Resistor Enabled	0.79	0.93	1.21	V
VTPD	Threshold Point with Pull-down Resistor Enabled	0.82	1.01	1.24	V
Ii	Input Leakage Current @ Vo=1.05 or 0V	—	—	±10µ	A
Loz	Tri-state Output Leakage Current @Vo=1.05V or 0V	—	—	±10µ	A
RPU	Pull-up Resistor	—	35k	—	Ω
RPD	Pull-down Resistor	—	35k	—	Ω
VOL	Output Low Voltage	—	—	0.375	V
VOH	Output High Voltage	2.25	—	—	V

6.7 AC Characteristics

Preliminary results. Data will be updated when testing is complete. Unless otherwise indicated, all compliance testing is performed at a junction temperature of 110C.

6.7.1 Reference Clock

It is recommended the device providing the REFCLK to the Porrima 400G DSP device meet the following minimal requirements:

Table 21 REFCLK Specifications

Parameters	Conditions	Min	Max	Units
Frequency		156.25	156.25	MHz
Frequency Tolerance		--	100	ppm
Differential Swing	Peak-to-peak	400	1600	mV
Single-ended Swing	Peak-to-peak	200	800	mV
Duty Cycle		40	60	%
Rise Time	20% to 80%	--	400	ps
Fall Time	80% to 20%	--	400	ps
AC Coupling		1	100	nF
RMS Jitter	12kHz – 1MHz	--	200	fs
	1MHz – 20MHz	--	250	fs
	12kHz – 20MHz	--	360	fs

7.0 Ball-Out and Packaging

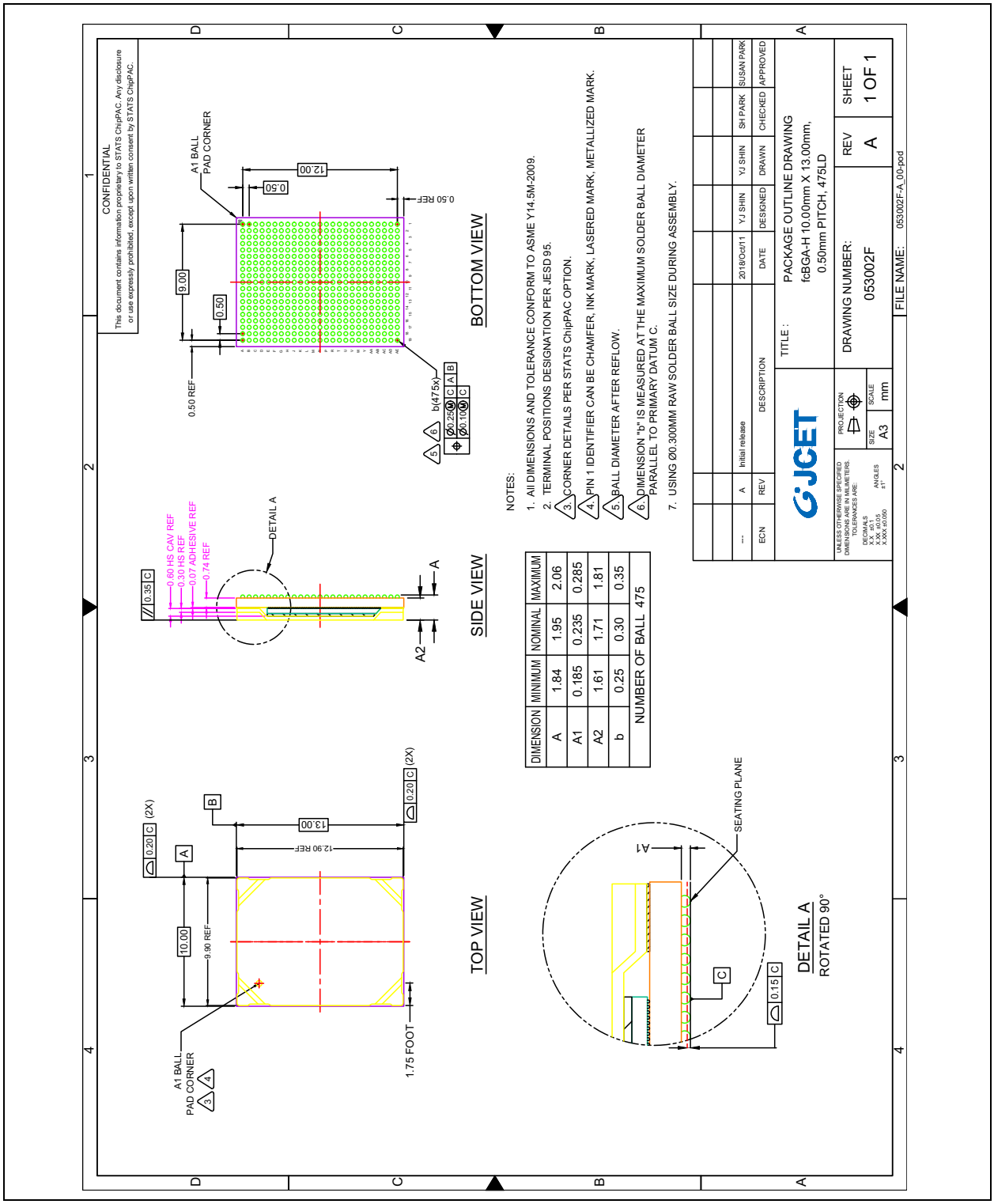
7.1 Package Ball-Out (10 mm × 13 mm, Ball Pitch 0.5 mm)

Figure 25 Ball Out

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	VSS	VSS	VSS	VSS	REFCN	REFCP	VSS	TCK	TIA_CTRL3	TIA_CTRL2	LOL_0N	LOL_2N	LOL_1N	LOL_3N	GPIO_2	GPIO_1	TRST_N	VSS	VSS	A
B	HTXN2	VSS	HTXN1	VSS	VSS	VSS	VSS	TMS	GPIO_3	MDIO_SEL	TIA_CTRL1	TIA_CTRL0	TDI	TDO	GPIO_5	GPIO_0	GPIO_4	VSS	LRXN1	B
C	HTXP2	VSS	HTXP1	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	VDDGPIO_1P2	VDDGPIO_1P2	VSS	GPIO_6	VSS	LRXP1	C
D	VSS	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	VDDGPIO_1P2	VDDGPIO_1P2	VSS	VSS	VSS	VSS	D
E	HTXN4	VSS	HTXN3	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VDD	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	LRXN2	E
F	HTXP4	VSS	HTXP3	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VDD	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	LRXP2	F
G	VSS	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	VSS	G
H	HTXN6	VSS	HTXN5	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	LRXN3	H
J	HTXP6	VSS	HTXP5	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD_DR4	VDD_DR4	VDD_DR4	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	LRXP3	J
K	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD_DR4	VDD_DR4	VDD_DR4	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	VSS	K
L	HTXN8	VSS	HTXN7	VSS	AVDDR_PLL_HRX	AVDDR_PLL_HRX	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	LRXN4	L
M	HTXP8	VSS	HTXP7	VSS	AVDDR_PLL_HRX	AVDDR_PLL_HRX	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	LRXP4	M
N	VSS	VSS	VSS	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VDD_DR4	VDD_DR4	VDD_DR4	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	VSS	N
P	HRXP7	VSS	HRXP8	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VDD_DR4	VDD_DR4	VDD_DR4	VSS	VSS	AVDDR_LRX	AVDDR_LRX	VSS	LTXP4	P
R	HRXN7	VSS	HRXN8	VSS	AVDDR_PLL_HRX	AVDDR_PLL_HRX	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	LTXN4	R
T	VSS	VSS	VSS	VSS	AVDDR_PLL_HRX	AVDDR_PLL_HRX	VSS	VSS	VDD	VDD	VSS	VSS	VSS	AVDDR_PLL	AVDDR_PLL	VSS	VSS	VSS	VSS	T
U	HRXP5	VSS	HRXP6	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	AVDDR_TX	AVDDR_TX	AVDDR_TX	VSS	VSS	AVDDR_LTX_DRV	AVDDR_LTX_DRV	VSS	LTXP3	U
V	HRXN5	VSS	HRXN6	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	AVDDR_TX	AVDDR_TX	AVDDR_TX	VSS	VSS	AVDDR_LTX_DRV	AVDDR_LTX_DRV	VSS	LTXN3	V
W	VSS	VSS	VSS	VSS	AVDDR_HRX	AVDDR_HRX	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VSS	VSS	W
Y	HRXP3	VSS	HRXP4	VSS	AVDDR_HRX	AVDDR_HRX	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VSS	AVDDR_TX	AVDDR_TX	VSS	VSS	VSS	LTXP2	Y
AA	HRXN3	VSS	HRXN4	VSS	VSS	VSS	AVDDR_HRX	AVDDR_HRX	VSS	VSS	VDDMDIO_1P2	VDDMDIO_1P2	VSS	VSS	VSS	AVDDR_LTX_DRV	AVDDR_LTX_DRV	VSS	LTXN2	AA
AB	VSS	VSS	VSS	VSS	VSS	VSS	AVDDR_HRX	AVDDR_HRX	VSS	VSS	VDDMDIO_1P2	VDDMDIO_1P2	VDDMDIO_3P3	VDDMDIO_3P3	VSS	AVDDR_LTX_DRV	AVDDR_LTX_DRV	VSS	VSS	AB
AC	HRXP1	VSS	HRXP2	VSS	VSS	VSS	VSS	PHYADR3	PHYADR4	PSRTCK	ATB_P	ATB_N	VDDMDIO_3P3	VDDMDIO_3P3	VSS	VSS	VSS	VSS	LTXP1	AC
AD	HRXN1	VSS	HRXN2	VSS	MDIO_3P3	INTR_N	VQPS	SELF_INIT	GPIO_1_3P3	MDC	SS_N	WP_N	MOSI	MISO	VSS	VSS	VSS	VSS	LTXN1	AD
AE	VSS	VSS	VSS	VSS	MDC_3P3	PHYADR0	PHYADR1	LDO_3P3	GPIO_0_3P3	MDIO	I2CSEL	RESET_N	PHYADR2	SCK	VSS	MONCKN	MONCKP	VSS	VSS	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

7.2 Package

Figure 26 Porrima 400G DSP Package Drawing



7.3 Ball List

Table 22 Alphabetical Listing by Ball

Ball	Signal
A1	VSS
A2	VSS
A3	VSS
A4	VSS
A5	REFCN
A6	REFCP
A7	VSS
A8	TCK
A9	TIA_CTRL3
A10	TIA_CTRL2
A11	LOL_0N
A12	LOL_2N
A13	LOL_1N
A14	LOL_3N
A15	GPIO_2
A16	GPIO_1
A17	TRST_N
A18	VSS
A19	VSS
B1	HTXN2
B2	VSS
B3	HTXN1
B4	VSS
B5	VSS
B6	VSS
B7	VSS
B8	TMS
B9	GPIO_3
B10	MDIO_SEL
B11	TIA_CTRL1
B12	TIA_CTRL0
B13	TDI
B14	TDO
B15	GPIO_5
B16	GPIO_0
B17	GPIO_4
B18	VSS
B19	LRXN1
C1	HTXP2
C2	VSS
C3	HTXP1
C4	VSS
C5	AVDDR_PLL
C6	AVDDR_PLL
C7	VSS
C8	VSS
C9	AVDDR_PLL
C10	AVDDR_PLL
C11	VSS
C12	VSS
C13	VSS
C14	VDDGPIO_1P2
C15	VDDGPIO_1P2
C16	VSS
C17	GPIO_6
C18	VSS
C19	LRXP1
D1	VSS
D2	VSS
D3	VSS
D4	VSS
D5	AVDDR_PLL
D6	AVDDR_PLL
D7	VSS
D8	VSS
D9	AVDDR_PLL
D10	AVDDR_PLL
D11	VSS
D12	VSS
D13	VSS
D14	VDDGPIO_1P2
D15	VDDGPIO_1P2
D16	VSS
D17	VSS
D18	VSS
D19	VSS
E1	HTXN4
E2	VSS
E3	HTXN3
E4	VSS
E5	VSS
E6	VSS
E7	VDD
E8	VDD
E9	VSS
E10	VSS
E11	VDD
E12	VDD
E13	VDD
E14	VSS
E15	VSS
E16	AVDDR_LRX
E17	AVDDR_LRX
E18	VSS
E19	LRXN2
F1	HTXP4
F2	VSS
F3	HTXP3
F4	VSS
F5	VSS
F6	VSS
F7	VDD
F8	VDD
F9	VSS
F10	VSS
F11	VDD
F12	VDD
F13	VDD
F14	VSS
F15	VSS
F16	AVDDR_LRX

Ball	Signal
F17	AVDDR_LRX
F18	VSS
F19	LRXP2
G1	VSS
G2	VSS
G3	VSS
G4	VSS
G5	AVDDR_PLL
G6	AVDDR_PLL
G7	VSS
G8	VSS
G9	VDD
G10	VDD
G11	VSS
G12	VSS
G13	VSS
G14	AVDDR_PLL
G15	AVDDR_PLL
G16	VSS
G17	VSS
G18	VSS
G19	VSS
H1	HTXN6
H2	VSS
H3	HTXN5
H4	VSS
H5	AVDDR_PLL
H6	AVDDR_PLL
H7	VSS
H8	VSS
H9	VDD
H10	VDD
H11	VSS
H12	VSS
H13	VSS
H14	AVDDR_PLL
H15	AVDDR_PLL
H16	VSS
H17	VSS

Ball	Signal
H18	VSS
H19	LRXN3
J1	HTXP6
J2	VSS
J3	HTXP5
J4	VSS
J5	VSS
J6	VSS
J7	VDD
J8	VDD
J9	VSS
J10	VSS
J11	VDD
J12	VDD
J13	VDD
J14	VSS
J15	VSS
J16	AVDDR_LRX
J17	AVDDR_LRX
J18	VSS
J19	LRXP3
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K5	VSS
K6	VSS
K7	VDD
K8	VDD
K9	VSS
K10	VSS
K11	VDD
K12	VDD
K13	VDD
K14	VSS
K15	VSS
K16	AVDDR_LRX
K17	AVDDR_LRX
K18	VSS

Ball	Signal
K19	VSS
L1	HTXN8
L2	VSS
L3	HTXN7
L4	VSS
L5	AVDDR_PLL_HRX
L6	AVDDR_PLL_HRX
L7	VSS
L8	VSS
L9	VDD
L10	VDD
L11	VSS
L12	VSS
L13	VSS
L14	AVDDR_PLL
L15	AVDDR_PLL
L16	VSS
L17	VSS
L18	VSS
L19	LRXN4
M1	HTXP8
M2	VSS
M3	HTXP7
M4	VSS
M5	AVDDR_PLL_HRX
M6	AVDDR_PLL_HRX
M7	VSS
M8	VSS
M9	VDD
M10	VDD
M11	VSS
M12	VSS
M13	VSS
M14	AVDDR_PLL
M15	AVDDR_PLL
M16	VSS
M17	VSS

Ball	Signal
M18	VSS
M19	LRXP4
N1	VSS
N2	VSS
N3	VSS
N4	VSS
N5	VSS
N6	VSS
N7	AVDDR_TX
N8	AVDDR_TX
N9	VSS
N10	VSS
N11	VDD
N12	VDD
N13	VDD
N14	VSS
N15	VSS
N16	AVDDR_LRX
N17	AVDDR_LRX
N18	VSS
N19	VSS
P1	HRXP7
P2	VSS
P3	HRXP8
P4	VSS
P5	VSS
P6	VSS
P7	AVDDR_TX
P8	AVDDR_TX
P9	VSS
P10	VSS
P11	VDD
P12	VDD
P13	VDD
P14	VSS
P15	VSS
P16	AVDDR_LRX
P17	AVDDR_LRX
P18	VSS

Ball	Signal
P19	LTXP4
R1	HRXN7
R2	VSS
R3	HRXN8
R4	VSS
R5	AVDDR_PLL_HRX
R6	AVDDR_PLL_HRX
R7	VSS
R8	VSS
R9	VDD
R10	VDD
R11	VSS
R12	VSS
R13	VSS
R14	AVDDR_PLL
R15	AVDDR_PLL
R16	VSS
R17	VSS
R18	VSS
R19	LTXN4
T1	VSS
T2	VSS
T3	VSS
T4	VSS
T5	AVDDR_PLL_HRX
T6	AVDDR_PLL_HRX
T7	VSS
T8	VSS
T9	VDD
T10	VDD
T11	VSS
T12	VSS
T13	VSS
T14	AVDDR_PLL
T15	AVDDR_PLL
T16	VSS
T17	VSS

Ball	Signal
T18	VSS
T19	VSS
U1	HRXP5
U2	VSS
U3	HRXP6
U4	VSS
U5	VSS
U6	VSS
U7	AVDDR_TX
U8	AVDDR_TX
U9	VSS
U10	VSS
U11	AVDDR_TX
U12	AVDDR_TX
U13	AVDDR_TX
U14	VSS
U15	VSS
U16	AVDDR_LTX_DRV
U17	AVDDR_LTX_DRV
U18	VSS
U19	LTXP3
V1	HRXN5
V2	VSS
V3	HRXN6
V4	VSS
V5	VSS
V6	VSS
V7	AVDDR_TX
V8	AVDDR_TX
V9	VSS
V10	VSS
V11	AVDDR_TX
V12	AVDDR_TX
V13	AVDDR_TX
V14	VSS
V15	VSS
V16	AVDDR_LTX_DRV

Ball	Signal
V17	AVDDR_LTX_DRV
V18	VSS
V19	LTXN3
W1	VSS
W2	VSS
W3	VSS
W4	VSS
W5	AVDDR_HRX
W6	AVDDR_HRX
W7	VSS
W8	VSS
W9	AVDDR_TX
W10	AVDDR_TX
W11	VSS
W12	VSS
W13	VSS
W14	AVDDR_TX
W15	AVDDR_TX
W16	VSS
W17	VSS
W18	VSS
W19	VSS
Y1	HRXP3
Y2	VSS
Y3	HRXP4
Y4	VSS
Y5	AVDDR_HRX
Y6	AVDDR_HRX
Y7	VSS
Y8	VSS
Y9	AVDDR_TX
Y10	AVDDR_TX
Y11	VSS
Y12	VSS
Y13	VSS
Y14	AVDDR_TX
Y15	AVDDR_TX
Y16	VSS
Y17	VSS

Ball	Signal
Y18	VSS
Y19	LTXP2
AA1	HRXN3
AA2	VSS
AA3	HRXN4
AA4	VSS
AA5	VSS
AA6	VSS
AA7	AVDDR_HRX
AA8	AVDDR_HRX
AA9	VSS
AA10	VSS
AA11	VDDMDIO_1P2
AA12	VDDMDIO_1P2
AA13	VSS
AA14	VSS
AA15	VSS
AA16	AVDDR_LTX_DRV
AA17	AVDDR_LTX_DRV
AA18	VSS
AA19	LTXN2
AB1	VSS
AB2	VSS
AB3	VSS
AB4	VSS
AB5	VSS
AB6	VSS
AB7	AVDDR_HRX
AB8	AVDDR_HRX
AB9	VSS
AB10	VSS
AB11	VDDMDIO_1P2
AB12	VDDMDIO_1P2
AB13	VDDMDIO_3P3
AB14	VDDMDIO_3P3
AB15	VSS
AB16	AVDDR_LTX_DRV

Ball	Signal
AB17	AVDDR_LTX_DRV
AB18	VSS
AB19	VSS
AC1	HRXP1
AC2	VSS
AC3	HRXP2
AC4	VSS
AC5	VSS
AC6	VSS
AC7	VSS
AC8	PHYADR3
AC9	PHYADR4
AC10	PSRTCK
AC11	ATB_P
AC12	ATB_N
AC13	VDDMDIO_3P3
AC14	VDDMDIO_3P3
AC15	VSS
AC16	VSS
AC17	VSS
AC18	VSS
AC19	LTXP1
AD1	HRXN1
AD2	VSS
AD3	HRXN2
AD4	VSS
AD5	MDIO_3P3
AD6	INTR_N
AD7	VQPS
AD8	SELF_INIT
AD9	GPIO_1_3P3
AD10	MDC
AD11	SS_N
AD12	WP_N
AD13	MOSI
AD14	MISO
AD15	VSS
AD16	VSS
AD17	VSS

Ball	Signal
AD18	VSS
AD19	LTXN1
AE1	VSS
AE2	VSS
AE3	VSS
AE4	VSS
AE5	MDC_3P3
AE6	PHYADR0
AE7	PHYADR1
AE8	LDO_3P3
AE9	GPIO_0_3P3
AE10	MDIO
AE11	I2CSEL
AE12	RESET_N
AE13	PHYADR2
AE14	SCK
AE15	VSS
AE16	MONCKN
AE17	MONCKP
AE18	VSS
AE19	VSS
A1	VSS

Appendix A Documentation References

For reference documentation, please visit www.inphi.com and log into your Inphi portal account for all Porrima-related product collateral.

Appendix B Order Information

Table 23 Ordering Information

Part #	Description
IN010C50-MD02-13GC-S03P	PAM-4 DSP for 400G Applications

Part # Qualifier	Description
IN010C50	IN = Inphi, 0 = Module, 1 = number of ports
MD	MD = 400G PAM
0	Speed grade for Line side interface 0 = Ethernet Grade
2	Process Node Qualifier
13	10 mm x 13 mm FCBGA Package
G	G = ROHS6 Package L = Lead-Free
C	C = Commercial Temperature
S03	Die Revision
P	P = Production Parts
No liability is assumed as a result of the use or application of this product. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No circuit patent licenses are implied. Contact Inphi Corporation's marketing department for the latest information regarding this product.	

Appendix C Contact Information

Inphi Corporation **2953 Bunker Hill Lane, Suite 300** **Santa Clara, CA 95054**	**Phone:(408) 217-7300** **Fax:(408) 217-7350** **E-Mail:**Products@Inphi.com
Visit us on the Internet at: http://www.inphi.com	

Appendix D Patent Notification

The Porrima 400G DSP product will be covered by one or more Inphi patents.

Appendix E Qualification Notification

The Porrima 400G DSP is fully qualified. Please contact Inphi for the qualification report.

For additional product and ordering information:

www.inphi.com