Mixed-Signal Products

UT30IBDAQ-16
16-Channel Sensor Data Acquisition Device with IntelliBus^{TM} Network Interface

Data Sheet
January 2013

FEATURES

- ❑ 16 Differential Resistive Bridge Sensor Input Channels
- ❑ External Temperature Sensor Input
- ❑ On-Chip Temperature Sensor
- ❑ 3V(max) Programmable Bridge Excitation
  - Optional Constant-Current Bridge Excitation
- ❑ Sigma-Delta ADC per channel
  - 16-Bit Resolution
  - Synchronous Data Collection
  - Input gain configurable (Av = 1, 5, 10 or 25)
  - Sample Rate Configurable to 5kSa/s
  - Dual 19-Word Input FIFO per Channel
- ❑ User-Programmable PLL (48 KHz to 24.576 MHz)
- ❑ SPI or I2C Peripheral Interface with 16-Word Input/Output FIFO
- ❑ IntelliBus Compliant Peripheral
  - Complies With Generation 3 Protocol
  - 7.5, 15 Or 30 Mb/s Data Rate
  - Internal Low-EMI MLVDS Transceiver
- ❑ 8KB RAM to Store EDS and Device Boot-Up
- ❑ External Serial Flash Interface
- ❑ Single 3.3V, Dual ± 1.50V or 1.65V Analog Supply
- ❑ Available For Commercial, Industrial and Automotive Temperature
- ❑ 145-pin FBGA (8 x 8 x 0.9mm)

APPLICATIONS

- ❑ Avionics
- ❑ Industrial Automation & Control
- ❑ Automotive Sensors
- ❑ Security
- ❑ HVAC
- ❑ Flight Test
- ❑ Ground Test

OVERVIEW

The UT30IBDAQ is a 16 channel Plug & Sense^{SM} IntelliBus peripheral compliant with Generation 3 IntelliBus protocols. The device supports synchronous analog-to-digital conversion of 16 differential analog sensors and communication via a multi-drop, multi-cast capable IntelliBus network. Sample rate is user programmable up to 5K samples per second with 16-bit resolution. The device also includes a configurable phase-locked loop (PLL) for clock generation and on-chip RAM for storing sensor calibration data and boot up instructions. An SPI/ I2C peripheral interface allows connection to additional ADCs or DACs and digital I/O are available for basic control and sense applications.

INTELLIBUS INTERFACE

The UT30IBDAQ-16 uses the IntelliBus network protocol. IntelliBus is a multi-drop, multicast serial data bus communication standard designed to network sensors, actuators, and subsystems while providing:

- the simplicity necessary for miniature smart sensors,
- the low latency needed for flight controls,
- the time determinism required for data analysis, and
- the distance required for industrial control.

IntelliBus permits the integration of signal conditioning, analog-to-digital conversion, and digital interfacing into a low-cost package that can be installed in any sensor, actuator, interface module, or system.

IntelliBus has a low overhead that enables maximum data transmittal, accommodates both sensors and actuators for monitoring and control, and incorporates fault avoidance features. Additionally, IntelliBus accommodates a high sensor count per bus (over 500), allows synchronization between multiple busses, simultaneous sampling capability, and isochronous transmission with low jitter (+/- 500ps). IntelliBus is time deterministic and enables high data rates per bus (30, 15, and 7.5 Mbps) while maintaining a low cost per node.

EXTERNAL SERIAL FLASH INTERFACE

The UT30IBDAQ-16 contains a boot up algorithm to support a unique ID and unique self-configuration per port, offloading the IntelliBus Network Interface Controller from configuring the smart sensors. This boot up data is stored in external flash memory, and downloaded at power-up into 8K words of internal RAM via a serial interface. Electronic Data Sheet information is also stored in the external flash and is available for access by the IntelliBus Network Interface Controller after the boot up procedure downloads the data to on board RAM. The flash interface is implemented as a standard SPI interface.

PERIPHERAL INTERFACE (PORTS)

The Channel 1 SPI/I2C port contains three FIFOs for buffering the data flow. A 16-word Output FIFO stores network data before transferring to the peripheral when the proper (optionally isochronous) IntelliBus command is decoded. A 16-word Input Buffer and a second 16-word Input FIFO are provided to allow isochronous data collection at peripheral data rates, with previous-frame data output to the IntelliBus network at IntelliBus data rates.

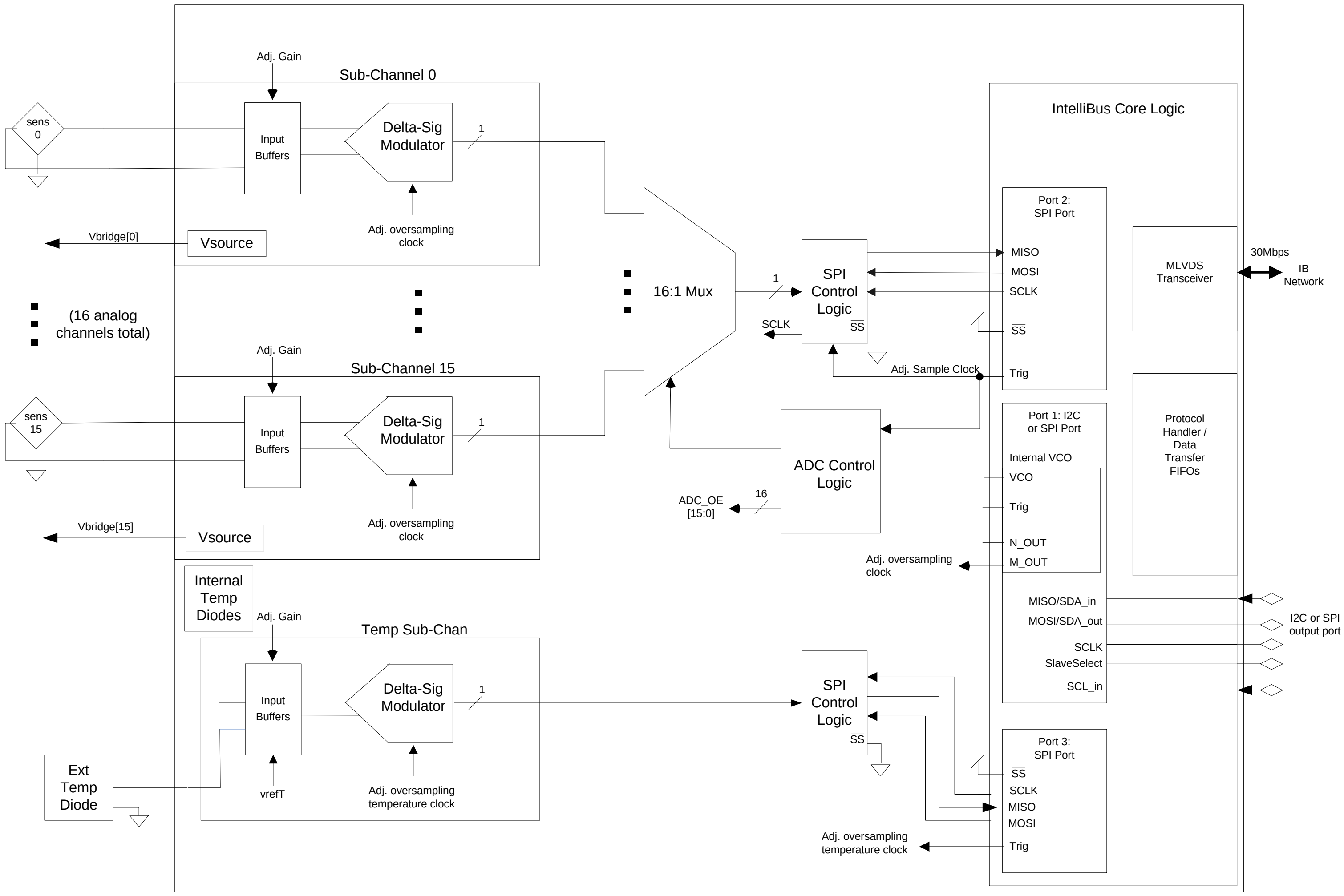
The PLL internal to the UT30IBDAQ provides peripheral clocking which is locked to the Trigger command.

DATA CONVERTERS

The UT30IBDAQ-16 contains 17 over-sampled sigma-delta analog to digital converters, all of which can be programmed to convert data synchronously (i.e. ADCs are not multiplexed). ADC sample rate is user programmable up to 5K. Gain control of the input amplifiers allows input voltage support up to $\pm$1.25V full scale. The converted sensor data for the first 16 channels is registered for transfer into the channel 2 FIFO, and then transferred onto the IntelliBus Network at data rates of up to 30Mbps. The 17^{th} ADC is used to sample an internal temperature sensor, an external temperature sensor or both, and is registered to transfer data to the channel 3 FIFO.

REMOTE ID INPUTS

The UT30IBDAQ contains support for ID inputs which can be read by the IntelliBus Network Interface Controller to determine the physical location of each device located on the bus. These ID inputs are discrete inputs externally tied to either V_{dd} or Ground.



Package Configuration

Pkg Pins	145
Package Type	FBGA
Package dimensions	8 mm X 8mm
Lead pitch	0.5 mm

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	TYP	MAX	UNITS

Voltage on AVdd, DVdd, AVdd3p3,DVdd3p3 Supplies relative to Gnd	0		3.8	V
Voltage on AVdd1p65 Supply relative to Gnd	0		1.9	V
Voltage on AVss1p65 Supply relative to Gnd	-1.9		0	V
Input voltage on digital signal I/O (note 1) relative to Gnd	– 0.5		5.5	V
Input voltage on DAQ signal I/O	AVss1p65 – 0.5		AVdd1p65 + 0.5	V
Input voltage on Vref	AVss1p65 – 0.5		AVdd1p65 + 0.5	V
Storage Temperature	-50		+140	^oC
Maximum Soldering Temperature			+220	^oC

Notes:

1: These voltages are with the Digital Power Supplies in their normal operating voltage range. Also, the clk_in pin is an exception, where range is –0.5 to 3.6V

2: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
ps	+1.65V Supply Voltage, Analog	+1.64	+1.65	+1.66	V	
ns	-1.65V Supply Voltage, Analog	-1.64	-1.65	-1.66	V	
AVdd3p3 DVddg	+3.3V Supply Voltage, Digital	3.0	3.3	3.6	V	
DVdd DVdd3p3	+3.3V Supply Voltage, Digital	3.0	3.3	3.6	V	
	Line/Load Regulation		±10		mV	
	Regulated Voltage Accuracy		±1.5		%	Note 3
	Power Supply Noise tolerance			200	mV	peak to peak, applies to DVDD3P3 and DVDD pins[1].
	Power Supply Ramp	0.2		50	mS	Note 1
	Case Temperature Range	0		72	°C	Note 4
	Vibration / Shock	N/R	N/R			
Vref	Vref Voltage	1.0	1.25	1.40	V	

Notes:

1. Guaranteed by design, not tested.
2. PWR Supply, Line/Load Regulation – Combined regulation maximum limits under all conditions.
3. PWR Supply, Regulated Voltage Accuracy – Nominal regulated voltage level deviation from PWR Supply Voltage.
4. Characterized, but not production tested. Note that the temperature range and unit accuracy/uncertainty does not guarantee that zero stability is maintained within this range –temperature characterization and correction in real time (on a host computer) using the on-board stored coefficients is recommended– these should be inclusive of all elements in the end product including the sensors. The thermal environment is expected to be stable or slowly changing (<1°C/minute), not a quickly changing thermal environment or thermal shock.

PERFORMANCE SPECIFICATIONS - ANALOG INPUTS & ADC

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS/ COMMENTS
Main Inputs					
Number of Channels		16			One ADC per Channel
Output Data Rate	7.8		4,400	Hz	Note 1
Resolution	16			Bits	Note 2
		≥60	≥60	dB	
Effective number of bits (Output					

Note:

1. Sample rate per channel – One A/D conversion will take place each sample. Sample rate is user controllable.
2. Resolution – The Sigma Delta A/D has 16 bits resolution for low speed operation with an over sample rate of 902 or or more, i.e. the Sigma Delta clock runs at 900*(Sample Rate). Also the input amplifier's noise floor can be much greater than 1LSB.
3. CMRR - The input amplifier's configuration must accommodate a Wheatstone bridge transducer interface, differential or single ended, source impedance and common mode voltage.
4. Non-Linearity – Maximum allowed deviation from a straight line defined as the least squares best fit. This deviation is intended to be corrected for in the host computer.
5. Comb. Offset & Gain Budget – This is the combined deviation budget for all amplifier and SDADC nominal and temperature induced offsets and gain deviations. These deviations are intended to be corrected for in the host computer.
6. Target only - Non-Temperature Drift, Offset – Any non-temperature induced offset drifts must be fairly stable over time as they will not be corrected for outside of the 6 month or 1 year calibration cycles. A given calibration cycle requires stability over a period twice as long in order to guarantee compliance and accuracy of the system during the time between calibration cycles.
7. Target only - Non-Temperature Drift, Gain/Scale - Any non-temperature induced gain or scale drifts must be fairly stable over time as they will not be corrected for outside of the 6 month or 1 year calibration cycles. A given calibration cycle requires stability over a period twice as long in order to guarantee compliance and accuracy of the system.
8. Output Referred Noise – This is the maximum allowed noise developed by the amplifier and downstream conditioning through the SDADC.
9. Anti Alias filter – Anti-alias filtering of out of bandwidth signals is required in sampled systems. All pre-Sigma-Delta filtering will be provided by off-chip filters. Sigma-Delta anti-aliasing due to decimation shall be provided by the internal Sinc3 filter, all other filtering shall be provided by the user off-chip.
10. Signal Desired Bandwidth – The amplifier preceding the SDADC will be designed to have at least the bandwidth of the signal requirements.
11. SDADC Input Signal Range – (At vcom = 0v) The input range represents the total possible input range over all transducer variations. This includes signal swings and offsets over the full temperature range. The gain of the input amplifier will be designed to use the full scale of the A/D converter's range less any thermal or offset variation of the preamp or sdadc RTO. The SDADC differential signal input range is set by the Vref voltage.
12. Signal Common Mode Voltage – DC voltage common to both differential amplifier inputs. While instrumentation signals can have significant AC CM content, usually at 60Hz, the applications here are limited to configurations where either the coupling is controlled through shielding (pressure scanner with close-coupled, shielded sensors), or eliminated by off-chip instrumentation amplifiers.

13. Signal Source Impedance - The input amplifier's configuration must accommodate a range of impediance including a 5Kohm Wheatstone bridge transducer interface differential source impedanceand associated common mode voltage, as well as a low impedance sources including differential or single ended.
14. Number of internal main temperature channels per ASIC assuming all temperature channels are multiplexed to one amplifier and sigma delta ADC.
15. Chips per Bus - Number of ASICs that may be connected to the same bus. The network data rates for the system depend on the number of chips sharing the bus.
16. Bus Speed - Determines intended IntelliBus bus speed and transceiver/clock option.
17. Power Dissipation – The required power for most of the immediate applications is not limited. However, due to the small size of the required package, it is desired that the chip not overheat while mounted to a circuit board which is lying on a desktop surface in a normal laboratory ambient environment. Future applications may derive power from batteries or from energy-harvesting sources which are typically power/weight limited, so minimizing the power consumption becomes a secondary desire if it can be easily accommodated through selection of technologies or through minimal impact to other requirements.
18. Flash Memory – 16 KB and functionality shall be provided on the ASIC for communication (read/write) of the EDS (Electronic Data Sheet) to and from the host computer from a separate SSI flash memory chip. In addition, ASIC functionality shall be provided to select specific configuration values from the EDS data set to perform ASIC boot configuration of on-chip functions and configuration of off-chip devices.
19. Number of Ports & Type – Such as SPI and I2C for communication and control off off-chip devices
20. Gain settings should be designed to encompass temperature signals over the dynamic range. Nominal scale factor is 2mV/°C. Guaranteed by design, not tested.
21. Not including Vref drift.
22. Gains with buffered Anti-Aliasing Filter enabled; 1, 5, 10 and 25 with filter disabled.
23. Common mode < ±0.1V. Enable/Disable capability. 0V = Disabled.

DC ELECTRICAL HARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
QI_{dd_dig}	Quiescent DV_{dd} Supply Current			3	mA	Floating outputs, no clock, DVdd = 3.6V
AI_{dd_dig1}	Active DV_{dd} Supply Current (100 Hz sampling, 16 subchnnl + 1 temp subchnnl)	12	15	25	mA	DVdd = 3.6V[4]
AI_{dd_dig2}	Active DV_{dd} Supply Current (4.4KHz sampling, 3 subchnnls + 1 temp subchnl)	13	16	26	mA	DVdd = 3.6V[4]
QI_{dd_an}	Quiescent AV_{dd} Supply Current			1	mA	Floating outputs, no clock, Avdd = 3.6V
AI_{dd_an}	Active AV_{dd} Supply Current		7	9	mA	Avdd = 3.6V
$QI_{dd\_anp1p65}$	Quiescent $+AV_{dd1p65}$ Supply Current		70		mA	
$AI_{dd\_anp1p65}$	Active $+AV_{dd1p65}$ Supply Current		75		mA	
$QI_{dd\_ann1p65}$	Quiescent $-AV_{dd1p65}$ Supply Current		70		mA	
$AI_{dd\_ann1p65}$	Active $-AV_{dd1p65}$ Supply Current		75		mA	
V_{IL}	Input Low (logic 0) Voltage	-0.5[2]		0.8	V	CMOS Input, LVTTL Input
V_{IH}	Input High (logic 1) Voltage	2.0		5.5[2]	V	CMOS Input, LVTTL Input
V_{HYS}	Hysteresis of Schmitt trigger inputs	190		300	mV	Only on pins notes as "Schmitt trigger"
I_{IL}	Input Low Current	-5		5	uA	Vin = 0V, Vdd = 3.6V
I_{IH}	Input High Current	-5		5	uA	Vin = $V_{dd,}$ Vdd = 3.6V
C_{IN}	Input Capacitance			10	pF	Input only pins[2]
R_{PD}	Pull Down Resistor	38		121	uA	Vin = V_{dd} , only on pins noted as "pulldown"[2]
R_{PU}	Pull Up Resistor	48		114	uA	Vin = Vss , only on pins noted as "pullup"[2]
C_{IO}	Bidirect Capacitance of pin			10	pF	Bidirect pins[2]
C_{OUT}	Output Capacitance of pin			10	pF	Output only pins[2]
C_{load}	Output Capacitive Drive			25	pF	Except pins in C_{VCO} pin.[1]
C_{VCO}	VCO Output Drive Capacitance			85	pF	Applies to pll_vco_out_m_in, pll_m_out, pll_n_out[1]
V_{OL}	Output Low (logic 1) Voltage			0.4	V	I_{OL} = -2 mA[3]
V_{OH}	Output High (logic 1) Voltage	2.4			V	I_{OH} = 2 mA[3]
V_{CLKINL}	clk_in Low voltage	-0.5[2]		0.8	V	when crystal is not used
V_{CLKINH}	clk_in High voltage	2.0		3.6[1]	V	when crystal is not used

Note:

1. Guaranteed by design, not tested.
2. Characterized, but not production tested.
3. I_{OL} and I_{OH} will be 16mA for pins listed under C_{VCO}
4. Min condition: no output loads, average current. Typ condition: outputs loaded, average current. Max condition: outputs loaded, peak currents.
5. Vdd = 3.0V to 3.6V, Testing Temp = 25°C, unless otherwise noted. These characteristics apply to all pins except the pll_ph_det_out and pll_vco_in which are analog signaling pins.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
$t_{CLKSTRT}$	Estimated Crystal Start Time			15	ms	3.3 vdc, crystal dependent[3]
$t_{CLKLOCK}$	Core Clock Lock Time			300	us	excluding crystal stability time[2]
t_{CONFIG}	Logic Configuration Time (4)			20	ms	Min = 2 chan, Max = 9 chan[1]
$f_{CLKINOSC}$	Input Clock frequency (CMOS osc)		12		MHz	when crystal is not used[2,5]
f_{CLKIN}	Input Clock frequency (crystal)		12		MHz	Notes 2 and 5
t_{CCJITT}	Input Clock Cycle-Cycle Jitter			TBD[10]	ps	when crystal is not used[1,7]
t_{CPJITT}	Input Clock Period Jitter			TBD[10]	ns	When crystal is not used[1,7]
t_{CDRIFT}	Input Clock Period Drift			TBD[10]	ps	when crystal is not used[1,7]
t_{CLKTOL}	Input Clock Tolerance			TBD[10]	%	When crystal is not used[1,7]
t_{RESET_OUT}	Reset Output pulse width	30			ns	Note 1
t_{RESET_IN}	reset_n active following valid power inputs	150			us	NDI device requires a minimum application of an active reset_n following power up.
f_{NTWK}	Network Input/Output Bit Rate	7.5		30	MBps	Valid Speeds are 7.5, 15, and 30 Mbps[1]
	Network Input frequency tolerance	-10		+10	%	Note 6
t_{Iodcd1}	Tx, TxE Duty Cycle Distortion due to I/O			200	ps	pulse skew, at 15pf load, targeted for 30Mbps applications[1]
t_{Iodcd2}	Tx, TxE Duty Cycle Distortion due to I/O			300	ps	pulse skew, at 20pf load, targeted for 15Mbps applications[1]
t_{TW}	Trig_pulse/sync_pulse Pulse Width	225			ns	Either high pulse or low pulse[2]
t_{RXTRIG}	Prop delay, RX to combinatorial output			9	ns	trigger and sync outputs, measured at 50% of Voh[8]

Note:

1. Guaranteed by design, not tested.
2. Characterized, but not production tested.
3. Not tested.
4. The time assumes that boot memory is properly configured and no boot schedule is being executed.
5. 6MHz input is a design goal for evaluation of a 40Mbps data rate. Input frequency is to be characterized starting at 6 MHz up to the highest operational frequency.
6. Design Goal only, not production tested.
7. To be determined during design phase.
8. Scaling of this spec, based on simulation results, will be required to determine tester limits, due to larger capacitive loading on the tester.
9. Vdd = 3.0V to 3.6V, Testing Temp = 25°C, unless otherwise noted.
10. Input clock requirements will be identified during characterization tests. A requirement for very low period jitter is anticipated.

TRIGGER-BASED PLL CLOCK MULTIPLIER CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
f_{MULT}	PLL Multiplier	1		2048		Tested at 512 for Range 3, 1024 for Range 2, and 1344 for Range 0[4].
f_{SOURCE}	PLL Signal Source Range	1		48	KHz	Note 4
ti_{CCJIT}	Source Input Cycle to Cycle Jitter			±15	nS	Note 2
Ti_{PERJIT}	Source Input Period Jitter			±15	nS	Note 2
f_{VCO}	PLL VCO Out Range (Internal)	2		25	MHz	Note 4
f_{VCO_DUTY}	VCO Output Duty Cycle	40	50	60	%	Note 2
to_{CCJIT}	VCO Output Cycle to Cycle Jitter			$ti_{CCJIT} \pm 2$	nS	Note 2
to_{PERJIT}	VCO Output Period Jitter			$Ti_{PERJIT} \pm 3$	nS	Note 2. For all PLL ranges
t_{LOCK}	PLL Lock Time			1	S	Notes 2 and 4
t_{PH_OFFSET}	ch1_trig_pulse to vco/mout/nout phase offset			10	ns	

Notes:
1. Guaranteed by design, not tested.
2. Characterized, but not production tested.
3. This time is dependent on the loop filter characteristics and the source frequency.
4. The PLL is guaranteed to operate in the ranges shown in and . The PLL multiplier may operate outside of the specified minimum and maximum ranges.

TRIGGER-BASED PLL MULTIPLIER IMPLEMENTATION DETAILS

The following table illustrates some example implementations using the internal VCO.

Evaluated Trigger-Based PLL Multiplier Settings

Config Number	Trigger (KHz)	VCO Out (MHz)	M Out (MHz)	N Out (MHz)	Mux Select	Range Select	M Divider Value[1]	N Divider Value[1]
1	1.6	2.1504	0.0016		M	0	1344	na
2	1	2.048	0.001		M	0	2048	na
3	5	5.12	0.005		M	1	1024	na
4	10	10.24	0.01		M	2	1024	na
5	48	12.288	1.536	0.048	N	2	8	32
6	48	18.432	2.304	0.048	N	3	8	48
7	48	24.576	3.072	0.048	N	3	8	64
8	41.664	21.332	0.041664		M	3	512	na
9	2	2.208	.92	.002	N	0	24	46
10	5	5.12	5.12	.002	N	1	1	1024

Device Level Signals – Total Pin Qty = 18

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
Clock								
clk_in	clk_in		In	In	In	Master clock or oscillator input pin 1 (6 or 8 MHz)	6 MHz, analog input	D10
Xtal1	Xtal1		-	i/o	i/o	Oscillator input pin 2		B10
reset_n	reset_n		In	In	In	Master reset signal input, logic 0 places NDI in reset	quasi-static, schmitt trig	K9
baud_clk	baud_clk		In	In	In	Input clock for spare URAT port	Schmitt Trigger	G8
IntelliBus Network Interface								
ib_network_in	ib_network_in		In	In	In	IntelliBus Network input	schmitt trigger	E11
ib_network_out	ib_network_out		Out	Out	Out	IntelliBus Network output		D14
xmit_driver_en	xmit_driver_en		Out	Out	Out	IntelliBus Network transmitter enable , logic 1 enables transceiver		H8
ib_a			An	An	An	MLVDS out A		E12
ib_b			An	An	An	MLVDS in B		E14
mlvds_en			In	in	in	Enables internal MLVDS xcvr		C12
Configuration/ Control I/O								
bit_rate_sel_0	bit_rate_sel_0	press_spi_ce_n[5]	In	In	In	Bit rate selection code bit 0	static	B6
bit_rate_sel_1	bit_rate_sel_1	temp_spi_ce_n[5]	In	In	In	Bit rate selection code bit 1	static	C8
secure_mem_jmp	secure_mem_jmp		In	In	In	Secure memory protection. Must be grounded for normal operation. When grounded this signal prevents writes to memory locations 0 to 7. When brought high (logic 1) memory locations 0 to 7 can be written and the device will respond to any logical address.	static, pulldown	B14

Device Level Signals – Total Pin Qty = 18 (Cont'd)

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
nvm_wr_en_hw	nvm_wr_en_hw	Test_sel_2[1,3] serial_out_sel[5]	In	In	In	Non-volatile memory protection. Inhibits when low (logic 0) writes to the entire non-volatile memory space. This pin will override memory protection registers. serial_out_sel = 0—temp data on sinc3_tm_out & press data on onebit_tm_out. Opposite when serial_out_sel = 1.	static, pulldown	A13
boot_complete	boot_complete		Out	Out	Out	Boot Operation complete status, logic 1 indicates operation complete	quasi-static	D12
reset_out_n	reset_out_n		Out	Out	Out	Reset out to be used by peripheral logic, logic 0 indicates a reset	30 ns pulse	D13
Test Mode En 0	test_mode_en_0	nand_out[4]	-	i/o	i/o	Reserved. Must be grounded for normal operation.	static, pulldn, schmitt trigger	L8
Test Mode En 1	test_mode_en_1	scan_out_c1[3]	-	i/o	i/o	Reserved. Must be grounded for normal operation.	static, pulldn, schmitt trigger	H7

Device Level Signals - Total Pin Qty = 16

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
NDI Non-volatile Serial Memory Interface								
ext_mem_sdo	ext_mem_sdo	rb_patt(1)	out	out	out	Serial data out		H11
ext_mem_sdi	ext_mem_sdi	rb_debug_sdo_en/ nvm_downld_dis_n	in	in	in	Serial data in	pullup	J9
ext_mem_sclk	ext_mem_sclk	rb_patt(0)	out	out	out	Serial clock		K10
ext_mem_cs_n	ext_mem_cs_n	rb_patt(2)	out	out	out	Serial nvm chip select, active low		J10

Pin Name	Signal Name: Normal	Signal Name: Test Modes	Signal Direction (An=analog): Core port	Signal Direction (An=analog): Tst md	Signal Direction (An=analog): I/O cell	Description	Characteristics	Pkg Pin #
Programmable Trigger Clock Multiplier PLL Interface – Channel 1 Controlled. See Section								
v1p8_reg_dig_out	v1p8_reg_dig_out		-	An	An	Digital Core 1.8 volt regulator output. Must be connected to grounded output capacitor. Not for other uses.	tie to decoupl cap, for digital core	A12
vddgpll	vddgpll		-	An	An	Core PLL Digital 1.8 volt regulator output. Must be connected to grounded output capacitor. Not for other uses.	tie to decouping cap for core PLL	A9
v1p8_reg_an_out	v1p8_reg_an_out		-	An	An	Digital Core 1.8 volt regulator output. Must be connected to grounded decoupling capacitor, C1. Not for other uses.	tie to decoupling cap, for core PLL analog V	B8
agnd	agnd		-	An	An	Analog ground for Trigger PLL and Analog Regulator.		C7
EXT_RBIAS	EXT_RBIAS		-	An	An	Bias resistor for PLL reference current		A6
AVDD3P3	avdd3p3		An	An	An	Analog 3.3 vdc (3.6 vdc max) supply for Trigger PLL and Analog Regulator.	3.3V (3.6V max) for Trig PLL	A8, B12
agndgpll	agndgpll		An	An	An	Analog ground for core PLL and Analog Regulator – connected to agnd in chip package.	Gnd for Trig PLL	-
chrgpmp_out	chrgpmp_out		-	An	An	Trigger PLL charge pump output signal ranging from 1.0 - 2.3 volts. This signal is tied to the input of an external passive 2nd-order low-pass filter. When an external VCO is used this output is tied to both the external low-pass filter, and the external VCO input.	Analog voltage source, ~1.5-2.0V	A7
pll_vco_out_m_in			-	i/o	i/o	Trigger PLL Internal VCO output (PLL output), or External VCO input.	Reference C_{VCO} in	F12

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
pll_m_out	pll_m_out		-	Out	Out	Trigger PLL Frequency Division output through an internal “m” programmable divider.	Reference C_{VCO} in	F10
pll_n_out	pll_n_out		-	Out	Out	Trigger PLL Frequency Division output through internal “m” and “n” programmable dividers.	Reference C_{VCO} in	F14
mult_lock_detect	mult_lock_detect	scan_out_ch2[3]	out	Out	Out	Trigger PLL lock indicator (lock is logic 1)		D7
VSSGPLL	vssgpll		An	An	An	Core PLL Digital Ground	Gnd for core PLL digital V	C10
dvddg	dvddg		An	An	An	Core PLL 3.3 VDC (3.6 VDC max) supply – connected to DVDD plane in chip package	3.3V (3.6V max) for core PLL	-

Device Level Signals - Total Pin Qty = 8

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
Remote ID								
remote_ID(0)	remote_id_0	core_lock_detect [1]	i/o	out	i/o		pullup	M7
remote_ID(1)	remote_ id_[1]	rb_parallel_dr	in	in	in		pullup	N11
remote_ID(2)	remote_ id_[2]	scan_en[3]	in	in	in		pullup	P8
remote_ID(3)	remote_ id_[3]	scan_in_ch2[3]/ adc_trig_press[5]	in	in	in		pullup	N9
remote_ID(4)	remote_ id_msnib[4]		i/o	in	i/o		pullup	M10
remote_ID(5)	remote_ id_msnib[5]		i/o	in	i/o		pullup	M9
remote_ID(6)	remote_ id_msnib[6]		i/o	in	i/o		pullup	L10
remote_ID(7)	remote_ id_msnib[7]		i/o	in	i/o		pullup	M8

Device Level Signals - Total Pin Qty = 16

Pin Name	Signal Name		Signal Direction (An=analog)					
	Normal	Test Modes	Core port	Tst md	I/O cell	Description	Characteristics	Pkg Pin #
Channel 1 (SPI/ I2C) Signals								
ch1_mosi_sdao	ch1_mosi_sdao		i/o	-	i/o		slew rate limited	N13
ch1_miso_sdai	ch1_miso_sdai		i/o	-	i/o			P11
ch1_data_valid	ch1_data_valid		i/o	-	i/o			N14
ch1_ss_sclo	ch1_ss_sclo	adc_trig_temp[5]	i/o	-	i/o		slew rate limited	M12
ch1_sclk_scli	ch1_sclk_scli	adc_scan_out[5]	i/o	-	i/o		adc_scan_out is connected to register srv_remoteid_sel_i_reg_15_	M11
ch1_slave_mode_en	ch1_slave_mode_en	scan_in_c1[3]	in	-	in		Static	M14
ch1_io_port_sel	ch1_io_port_sel	mbrun	in	-	in		Static	L14
ch1_trig_pulse	ch1_trig_pulse	clk_1x_pll_tst	out	out	out			K12
ch1_sync_pulse	ch1_sync_pulse	clk_fx_pll_tst [1]	out	out	out			K11
ch1_sleep_mode_out	ch1_sleep_mode_en	rb_error[3]	out	-	out		quasi-static	J13
ch1_srvc_flags_1		rb_done[3]	out		out			E9
ch1_srvc_flags_2		rb_pause[3]	out		out			E10
ch1_srvc_flags_3		rb_debug_so[3]	out		out			C14
ch1_srvc_flags_4			out		out			F9
ch1_srvc_flags_5			out		out			-
ch1_srvc_flags_6			out		out			-
ch1_srvc_flags_7			out		out			-
ch1_srvc_flags_8			out		out			-
ch1_ext_flags_0	ch1_ext_flags_0	test_sel_1	in	in	in			L12
ch1_ext_flags_1	ch1_ext_flags_1	test_sel_0	in	in	in			K14

Notes:

1. When active, test mode signals are indicated by superscript numbers. All non-specified numbers will map the Normal mode onto the pin to allow functional testing:

   [1] Analog Test Mode [2] Functional Test Mode [3] Scan Test Mode [4] NAND Tree Mode [5] ADC Test Mode

2. Some Channel 1 pins may have an alternate function selected by ch1_io_port_sel. Primary and alternate functions for these ch1 pins are identified in the following table.
3. These 4 pins are shared with Remote_ID(7:4) pins

Device Level Signals - Total Pin Qty = 16

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
DAQ – Constant Current Signals								
ibridge_pad[0]					O	Channel 0 constant current output		P1
ibridge_pad[1]					O	Channel 1 constant current output		N1
ibridge_pad[2]					O	Channel 2 constant current output		M1
ibridge_pad[3]					O	Channel 3 constant current output		L1
ibridge_pad[4]					O	Channel 4 constant current output		K1
ibridge_pad[5]					O	Channel 5 constant current output		J1
ibridge_pad[6]					O	Channel 6 constant current output		H1
ibridge_pad[7]					O	Channel 7 constant current output		F6
ibridge_pad[8]					O	Channel 8 constant current output		E6
ibridge_pad[9]					O	Channel 9 constant current output		C6
ibridge_pad[10]					O	Channel 10 constant current output		C5
ibridge_pad[11]					O	Channel 11 constant current output		E1
ibridge_pad[12]					O	Channel 12 constant current output		D1
ibridge_pad[13]					O	Channel 13 constant current output		C1
ibridge_pad(14]					O	Channel 14 constant current output		B1
ibridge_pad[15]					O	Channel 15 constant current output		A1

Device Level Signals - Total Pin Qty = 37

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
DAQ – Analog I/O Signals								
vip_pad[0]					I	Channel 0 input high		P2
vim_pad[0]						Channel 0 input low		P3
vip_pad[1]						Channel 1 input high		N3
vim_pad[1]						Channel 1 input low		M4
vip_pad[2]						Channel 2 input high		M2
vim_pad[2]						Channel 2 input low		M3
vip_pad[3]						Channel 3 input high		L3
vim_pad[3]						Channel 3 input low		L5
vip_pad[4]						Channel 4 input high		K3
vim_pad[4]						Channel 4 input low		K4
vip_pad[5]						Channel 5 input high		K5
vim_pad[5]						Channel 5 input low		J6
vip_pad[6]						Channel 6 input high		M6
vim_pad[6]						Channel 6 input low		K6
vip_pad[7]						Channel 7 input high		J3
vim_pad[7]						Channel 7 input low		J5
vip_pad[8]						Channel 8 input high		G2
vim_pad[8]						Channel 8 input low		G1
vip_pad[9]						Channel 9 input high		F3
vim_pad[9]						Channel 9 input low		G3
vip_pad[10]						Channel 10 input high		E4
vim_pad[10]						Channel 10 input low		E5
vip_pad[11]						Channel 11 input high		E2
vim_pad[11]						Channel 11 input low		E3
vip_pad[12]						Channel 12 input high		D3
vim_pad[12]						Channel 12 input low		D5
vip_pad[13]						Channel 13 input high		C2
vim_pad[13]						Channel 13 input low		C3
vip_pad[14]						Channel 14 input high		B3
vim_pad[14]						Channel 14 input low		C4
vip_pad[15]						Channel 15 input high		A2
vim_pad[15]						Channel 15 input low		A3
vref_pad						SDADC Reference – internally set to either vcom or to this external pad		B5, P6
vrefTcm_pad						Reference level for temperature conversion. It should be a common mode level of an applicable pressure sensor bridge – internally set to either vcom or to this external pad		G4

Device Level Signals - Total Pin Qty = 37 (Cont'd)

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
DAQ – Analog I/O Signals - Continued								
vrefTdi_pad						voltage reference for temp conversion using internal or external diode – internally set to either vcom or to this external pad		H4
vcomT_pad						vcom for temp sensor – connected to vcom plane in chip package		-
vcom_temp_pad						vcom for internal temp sensor – uses same die pad as vcomT_Pad		-
ext_diode_pad						Ext temp diode pin		H3

Device Level Signals - Total Pin Qty = 6

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
Analog Section Test Pins								
onebit_tm_out						Test pin, 900-bit serial output of the temperature-selected subchannel's delta-sigma		G12
sinc3_tm_out						Test pin, 16-bit serial output from the temperature-selected subchannel's sinc3 filter		G13
Vctemp_pad						Test signal; muxed temp sense		F5
Itest_pad						test pin to bring out a reference current (I could live without this one if we are hurting for pins)		N5
vanaoutp_pad						test pin to bring out the positive side of the pre-amp (v01 on schematics) - of the selected channel - test mode only (tm1)		P5
vanaoutm_pad						test pin to bring out the negative side of the pre-amp (v01 on schematics) - of the selected channel - test mode only (tm1)		P4

Device Level Signals - Total Pin Qty = 28

Pin Name	Signal Name		Signal Direction (An=analog)			Description	Characteristics	Pkg Pin #
	Normal	Test Modes	Core port	Tst md	I/O cell			
Power Supply								
DVDD			-	An	An	3.3 volt input power (io cells)	6 Pins	A14, D8, G14, J12, P12, P9
DVSS			-	An	An	power ground (io cells)	6 Pins	A10, G11, H12, J14, P10, P13
DVDD3P3			-	An	An	3.3V input power (digital core)	2 Pins	A11, C11
vss			-	An	An	Power ground (digital core)	5 Pins	G7, H14, L7, L13, P14
PS	ps			An	An	+1.65 Volt power supply (analog inputs)	2 Pins	P7, A4
vcom	vcom			An	An	Power ground (analog inputs)	4 Pins	A5, F1, J2, M5
NS	ns			An	An	-1.65 Volt power supply (analog inputs)	2 Pins	N7, B4

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping

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