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SEE HS-65647RH

HS-83C55RH

September 1997

Radiation Hardened 16K Bit CMOS ROM

Features

- **Radiation Hardened EPI-CMOS**
  - **Total Dose 1 x 10^5 RAD(Si)**
  - **Transient Upset > 1 x 10^8 RAD(Si)/s (Ports and DDR)**
  - **Latch-Up Free > 1 x 10^{12} RAD(Si)/s**
- **2048 Words x 8 Bits ROM**
- **Electrically Equivalent to Sandia SA3002**
- **Pin Compatible with Intel 8355**
- **Bus Compatible with HS-80C85RH**
- **Single 5 Volt Power Supply**
- **Low Standby Current 100μA Max**
- **Low Operating Current 2mA/MHz**
- **Completely Static Design**
- **Internal Address Latches**
- **Two General Purpose 8-Bit I/O Ports**
- **Multiplexed Address and Data Bus**
- **Self Aligned Junction Isolated (SAJI) Process**
- **Military Temperature Range -55°C to +125°C**

Description

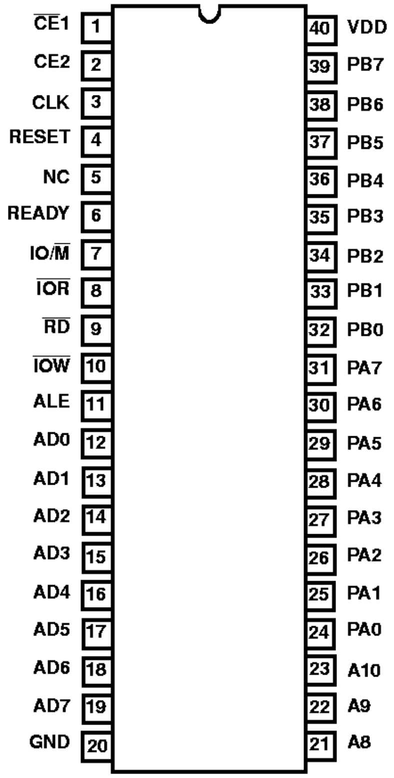
The HS-83C55RH is a radiation hardened ROM and I/O chip fabricated using the Harris radiation hardened Self-Aligned Junction Isolated (SAJI) silicon gate technology. Latch-up free operation is achieved by the use of epitaxial starting material to eliminate the parasitic SCR effect seen in conventional bulk CMOS devices.

The HS-83C55RH is intended for use with the HS-80C85RH radiation hardened microprocessor system.

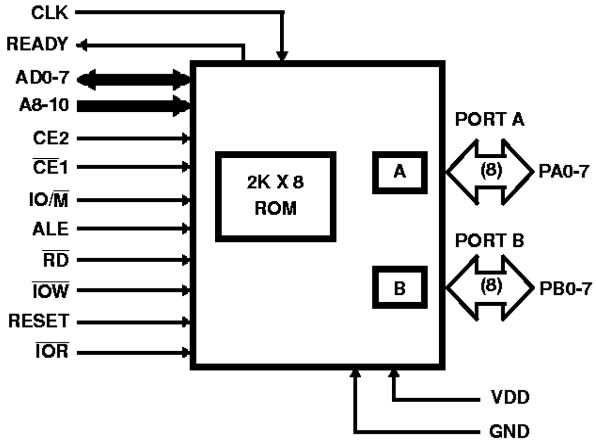
The ROM portion is designed as 16,384 mask programmable cells organized in a 2048 word x 8-bit format. A maximum post irradiation access time of 340ns allows the HS-83C55RH to be used with the HS-80C85RH CPU without any wait states. This ROM is designed for operation utilizing a single 5 volt power supply.

Pinout

HS-83C55RH 40 LEAD BRAZE SEAL DIP COMPLIANT OUTLINE D5, CONFIGURATION 3
TOP VIEW



Block Diagram



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
ALE	11	I	Address Latch Enable: When high, AD0-7, IO/$\overline{\text{M}}$, A8-0, CE2, and $\overline{\text{CE}}$1, enter the address latches. The signals (AD, IO/$\overline{\text{M}}$, A8-10, CE2, CE1) are latched in at the trailing edge of ALE.*
AD0-7	12-19	I	Address/Data Bus (Bidirectional): The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD0. If $\overline{\text{RD}}$ or $\overline{\text{IOR}}$ is low when the latched chip enables are active, the output buffers present data on the bus.
A8-10	21, 22, 23	I	Address Bus: High order bits of the ROM address. They do not affect I/O operations.
$\overline{\text{CE}}$1,CE2	1, 2	I	Chip Enable Inputs: $\overline{\text{CE}}$1 is active low and CE2 is active high.The HS-83C55RH can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them In. If either Chip Enable input is not active, the AD0-7 and READY outputs will be in a high impedance state.
IO/$\overline{\text{M}}$	7	I	I/O Memory: If the latched IO/$\overline{\text{M}}$ is high when $\overline{\text{RD}}$ Is low, the output data comes from an I/O port. If it is low, the output data comes from the ROM.
$\overline{\text{RD}}$	9	I	Read: If the latched Chip Enables are active when $\overline{\text{RD}}$ goes low, the AD0-7 output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{\text{RD}}$ and $\overline{\text{IOR}}$ are high, the AD0-7 output buffers are 3-stated.
$\overline{\text{IOW}}$	10	I	I/O Write: If the latched Chip Enables are active, a low on $\overline{\text{IOW}}$ causes the output port pointed to by the latched value of AD0 to be written with the data on AD0-7. The state of IO/$\overline{\text{M}}$ is ignored.
CLK	3	I	Clock: Used to force the READY into its high impedance state after it has been forced low by $\overline{\text{CE}}$1, low, CE2 high and ALE high.
READY	6	O	READY: A 3-state output controlled by $\overline{\text{CE}}$1, CE2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK.
PA0-7	24-31	I/O	Port A: General purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{\text{IOW}}$ is low and a 0 was previously latched from AD0, AD1. Read operation is selected by either $\overline{\text{IOR}}$ low and active Chip Enables and AD0 and AD1 low, or IO/$\overline{\text{M}}$ high, RD low, active chip enables, and AD0 and AD1, LOW.
PB0-7	32-39	I/O	Port B: This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD0 and a 0 from AD1.
RESET	4	I	Reset: An input high causes all pins in Port A and B to assume input-mode. (Clear DDR Register.)
$\overline{\text{IOR}}$	8	I	I/O Read: When the Chip Enables are active, a low on $\overline{\text{IOR}}$ will output the selected I/O port onto the AD bus. $\overline{\text{IOR}}$ low performs the same function as the combination IO/$\overline{\text{M}}$ high and $\overline{\text{RD}}$ low. When $\overline{\text{IOR}}$ is not used in a system, $\overline{\text{IOR}}$ should be tied to VCC.
VDD	40	I	Voltage: +5 Volt
GND	20	I	Ground: Ground Reference.

* ALE must be clocked once after power up.

Absolute Maximum Ratings

Supply Voltage . . . . +7.0V
Input, Output or I/O Voltage . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +175°C
Lead Temperature (Soldering 10s) . . . . +300°C
Typical Derating Factor . . . . 1.5mA/MHz Increase in IDDOP
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	25.8°C/W	9.9°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 1.94W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +4.75V to +5.25V
Operating Temperature Range . . . . -55°C to +125°C
Input Low Voltage . . . . 0V to +0.8V
Input High Voltage . . . . VDD -0.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

All Devices are Guaranteed at Worst Case Limits and Over Radiation. Dynamic Current is Proportional to Operating Frequency.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current	IIH	VDD = 5.25V, VIN = 0V Pin Under Test = VDD	1, 2, 3	-55°C, +25°C, or +125°C	-	1.0	µA
	IIL	VDD = 5.25V, VIN = 5.25V Pin Under Test = 0V	1, 2, 3	-55°C, +25°C, or +125°C	-1.0	-	µA
High Level Output Voltage	VOH	VDD = 4.75V, IOH = -2.0mA	1, 2, 3	-55°C, +25°C, or +125°C	4.25	-	V
Low Level Output Voltage	VOL	VDD = 5.25V, IOL = 2.0mA,	1, 2, 3	-55°C, +25°C, or +125°C	-	0.5	V
Output Leakage Current	IOZL	VDD = 5.25V, VIN = 0V	1, 2, 3	-55°C, +25°C, or +125°C	-10	-	µA
	IOZH	VDD = 5.25V, VIN = 5.25V	1, 2, 3	-55°C, +25°C, or +125°C	-	10	µA
Static Current	IDDSB	VDD = 5.25V	1, 2, 3	-55°C, +25°C, or +125°C	-	100	µA
Dynamic Current	IDDOP	VDD = 5.25V, f = 1MHz	1, 2, 3	-55°C, +25°C, or +125°C	-	5.0	mA/MHz
Functional Tests	FT	VDD = 4.75V and 5.25V, VIH = VDD - 0.5, VIL = 0.8V	7, 8A, 8B	-55°C, +25°C, or +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Data Bus Float After Read	TRDF	9, 10, 11	-55°C, +25°C, +125°C	0	110	ns
Read Control to Data Bus Enable	TRDE	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Clock Pulse Width Low	T1	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
Clock Pulse Width High	T2	9, 10, 11	-55°C, +25°C, +125°C	70	-	ns
Clock Rise and Fall Times	TR, TF	9, 10, 11	-55°C, +25°C, +125°C	-	100	ns
Address to Latch Setup Time	TAL	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Address Hold Time After Latch	TLA	9, 10, 11	-55°C, +25°C, +125°C	60	-	ns
Latch to Read/Write Control	TLC	9, 10, 11	-55°C, +25°C, +125°C	140	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC Tests are Guaranteed Through Functional Testing with the Clock Period Equal to 500ns. TRDE + TRDF are the Only Read and Record Parameters. Output Timings are Measured with a Capacitive Load CL = 170pF, VIH = 4.25, and VIL = 0.8V

PARAMETERS	SYMBOL	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Valid Out Delay from Read Control (Note 1)	TRD	9, 10, 11	-55°C, +25°C, +125°C	-	140	ns
Address Stable to Data Out Valid (Note 2)	TAD	9, 10, 11	-55°C, +25°C, +125°C	-	340	ns
Latch Enable Width	TLL	9, 10, 11	-55°C, +25°C, +125°C	120	-	ns
Read/Write Control of Latch Enable	TCL	9, 10, 11	-55°C, +25°C, +125°C	40	-	ns
Read/Write Control Width	TCC	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
Data In to Write Setup Time	TDW	9, 10, 11	-55°C, +25°C, +125°C	150	-	ns
Data In Hold Time After Write	TWD	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Write to Port Output	TWP	9, 10, 11	-55°C, +25°C, +125°C	-	300	ns
Port Input Setup Time	TPR	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Port Input Hold Time	TRP	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
Ready Hold Time	TRYH	9, 10, 11	-55°C, +25°C, +125°C	0	160	ns
Address CE to Ready	TARY	9, 10, 11	-55°C, +25°C, +125°C	-	160	ns
Recovery Time Between Controls	TRV	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns

NOTES:

1. Or TAD - (TAL + TLC), whichever is greater.
2. Defines ALE to Data Out Valid in conjunction with TAL.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	T_A = +25°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	T_A = +25°C	-	10	pF

NOTE:

1. All measurements referenced to device ground.

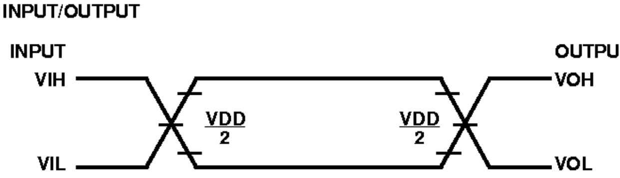
TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Table 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

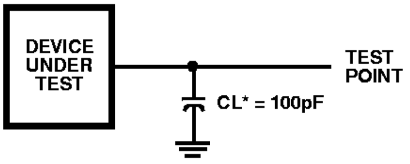
PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
Input Leakage Current	IIH	± 100nA
Static Current	IDDSB	±30µA

A.C. Testing Input, Output Waveform



A.C. TESTING: All input signals must switch between VIL max and VIH min, tr and tf must be less than or equal to 15ns.

A.C. Testing Load Circuit (Note 1)



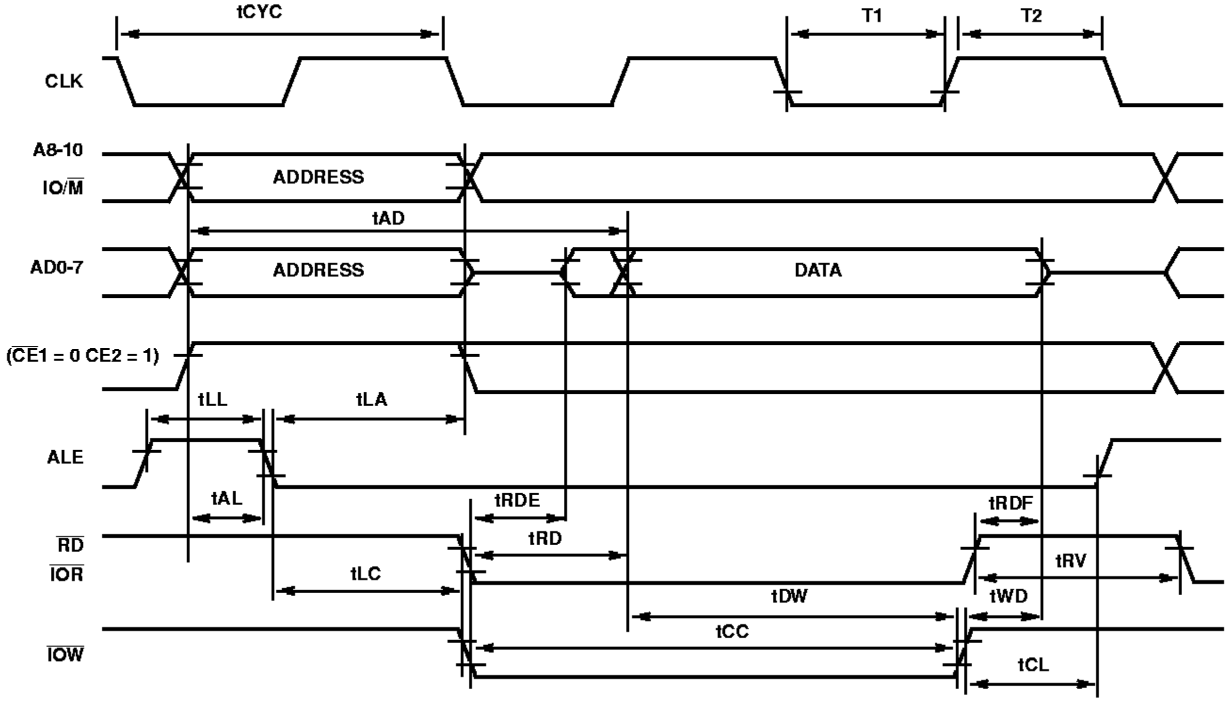
* CL includes stray and jig capacitance.

NOTES:

1. Output timings are measured with purely capacitive load.
2. Devices screened to more rigorous electrical specifiecations are available. Contact your nearest Harris representative for details.

Waveforms

ROM READ AND I/O READ AND WRITE



83C55RH CLOCK SPECIFICATIONS