

LCD Controllers/Interfaces

■ LCD controllers

LCD controllers prepare the display data for dot-matrix display and control the display drivers. The load of microprocessor for display is reduced by these devices.

SED1330FBA/BB, SED1335F0A/0B, and SED1336F0A

These ICs manage its own dedicated display memory. The display data is manipulated using instructions from the microprocessor.

Features

- $V_{DD} = 5.0 V \pm 10\%$ (SED1330FBA/BB), $V_{DD} = 2.7$ to $5.5 V$ (SED1335F0A/0B), or $V_{DD} = 3.0$ to $5.5 V$ (SED1336F0A)
- Output to LCD-screen TVs (SED1336F0A)
- Character and graphic screens can be overlaid, with a maximum of three graphics screens.
- Built-in character generator
- Smooth horizontal scrolling
- Split-screen operation
- Display memory management (VRAM) of up to 64 Kbytes

SED1351F0A/SED1351FLB, SED1352F0B

The SED1351F0A/LB and SED1352F0B uses display data stored in microprocessor memory. The microprocessor accesses and manipulates display data directly.

Features

- $V_{DD} = 5 V \pm 10\%$ (SED1351F0A), $V_{DD} = 2.7$ to $3.6 V$ (SED1351FLB), $V_{DD} = 2.7$ to $5.5 V$ (SED1352F0B)
- Making access from MPU to VRAM by cycle steal.
- Smooth scrolling to the vertical direction.
- Display memory capacity : 64 KB (Max.) (SED1351F0A/FLB) or 128 KB (Max.) (SED1352F0B)
- The image plane can be vertically divided into two parts.
- Gray scale : Max. 4 levels (SED1351F0A/FLB) or max. 16 levels (SED1352F0B)
- OR indications of two pictures are available.

Part number	Display area (pixels)	Microprocessor interface	Display modes	VRAM location	Package	Evaluation board
SED1330FBA	640×256×3	68-series, 80-series, 8-bit bus	Character, graphics	Controller address space	QFP5-60pin	SDU1330BcA
SED1330FBB					QFP6-60pin	
SED1335F0A					QFP5-60pin	—
SED1335F0B					QFP6-60pin	
SED1336F0A	640×256×3 (LCD) 256×200×3 (TV)				QFP6-60pin	SDU1336BcA
SED1351F0A	524,288	80-series, 8- or 16-bit bus	Graphics	Microprocessor address space	QFP5-100pin	SDU1351Bc1/02
SED1351FLB						
SED1352F0B	640×400 (16-level gray scale)	Applicable to 68-series, 80-series 8-bit and ISA bus		MPU address space	Chip QFP5-100pin QFP15-100pin	SDU1352#cc
SED1353F0A	640×200 (256 color)				Planning	