National Semiconductor

ADVANCED INFORMATION

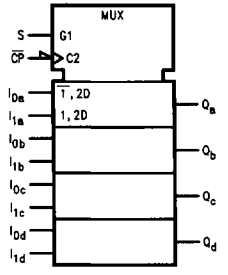
54F/74F298
Quad 2-Input Multiplexer with Storage

General Description

This device is a high-speed multiplexer with storage. It selects four bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Logic Symbols

IEEE/IEC



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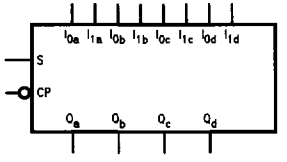

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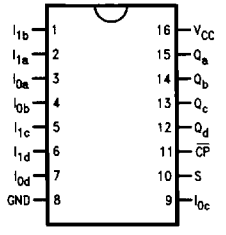
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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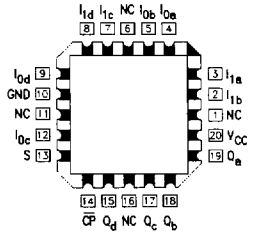
Pin Assignment for LCC and PCC



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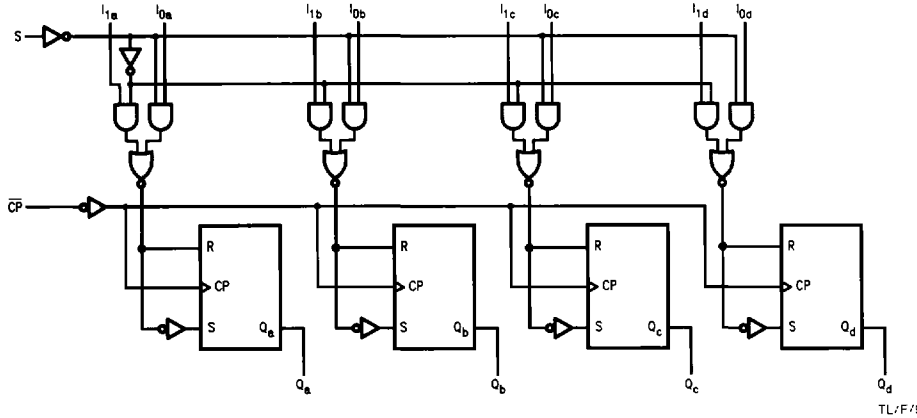
Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.