# CRYSTAL OSCILLATOR (XO) (10 MHZ TO 1.4 GHZ)

## Features

- Available with any-rate output frequencies from 10 MHz to 945 MHz and select frequencies to 1.4 GHz
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

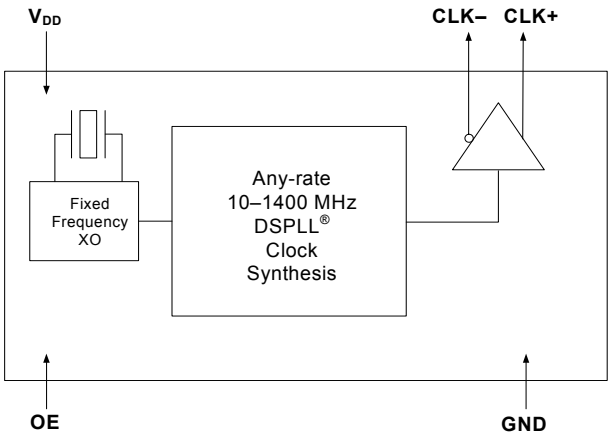
## Applications

- SONET/SDH
- Networking
- SD/HD video
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clock generation

## Description

The Si530/531 XO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low jitter clock at high frequencies. The Si530/531 is available with any-rate output frequency from 10 to 945 MHz and select frequencies to 1400 MHz. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si530/531 uses one fixed crystal to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si530/531 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

## Functional Block Diagram





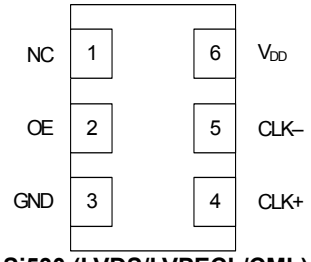
**Ordering Information:**

See page 7.

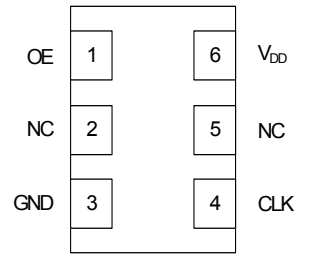
**Pin Assignments:**

See page 6.

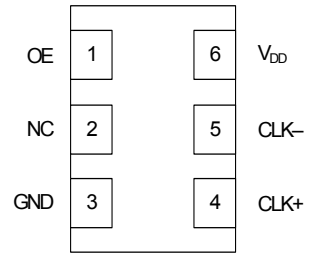
(Top View)




**Si530 (LVDS/LVPECL/CML)**




**Si530 (CMOS)**




**Si531 (LVDS/LVPECL/CML)**

# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage[1] | $V_{DD}$ | 3.3 V option | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V option | 2.25 | 2.5 | 2.75 | |
| | | 1.8 V option | 1.71 | 1.8 | 1.89 | |
| Supply Current | $I_{DD}$ | Output enabled<br>LVPECL<br>CML<br>LVDS<br>CMOS | <br>—<br>—<br>—<br>— | <br>111<br>99<br>90<br>81 | <br>121<br>108<br>98<br>88 | mA |
| | | TriState mode | — | 60 | 70 | |
| Output Enable (OE)[2] | | $V_{IH}$ | 0.75 x $V_{DD}$ | — | — | V |
| | | $V_{IL}$ | — | — | 0.5 | |
| Operating Temperature Range[3] | $T_A$ | | –40 | — | 85 | ºC |

**Notes:**
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 7 for further details.
2. OE pin includes a 17 kΩ pullup resistor to $V_{DD}$. Pulling OE to ground causes outputs to tristate.
3. If the device is powered up below –20 ºC and the ambient temperature rises by approximately 105 ºC during normal operation, the device will perform a one-time recalibration. The output is squelched for approximately 2–3 ms during this recalibration.

### Table 2. CLK± Output Frequency Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Nominal Frequency[1,2] | $f_O$ | LVPECL/LVDS/CML | 10 | — | 945 | MHz |
| | | CMOS | 10 | — | 160 | |
| Initial Accuracy | $f_i$ | Measured at +25 °C at time of shipping | — | ±1.5 | — | ppm |
| Temperature Stability[1,3] | $\Delta f/f_O$ | | –20<br>–50 | —<br>— | +20<br>+50 | ppm |
| Aging | $f_a$ | Frequency drift over projected 15 year life | — | — | ±10 | ppm |
| Powerup Time[4] | $t_{OSC}$ | | — | — | 10 | ms |

**Notes:**
1. See Section 3. "Ordering Information" on page 7 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Selectable parameter specified by part number.
4. Time from powerup or tristate mode to $f_O$.

**Table 3. CLK± Output Levels and Symmetry**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LVPECL Output Option[1] | $V_O$ | mid-level | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| | $V_{OD}$ | swing (diff) | 1.1 | — | 1.9 | $V_{PP}$ |
| | $V_{SE}$ | swing (single-ended) | 0.5 | — | 0.93 | $V_{PP}$ |
| LVDS Output Option[2] | $V_O$ | mid-level | 1.125 | 1.20 | 1.275 | V |
| | $V_{OD}$ | swing (diff) | 0.32 | 0.40 | 0.50 | $V_{PP}$ |
| CML Output Option[2] | $V_O$ | mid-level | — | $V_{DD}$ – 0.75 | — | V |
| | $V_{OD}$ | swing (diff) | 0.70 | 0.95 | 1.20 | $V_{PP}$ |
| CMOS Output Option[3] | $V_{OH}$ | $I_{OH}$ = 32 mA | 0.8 x $V_{DD}$ | — | $V_{DD}$ | V |
| | $V_{OL}$ | $I_{OL}$ = 32 mA | — | — | 0.4 | |
| Rise/Fall time (20/80%) | $t_R$, $t_F$ | LVPECL/LVDS/CML | — | — | 350 | ps |
| | | CMOS with CL = 15 pF | — | 1 | — | ns |
| Symmetry (duty cycle) | SYM | LVPECL: $V_{DD}$ – 1.3 V (diff)<br>LVDS: 1.25 V (diff)<br>CMOS: $V_{DD}$/2 | 45 | — | 55 | % |

**Notes:**
1. 50 Ω to $V_{DD}$ – 2.0 V.
2. $R_{term}$ = 100 Ω (differential).
3. $C_L$ = 15 pF

**Table 4. CLK± Output Phase Jitter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS)* for $F_{OUT} \geq$ 500 MHz | $\phi_J$ | 12 kHz to 20 MHz (OC-48) | — | 0.40 | 0.50 | ps |
| | | 50 kHz to 80 MHz (OC-192) | | | | |
| | | LVPECL | — | 0.30 | 0.40 | ps |
| | | CML | — | 0.35 | 0.47 | |
| | | LVDS | — | 0.40 | 0.49 | |
| Phase Jitter (RMS)* for $F_{OUT}$ of 125 to 500 MHz | $\phi_J$ | 12 kHz to 20 MHz (OC-48) | | | | |
| | | LVPECL | — | 0.40 | 0.50 | ps |
| | | CML | — | 0.45 | 0.50 | |
| | | LVDS | — | 0.45 | 0.52 | |

***Note:** Differential Modes: LVPECL/LVDS/CML. Refer to AN256 for further information.

### Table 5. CLK± Output Period Jitter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Period Jitter* for $F_{OUT} \leq 160$ MHz | $J_{PER}$ | RMS | — | 1 | — | ps |
| | | Peak-to-Peak | — | 5 | — | |
| ***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information. | | | | | | |

### Table 6. CLK± Output Phase Noise (Typical)

| Configuration | $f_C$ Output | 81.25 MHz LVDS | 312.5 MHz LVPECL | 1066 MHz LVPECL | Units |
|---|---|---|---|---|---|
| Offset Frequency (f) | | $\mathcal{L}$ (f) | | | dBc/Hz |
| 100 Hz | | –110 | –100 | –87 | |
| 1 kHz | | –127 | –115 | –102 | |
| 10 kHz | | –134 | –119 | –107 | |
| 100 kHz | | –136 | –123 | –111 | |
| 1 MHz | | –143 | –135 | –121 | |
| 10 MHz | | –147 | –144 | –135 | |
| 100 MHz | | n/a | –147 | –142 | |

### Table 7. Absolute Maximum Ratings[1]

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.5 to +3.8 | Volts |
| Input Voltage (any input pin) | $V_I$ | –0.5 to $V_{DD}$ + 0.3 | Volts |
| Storage Temperature | $T_S$ | –55 to +125 | ºC |
| ESD Sensitivity (HBM, per JESD22-A114) | ESD | >2500 | Volts |
| Soldering Temperature (Pb-free profile)[2] | $T_{PEAK}$ | 260 | ºC |
| Soldering Temperature Time @ $T_{PEAK}$ (Pb-free profile)[2] | $t_P$ | 10 | seconds |

**Notes:**
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions.
2. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

**Table 8. Environmental Compliance**

The Si530/531 meets the following qualification test requirements.

| Parameter | Conditions/ Test Method |
|---|---|
| Mechanical Shock | MIL-STD-883F, Method 2002.3 B |
| Mechanical Vibration | MIL-STD-883F, Method 2007.3 A |
| Solderability | MIL-STD-883F, Method 203.8 |
| Gross & Fine Leak | MIL-STD-883F, Method 1014.7 |
| Resistance to Solvents | MIL-STD-883F, Method 2016 |

## 2. Pin Descriptions

(Top View)

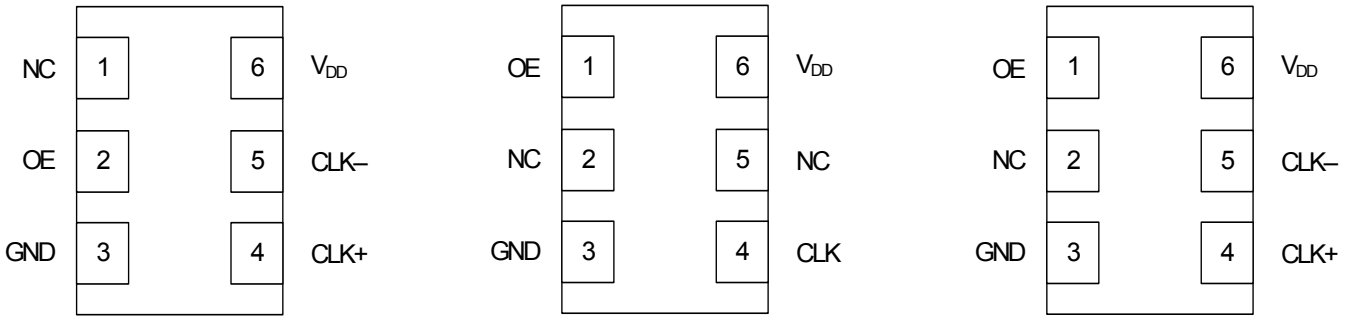



**Table 9. Pinout for Si530 Series**

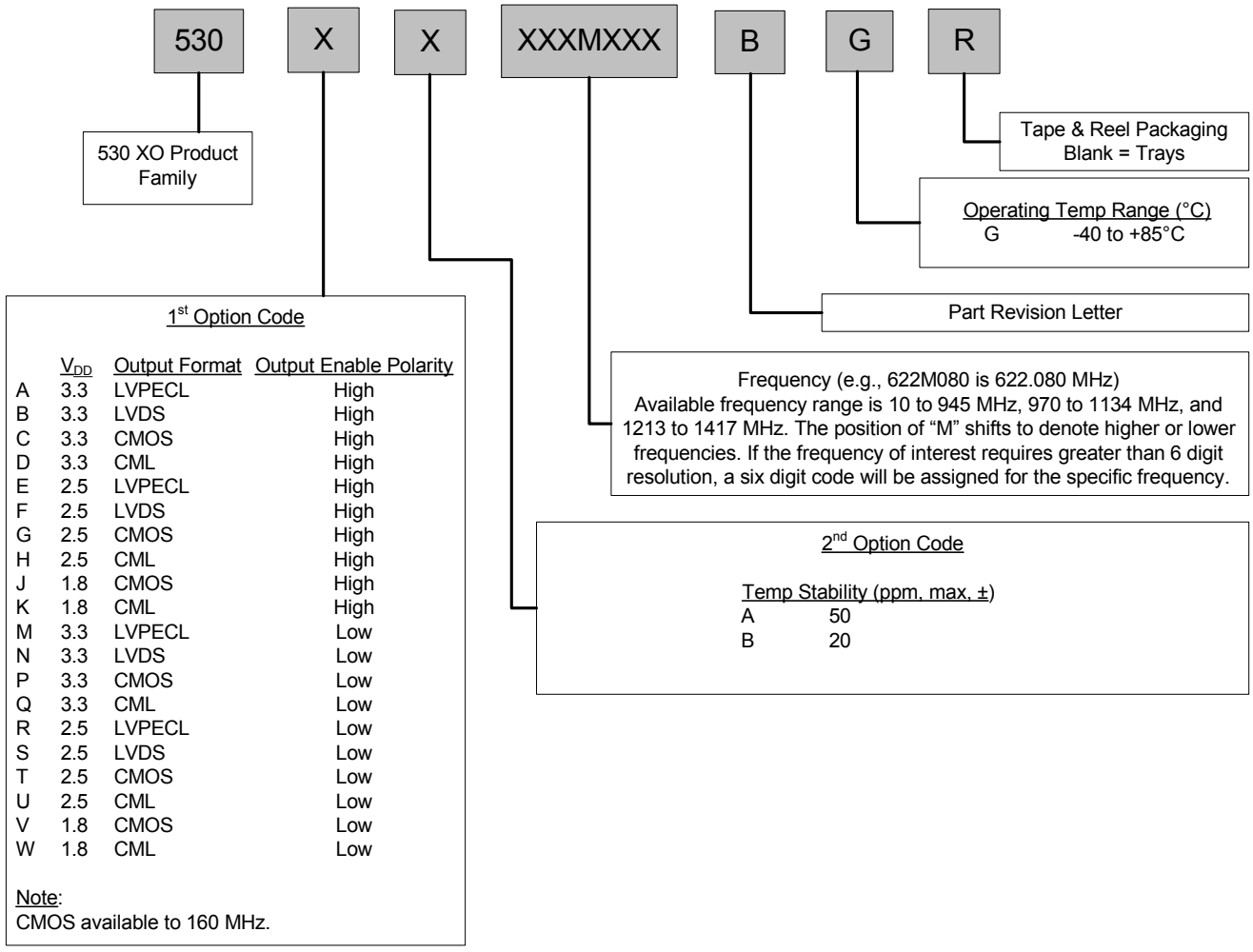
| Pin | Symbol | LVDS/LVPECL/CML Function | CMOS Function |
|---|---|---|---|
| 1 | OE (CMOS only) | No connection | Output enable<br>0 = clock output disabled (outputs tristated)<br>1 = clock output enabled |
| 2 | OE<br>(LVPECL,LVDS, CML) | Output enable<br>0 = clock output disabled (outputs tristated)<br>1 = clock output enabled | No connection |
| 3 | GND | Electrical and Case Ground | Electrical and Case Ground |
| 4 | CLK+ | Oscillator Output | Oscillator Output |
| 5 | CLK– | Complementary output | No connection |
| 6 | $V_{DD}$ | Power Supply Voltage | Power Supply Voltage |

**Table 10. Pinout for Si531 Series**

| Pin | Symbol | LVDS/LVPECL/CML Function |
|---|---|---|
| 1 | OE (LVPECL, LVDS, CML) | Output enable<br>0 = clock output disabled (outputs tristated)<br>1 = clock output enabled |
| 2 | No connection | No connection |
| 3 | GND | Electrical and Case Ground |
| 4 | CLK+ | Oscillator Output |
| 5 | CLK– | Complementary output |
| 6 | $V_{DD}$ | Power Supply Voltage |

## 3. Ordering Information

The Si530/531 XO was designed to support a variety of options including frequency, temperature stability, output format, and $V_{DD}$. Specific device configurations are programmed into the Si530/531 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si530 and Si531 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm package. The 531 Series supports an alternate OE pinout (pin #1) for the LVPECL, LVDS, and CML output formats. See Tables 9 and 10 for the pinout differences between the Si530 and Si531 series.




Example P/N: 530AB622M080BGR is a 5 x 7 XO in a 6 pad package. The frequency is 622.080 MHz, with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specifed as ±20 ppm. The part is specified for –40 to +85 °C ambient temperature range operation and is shipped in tape and reel format.

**Figure 1. Part Number Convention**

## 4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si530/531. Table 11 lists the values for the dimensions shown in the illustration.

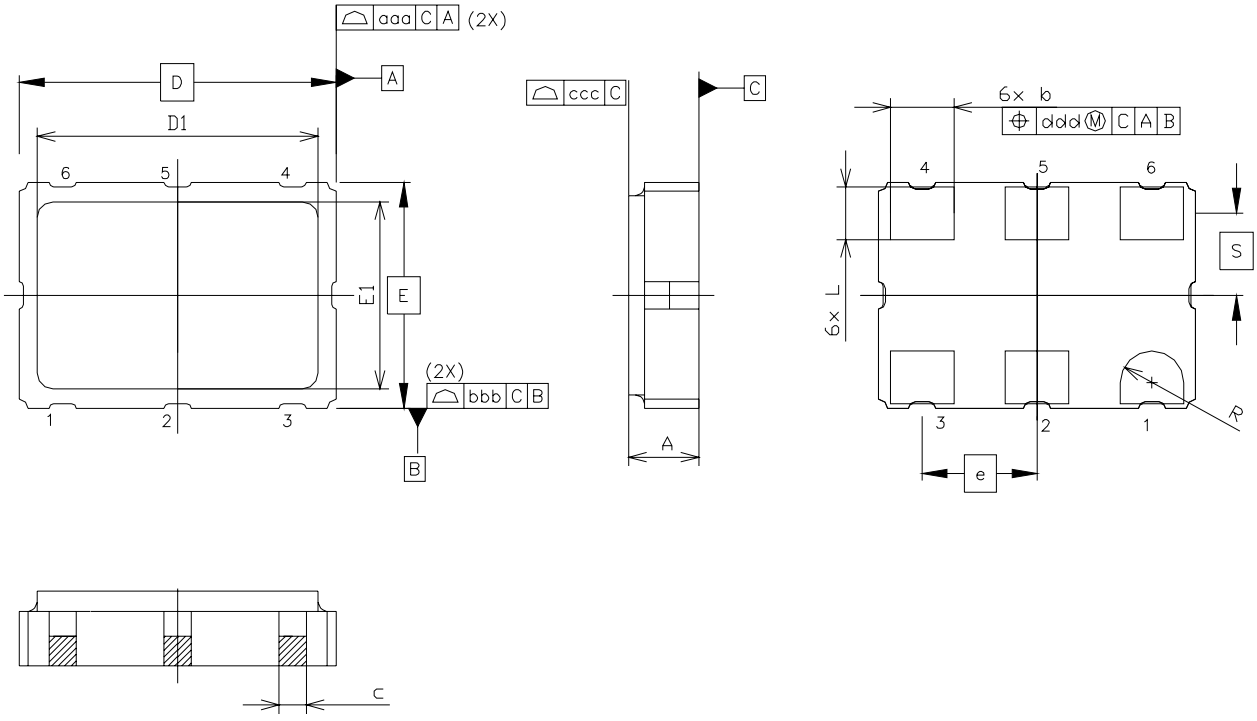



**Figure 2. Si530/531 Outline Diagram**

**Table 11. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.45 | 1.65 | 1.85 |
| b | 1.2 | 1.4 | 1.6 |
| c | | 0.60 TYP. | |
| D | | 7.00 BSC. | |
| D1 | 6.10 | 6.2 | 6.30 |
| e | | 2.54 BSC. | |
| E | | 5.00 BSC. | |
| E1 | 4.30 | 4.40 | 4.50 |
| L | 1.07 | 1.27 | 1.47 |
| S | | 1.815 BSC. | |
| R | | 0.7 REF. | |
| aaa | — | — | 0.15 |
| bbb | — | — | 0.15 |
| ccc | — | — | 0.10 |
| ddd | — | — | 0.10 |

## 5. 6-Pin PCB Land Pattern

Figure 3 illustrates the 6-pin PCB land pattern for the Si530/531. Table 12 lists the values for the dimensions shown in the illustration.

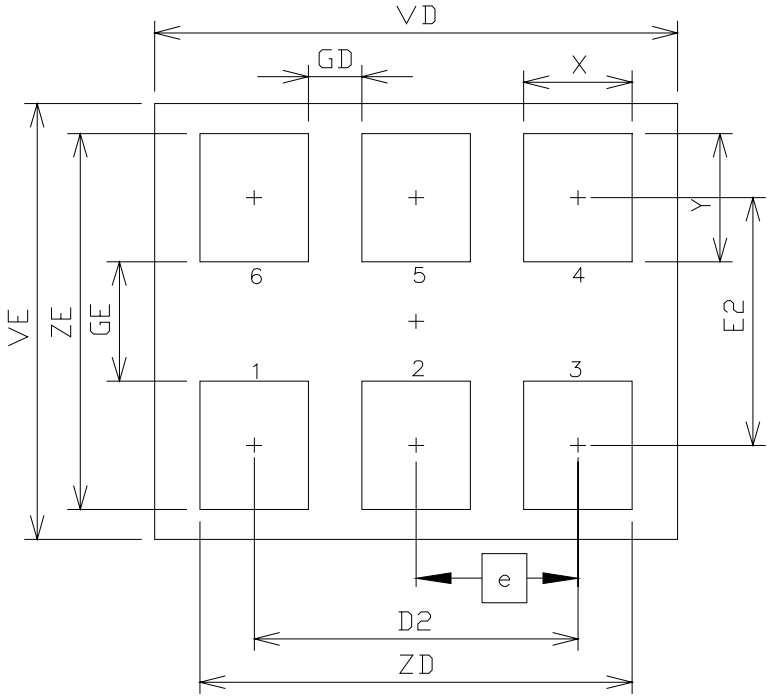



**Figure 3. Si530/531 PCB Land Pattern**

**Table 12. PCB Land Pattern Dimensions (mm)**

| Dimension | Min | Max |
|---|---|---|
| D2 | 5.08 REF | |
| e | 2.54 BSC | |
| E2 | 4.15 REF | |
| GD | 0.84 | — |
| GE | 2.00 | — |
| VD | 8.20 REF | |
| VE | 7.30 REF | |
| X | 1.70 TYP | |
| Y | 2.15 REF | |
| ZD | — | 6.78 |
| ZE | — | 6.30 |

**Notes:**
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

# DOCUMENT CHANGE LIST

## Revision 0.4 to Revision 0.5

- Updated Table 1, “Recommended Operating Conditions,” on page 2.
  - Added maximum supply current specifications.
  - Specified relationship between temperature at startup and operation temperature.
- Updated Table 4, “CLK± Output Phase Jitter,” on page 3 to include maximum rms jitter generation specifications and updated typical rms jitter specifications.
- Added Table 6, “CLK± Output Phase Noise (Typical),” on page 4.
- Added Output Enable active polarity as an option in Figure 1, “Part Number Convention,” on page 7.

## Revision 0.5 to Revision 1.0

- Updated Note 3 in Table 1, “Recommended Operating Conditions,” on page 2.
- Updated Figure 1, “Part Number Convention,” on page 7.

## NOTES:

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