FAIRCHILD SEMICONDUCTOR

March 1998

# 100398
# Quad Differential ECL/TTL Translating Transceiver with Latch

## General Description

The 100398 is a quad latched transceiver designed to convert TTL logic levels to differential F100K ECL logic levels and vice versa. This device was designed with the capability of driving a differential 25Ω ECL load with cutoff capability, and will sink a 64 mA TTL load. The 100398 is ideal for mixed technology applications utilizing either an ECL or TTL backplane.

The direction of translation is set by the direction control pin (DIR). The DIR pin on the 100398 accepts TTL logic levels. A TTL LOW on DIR sets up the ECL pins as inputs and TTL pins as outputs. A TTL HIGH on DIR sets up the TTL pins as inputs and ECL pins as outputs.

A LOW on the output enable input pin (OE) holds the ECL output in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the latch transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

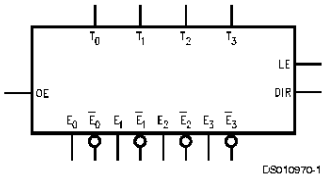
The 100398 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All Inputs have 50 kΩ pull-down resistors.

## Features

- Differential ECL input/output structure
- 64 mA FAST TTL outputs
- 25Ω differential ECL outputs with cut-off
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- 3-STATE outputs
- Voltage compensated operating range = –4.2V to –5.7V

## Ordering Code:

## Logic Symbol

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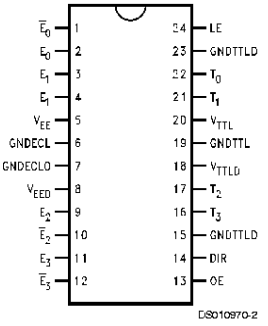
## Connection Diagrams

### 24-Pin DIP

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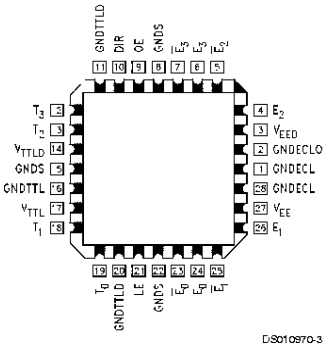
### 28-Pin PCC

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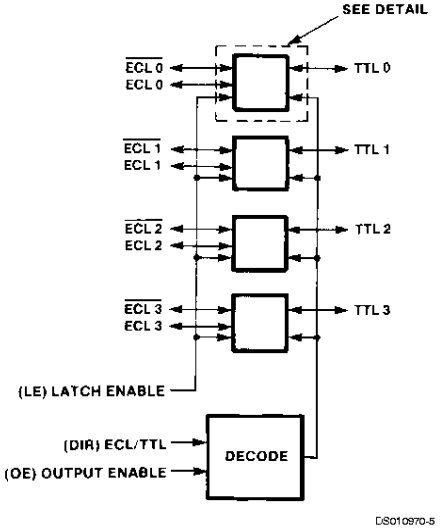
## Functional Diagram

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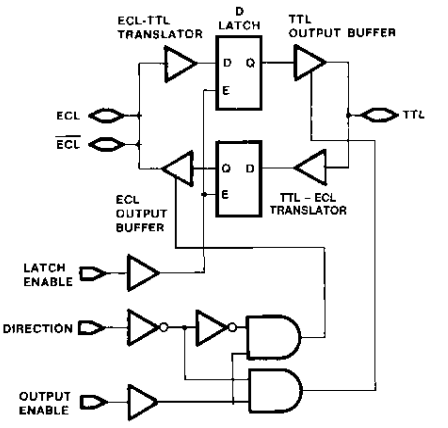
**Note:** LE and OE use TTL logic levels

## Detail




DS010970-6

| Pin Names | Description |
|---|---|
| $E_0$–$E_3$ | ECL Data I/O |
| $\overline{E_0}$–$\overline{E_3}$ | Complementary ECL Data I/O |
| $T_0$–$T_3$ | TTL Data I/O |
| OE | Output Enable Input Levels |
| LE | Latch Enable Input Levels |
| DIR | Direction Control Input (TTL levels) |
| GNDECL | ECL Ground |
| GNDECLO | ECL Output Ground |
| GNDS | ECL Ground-to-Substrate |
| $V_{EE}$ | ECL Quiescent Power Supply |
| $V_{EED}$ | ECL Dynamic Power Supply |
| GNDTTL | TTL Quiescent Ground |
| GNDTTLD | TTL Dynamic Ground |
| $V_{TTL}$ | TTL Quiescent Power Supply |
| $V_{TTLD}$ | TTL Dynamic Power Supply |

## Truth Table

| LE | DIR | OE | ECL Port | TTL Port | Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | LOW (Cut-Off) | Z | |
| 0 | 0 | 1 | Input | Output | 1, 4 |
| 0 | 1 | 0 | LOW (Cut-Off) | Z | |
| 0 | 1 | 1 | Output | Input | 2, 4 |
| 1 | 0 | 0 | Input | Z | 1, 3 |
| 1 | 0 | 1 | Latched | X | 1, 3 |
| 1 | 1 | 0 | Low (Cut-Off) | Input | 2, 3 |
| 1 | 1 | 1 | Latched | X | 2, 3 |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

**Note 1:** ECL input to TTL output mode

**Note 2:** TTL input to ECL output mode

**Note 3:** Retains data present before LE set HIGH

**Note 4:** Latch is transparent

## Absolute Maximum Ratings (Note 5)

| | |
|---|---|
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| $V_{TTL}$ Pin Potential to Ground Pin | −0.5V to +6.0V |
| ECL Input Voltage (DC) | $V_{EE}$ to +0.5V |
| ECL Output Current (DC Output HIGH) | −50 mA |
| TTL Input Voltage (Note 8) | −0.5V to +7.0V |
| TTL Input Current (Note 8) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State 3-STATE Output | −0.5V to +5.5V |
| Current Applied to TTL Output in LOW State (Max) | Twice the Rated $I_{OL}$ (mA) |
| ESD (Note 6) | ≥2000V |

## Recommended Operating Conditions

| | |
|---|---|
| Case Temperature ($T_C$) | |
| Commercial | 0°C to +85°C |
| Industrial | −40°C to +85°C |
| Military | −55°C to +125°C |
| ECL Supply Voltage ($V_{EE}$) | −5.7V to −4.2V |
| TTL Supply Voltage ($V_{TTL}$) | +4.5V to +5.5V |

**Note 5:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 6:** ESD testing conforms to MIL-STD-883, Method 3015.

## Commercial Version TTL-to-ECL DC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, GND = 0V, $T_C$ = 0°C to +85°C, $V_{TTL}$ = +4.5V to +5.5V (Note 8)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −870 | mV | $V_{IN}$ = $V_{IH(Max)}$ or $V_{IL(Min)}$ |
| $V_{OL}$ | Output LOW Voltage | −1830 | −1705 | −1620 | mV | Loading with 50Ω to − 2V |
| | Cutoff Voltage | | −2000 | −1950 | mV | OE and LE Low, DIR High<br>$V_{IN}$ = $V_{IH(Max)}$ or $V_{IL}$(Min),<br>Loading with 50Ω to −2V |
| $V_{OHC}$ | Output HIGH Voltage Corner Point High | −1035 | | | mV | $V_{IN}$ = $V_{IH(Min)}$ or $V_{IL(Max)}$<br>Loading with 50Ω to −2V |
| $V_{OLC}$ | Output LOW Voltage Corner Point Low | | | −1610 | mV | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 5.0 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $V_{IL}$ | Input LOW Voltage | 0 | | 0.8 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | μA | $V_{IN}$ = +2.7V |
| | Breakdown Test | | | 0.5 | mA | $V_{IN}$ = +5.5V |
| $I_{IL}$ | Input LOW Current | −700 | | | μA | $V_{IN}$ = +0.5V |
| $V_{FCD}$ | Input Clamp Diode Voltage | −1.2 | | | V | $I_{IN}$ = −18 mA |
| $I_{EE}$ | $V_{EE}$ Supply Current | −99 | | −50 | mA | LE Low, OE and DIR High<br>Inputs Open |
| $I_{EEZ}$ | $V_{EE}$ Supply Current | −159 | | −90 | mA | LE and OE Low, DIR High<br>Inputs Open |

**Note 7:** Either voltage limit or current limit is sufficient to protect inputs.

**Note 8:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## ECL-to-TTL DC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = 0˚C to +85˚C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V (Note 9)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.1 | | V | $I_{OH}$ = –3 mA, $V_{TTL}$ = 4.75V |
| | | 2.4 | 2.9 | | V | $I_{OH}$ = –3 mA, $V_{TTL}$ = 4.50V |
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $I_{OL}$ = 24 mA, $V_{TTL}$ = 4.50V |
| $V_{IH}$ | Input HIGH Voltage | –1165 | | –870 | mV | Guaranteed HIGH Signal for All Inputs |
| $V_{IL}$ | Input LOW Voltage | –1830 | | –1475 | mV | Guaranteed LOW Signal for All Inputs |
| $V_{DIFF}$ | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| $V_{CM}$ | Common Mode Voltage | GNDECL – 2.0 | | GNDECL – 0.5 | V | |
| $I_{IH}$ | Input HIGH Current | | | 30 | µA | $V_{IN}$ = $V_{IH}$ (Max) |
| $I_{IL}$ | Input LOW Current | 0.50 | | | µA | $V_{IN}$ = $V_{IL}$ (Min) |
| $I_{OZHT}$ | 3-STATE Current Output High | | | 70 | µA | $V_{OUT}$ = +2.7V |
| $I_{OZLT}$ | 3-STATE Current Output Low | –650 | | | µA | $V_{OUT}$ = +0.5V |
| $I_{OS}$ | Output Short-Circuit Current | –100 | | –225 | mA | $V_{OUT}$ = 0.0V, $V_{TTL}$ = +5.5V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | $V_{OUT}$ = 5.5V |
| $I_{ZZ}$ | Bus Drainage Test | | | 500 | µA | $V_{OUT}$ = 5.25V |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | | 39 | mA | TTL Outputs LOW |
| | | | | 27 | mA | TTL Outputs HIGH |
| | | | | 39 | mA | TTL Outputs in 3-STATE |

**Note 9:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DIP and PCC TTL-to-ECL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | $T_C$ = 0˚C | | $T_C$ = 25˚C | | $T_C$ = 85˚C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $F_{max}$ | Toggle Frequency | 180 | | 180 | | 180 | | MHz | |
| $t_{PLH}$ $t_{PHL}$ | $T_n$ to $E_n$, $\overline{E}_n$ (Transparent) | 0.90 | 2.10 | 0.80 | 2.20 | 0.70 | 2.50 | ns | *Figures 1, 3* |
| $t_{PLH}$ $t_{PHL}$ | LE to $E_n$, $\overline{E}_n$ | 1.40 | 2.70 | 1.50 | 2.70 | 1.80 | 3.10 | ns | *Figures 1, 3* |
| $t_{PZH}$ | OE to $E_n$, $\overline{E}_n$ (Cutoff to High) | 2.90 | 8.00 | 2.80 | 6.90 | 2.80 | 5.80 | ns | *Figures 1, 3* |
| $t_{PHZ}$ | OE to $E_n$, $\overline{E}_n$ (High to Cutoff) | 1.30 | 2.70 | 1.40 | 2.90 | 1.70 | 3.40 | ns | *Figures 1, 3* |
| $t_{PHZ}$ | DIR to $E_n$, $\overline{E}_n$ (High to Cutoff) | 1.30 | 2.70 | 1.40 | 2.90 | 1.80 | 3.50 | ns | *Figures 1, 3* |
| $t_S$ | $T_n$ to LE | 0.70 | | 0.70 | | 0.70 | | ns | *Figures 1, 3* |
| $t_H$ | $T_n$ to LE | 0.90 | | 0.80 | | 0.70 | | ns | *Figures 1, 3* |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | *Figures 1, 3* |

## DIP and PCC ECL-to-TTL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, $C_L$ = 50 pF

| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = 25°C | | $T_C$ = 85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $F_{max}$ | Toggle Frequency | 75 | | 75 | | 75 | | MHz | |
| $t_{PLH}$ | $E_n$, $\overline{E}_n$ to $T_n$ | 1.70 | 4.90 | 1.70 | 5.10 | 1.80 | 5.80 | ns | *Figures 2, 4* |
| $t_{PHL}$ | (Transparent) | | | | | | | | |
| $t_{PLH}$ | LE to $T_n$ | 2.30 | 4.60 | 2.40 | 4.70 | 2.60 | 4.90 | ns | *Figures 2, 4* |
| $t_{PHL}$ | | 3.30 | 5.50 | 3.50 | 5.70 | 4.00 | 6.70 | | |
| $t_{PZH}$ | OE to $T_n$ | 2.30 | 4.90 | 2.10 | 4.70 | 2.00 | 4.30 | ns | *Figures 2, 5* |
| $t_{PZL}$ | (Enable Time) | 4.10 | 7.90 | 4.10 | 7.80 | 4.20 | 7.80 | | |
| $t_{PHZ}$ | OE to $T_n$ | 3.30 | 7.90 | 3.30 | 7.50 | 3.70 | 7.90 | ns | *Figures 2, 5* |
| $t_{PLZ}$ | (Disable Time) | 4.10 | 7.50 | 4.30 | 7.80 | 5.30 | 9.40 | | |
| $t_{PHZ}$ | DIR to $T_n$ | 2.00 | 6.00 | 1.90 | 5.70 | 1.70 | 5.20 | ns | *Figures 2, 6* |
| $t_{PLZ}$ | (Disable Time) | 2.00 | 4.00 | 2.00 | 3.70 | 1.90 | 3.70 | | |
| $t_S$ | $E_n$, $\overline{E}_n$ to LE | 0.50 | | 0.50 | | 0.50 | | ns | *Figures 2, 4* |
| $t_H$ | $E_n$, $\overline{E}_n$ to LE | 1.00 | | 1.00 | | 1.00 | | ns | *Figures 2, 4* |

## Industrial Version
## TTL-to-ECL DC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –40°C to +85°C, $V_{TTL}$ = +4.5V to +5.5V (Note 10)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | –1085 | –955 | –870 | mV | $V_{IN}$ = $V_{IH(Max)}$ or $V_{IL(Min)}$ |
| $V_{OL}$ | Output LOW Voltage | –1830 | –1705 | –1575 | mV | Loading with 50Ω to –2V |
| | Cutoff Voltage | | –2000 | –1900 | mV | OE and LE Low, DIR High<br>$V_{IN}$= $V_{IH(Max)}$ or $V_{IL(Min)}$,<br>Loading with 50Ω to –2V |
| $V_{OHC}$ | Output HIGH Voltage<br>Corner Point High | –1095 | | | mV | $V_{IN}$ = $V_{IH(Min)}$ or $V_{IL(Max)}$<br>Loading with 50Ω to –2V |
| $V_{OLC}$ | Output LOW Voltage<br>Corner Point Low | | | –1565 | mV | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 5.0 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $V_{IL}$ | Input LOW Voltage | 0 | | 0.8 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | μA | $V_{IN}$ = +2.7V |
| | Breakdown Test | | | 0.5 | mA | $V_{IN}$ = +5.5V |
| $I_{IL}$ | Input LOW Current | –700 | | | μA | $V_{IN}$ = +0.5V |
| $V_{FCD}$ | Input Clamp<br>Diode Voltage | –1.2 | | | V | $I_{IN}$ = –18 mA |
| $I_{EE}$ | $V_{EE}$ Supply Current | –99 | –40 | | mA | LE Low, OE and DIR High<br>Inputs Open |

**Note 10:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## ECL-to-TTL DC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –40°C to +85°C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V (Note 11)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.1 | | V | $I_{OH}$ = –3 mA, $V_{TTL}$ = 4.75V |
| | | 2.4 | 2.9 | | V | $I_{OH}$ = –3 mA, $V_{TTL}$ = 4.50V |
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $I_{OL}$ = 24 mA, $V_{TTL}$ = 4.50V |
| $V_{IH}$ | Input HIGH Voltage | –1170 | | –870 | mV | Guaranteed HIGH Signal for All Inputs |

## ECL-to-TTL DC Electrical Characteristics (Continued)

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –40°C to +85°C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V (Note 11)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | –1830 | | –1480 | mV | Guaranteed LOW Signal for All Inputs |
| $V_{DIFF}$ | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| $V_{CM}$ | Common Mode Voltage | GNDECL – 2.0 | | GNDECL – 0.5 | V | |
| $I_{IH}$ | Input HIGH Current | | | 35 | µA | $V_{IN} = V_{IH(Max)}$ |
| $I_{IL}$ | Input LOW Current | 0.50 | | | µA | $V_{IN} = V_{IH(Min)}$ |
| $I_{OZHT}$ | 3-STATE Current Output High | | | 70 | µA | $V_{OUT}$ = +2.7V |
| $I_{OZLT}$ | 3-STATE Current Output Low | –650 | | | µA | $V_{OUT}$ = +0.5V |
| $I_{OS}$ | Output Short-Circuit Current | –100 | | –225 | mA | $V_{OUT}$ = 0.0V, $V_{TTL}$ = +5.5V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | $V_{OUT}$ = 5.5V |
| $I_{ZZ}$ | Bus Drainage Test | | | 500 | µA | $V_{OUT}$ = 5.25V |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | | 39 | mA | TTL Outputs LOW |
| | | | | 27 | mA | TTL Outputs HIGH |
| | | | | 39 | mA | TTL Outputs in 3-STATE |

**Note 11:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## PCC TTL-to-ECL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | $T_C$ = –40°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $F_{max}$ | Toggle Frequency | 180 | | 180 | | 180 | | MHz | |
| $t_{PLH}$ $t_{PHL}$ | $T_n$ to $E_n$, $\overline{E}_n$ (Transparent) | 0.90 | 2.40 | 0.80 | 2.20 | 0.70 | 2.50 | ns | *Figures 1, 3* |
| $t_{PLH}$ $t_{PHL}$ | LE to $E_n$, $\overline{E}_n$ | 1.30 | 2.70 | 1.50 | 2.70 | 1.80 | 3.10 | ns | *Figures 1, 3* |
| $t_{PZH}$ | OE to $E_n$, $\overline{E}_n$ (Cutoff to High) | 2.90 | 9.00 | 2.80 | 6.90 | 2.80 | 5.80 | ns | *Figures 1, 3* |
| $t_{PHZ}$ | OE to $E_n$, $\overline{E}_n$ (High to Cutoff) | 1.10 | 2.70 | 1.40 | 2.90 | 1.70 | 3.40 | ns | *Figures 1, 3* |
| $t_{PHZ}$ | DIR to $E_n$, $\overline{E}_n$ (High to Cutoff) | 1.10 | 2.70 | 1.40 | 2.90 | 1.80 | 3.50 | ns | *Figures 1, 3* |
| $t_S$ | $T_n$ to LE | 0.70 | | 0.70 | | 0.70 | | ns | *Figures 1, 3* |
| $t_H$ | $T_n$ to LE | 0.90 | | 0.90 | | 0.90 | | ns | *Figures 1, 3* |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.20 | 0.45 | 1.50 | 0.45 | 1.50 | ns | *Figures 1, 3* |

## PCC ECL-to-TTL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, $C_L$ = 50 pF

| Symbol | Parameter | $T_C$ = –40°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $F_{max}$ | Toggle Frequency | 75 | | 75 | | 75 | | MHz | |

## PCC ECL-to-TTL AC Electrical Characteristics (Continued)

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, $C_L$ = 50 pF

| Symbol | Parameter | $T_C$ = –40°C | | $T_C$ = +25°C | | $T_C$ = +85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | $E_n$, $\overline{E}_n$ to $T_n$<br>(Transparent) | 1.70 | 4.90 | 1.70 | 5.10 | 1.80 | 5.80 | ns | *Figures 2, 4* |
| $t_{PLH}$<br>$t_{PHL}$ | LE to $T_n$ | 2.30<br>3.30 | 4.80<br>5.50 | 2.40<br>3.50 | 4.70<br>5.70 | 2.60<br>4.00 | 4.90<br>6.70 | ns | *Figures 2, 4* |
| $t_{PZH}$<br>$t_{PZL}$ | OE to $T_n$<br>(Enable Time) | 2.30<br>4.10 | 5.50<br>8.20 | 2.10<br>4.10 | 4.70<br>7.80 | 2.00<br>4.20 | 4.30<br>7.80 | ns | *Figures 2, 5* |
| $t_{PHZ}$<br>$t_{PLZ}$ | OE to $T_n$<br>(Disable Time) | 3.20<br>4.00 | 7.90<br>7.40 | 3.30<br>4.30 | 7.50<br>7.80 | 3.70<br>5.30 | 7.90<br>9.40 | ns | *Figures 2, 5* |
| $t_{PHZ}$<br>$t_{PLZ}$ | DIR to $T_n$<br>(Disable Time) | 2.00<br>2.10 | 6.60<br>4.70 | 1.90<br>2.00 | 5.70<br>3.70 | 1.70<br>1.90 | 5.20<br>3.70 | ns | *Figures 2, 6* |
| $t_S$ | $E_n$, $\overline{E}_n$ to LE | 0.50 | | 0.50 | | 0.50 | | ns | *Figures 2, 4* |
| $t_H$ | $E_n$, $\overline{E}_n$ to LE | 1.00 | | 1.00 | | 1.00 | | ns | *Figures 2, 4* |

## Military Version—Preliminary
## TTL-to-ECL DC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –55°C to +125°C, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | –1025 | –870 | mV | 0°C to +125°C | $V_{IN}$ = $V_{IH}$ (Max) or $V_{IL}$ (Min) | Loading with 50Ω to –2.0V | (Notes 12, 13, 14) |
| | | –1085 | –870 | mV | –55°C | | | |
| $V_{OL}$ | Output LOW Voltage | –1830 | –1620 | mV | 0°C to +125°C | | | |
| | | –1830 | –1555 | mV | –55°C | | | |
| | Cutoff Voltage | | –1950 | mV | 0°C to +125°C | OE or DIR Low | | |
| | | | –1850 | mV | –55°C | | | |
| $V_{OHC}$ | Output HIGH Voltage | –1035 | | mV | 0°C to +125°C | $V_{IN}$ = $V_{IH}$ (Min) or $V_{IL}$ (Max) | Loading with 50Ω 0 to –2.0V | (Notes 12, 13, 14) |
| | | –1085 | | mV | –55°C | | | |
| $V_{OLC}$ | Output LOW Voltage | | –1610 | mV | 0°C to +125°C | | | |
| | | | –1555 | mV | –55°C | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | V | –55°C to +125°C | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range | | (Notes 12, 13, 14, 15) |
| $V_{IL}$ | Input LOW Voltage | | 0.8 | V | –55°C to +125°C | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range | | (Notes 12, 13, 14, 15) |
| $I_{IH}$ | Input HIGH Current | | 70 | µA | –55°C to 125°C | $V_{IN}$ = +2.7V | | (Notes 12, 13, 14) |
| | Breakdown Test | | 1.0 | mA | –55°C to +125°C | $V_{IN}$ = +5.5V | | |
| $I_{IL}$ | Input LOW Current | –1.0 | | mA | –55°C to +125°C | $V_{IN}$ = +0.5V | | (Notes 12, 13, 14) |
| $V_{FCD}$ | Input Clamp Diode Voltage | –1.2 | | V | –55°C to +125° C | $I_{IN}$ = –18 mA | | (Notes 12, 13, 14) |

## Military Version—Preliminary
## TTL-to-ECL DC Electrical Characteristics (Continued)

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –55˚C to +125˚C, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| $I_{EE}$ | $V_{EE}$ Supply Current | | | | | LE Low, OE and DIR High | (Notes 12, 13, 14) |
| | | | | | –55˚C to | Inputs Open | |
| | | –165 | –65 | mA | +125˚C | $V_{EE}$ = –4.2V to –4.8V | |
| | | –175 | –65 | | | $V_{EE}$ = –4.2V to –5.7V | |

## ECL-to-TTL DC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, GND = 0V, $T_C$ = –55˚C to +125˚C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to + 5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | mV | 0˚C to +125˚C | $I_{OH}$ = –1 mA, $V_{TTL}$ = 4.50V | (Notes 12, 13, 14) |
| | | 2.4 | | | –55˚C | $I_{OH}$ = –3 mA, $V_{TTL}$ = 4.50V | |
| $V_{OL}$ | Output LOW Voltage | | 0.5 | mV | –55˚C to +125˚C | $I_{OL}$ = 24 mA, $V_{TTL}$ = 4.50V | |
| $V_{IH}$ | Input HIGH Voltage | –1165 | –870 | mV | –55˚C to +125˚C | Guaranteed HIGH Signal for All Inputs | (Notes 12, 13, 14, 15) |
| $V_{IL}$ | Input LOW Voltage | –1830 | –1475 | mV | –55˚C to +125˚C | Guaranteed LOW Signal for All Inputs | (Notes 12, 13, 14, 15) |
| $I_{IH}$ | Input HIGH Current | | 350 | µA | 0˚C to | $V_{EE}$ = –5.7V | (Notes 12, |
| | | | 500 | | +125˚C | $V_{IN}$ = $V_{IH(Max)}$ | 13, 14) |
| $I_{IL}$ | Input LOW Current | 0.50 | | µA | –55˚C to +125˚C | $V_{EE}$ = –4.2V $V_{IN}$ = $V_{IL(Min)}$ | (Notes 12, 13, 14) |
| $I_{OZHT}$ | 3-STATE Current Output High | | 70 | µA | –55˚C to +125˚C | $V_{OUT}$ = +2.7V | (Notes 12, 13, 14) |
| $I_{OZLT}$ | 3-STATE Current Output Low | –1.0 | | mA | –55˚C to +125˚C | $V_{OUT}$ = +0.5V | (Notes 12, 13, 14) |
| $I_{OS}$ | Output Short-Circuit Current | –150 | –60 | mA | –55˚C to +125˚C | $V_{OUT}$ = 0.0V, $V_{TTL}$ = +5.5V | (Notes 12, 13, 14) |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | 75 | mA | –55˚C to | TTL Outputs Low | (Notes 12, |
| | | | 50 | mA | +125˚C | TTL Output High | 13, 14) |
| | | | 70 | mA | | TTL Output in 3-STATE | |

**Note 12:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals –55˚C) then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up This provides "cold start" specs which can be considered a worst case condition at cold temperatures

**Note 13:** Screen tested 100% on each device at –55˚C +25˚C and +125˚C Subgroups 1 2 3 7 and 8

**Note 14:** Sample tested (Method 5005 Table I) on each manufactured lot at –55˚C +25˚C and +125˚C Subgroups A1 2 3 7 and 8

**Note 15:** Guaranteed by applying specified input condition and testing $V_{OH}/V_{OL}$

## TTL-to-ECL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, GND = 0V

| Symbol | Parameter | $T_C$ = –55˚C | | $T_C$ = +25˚C | | $T_C$ = +125˚C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PLH}$ $t_{PHL}$ | $T_n$ to $E_n$, $\overline{E}_n$ (Transparent) | 1.0 | 3.9 | 1.1 | 3.6 | 1.1 | 4.0 | ns | *Figures 1, 2* | (Notes 12, 13, 14) |
| $t_{PLH}$ $t_{PHL}$ | LE to $E_n$, $\overline{E}_n$ | 1.2 | 3.8 | 1.4 | 3.7 | 1.6 | 4.2 | ns | *Figures 1, 2* | |

## TTL-to-ECL AC Electrical Characteristics (Continued)

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, GND = 0V

| Symbol | Parameter | $T_C$ = –55°C | | $T_C$ = +25°C | | $T_C$ = +125°C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PZH}$ | OE to $E_n$, $\overline{E}_n$ (Cutoff to HIGH) | 1.0 | 4.3 | 1.5 | 4.4 | 1.7 | 5.2 | ns | *Figures 1, 2* | (Notes 12, 13, 14) |
| $t_{PHZ}$ | OE to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 1.5 | 5.1 | 1.6 | 4.5 | 1.6 | 5.1 | ns | *Figures 1, 2* | |
| $t_{PHZ}$ | DIR to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 1.6 | 4.7 | 1.6 | 4.3 | 1.7 | 4.9 | ns | *Figures 1, 2* | |
| $t_S$ | $T_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | (Note 15) |
| $t_H$ | $T_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | |
| $t_{PW}$(H) | Pulse Width LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 1, 2* | (Note 15) |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.4 | 2.3 | 0.5 | 2.1 | 0.4 | 2.4 | ns | *Figures 1, 2* | (Note 15) |

## ECL-to-TTL AC Electrical Characteristics

$V_{EE}$ = –4.2V to –5.7V, $V_{TTL}$ = +4.5V to +5.5V, GND = 0V, $C_L$ = 50 pF

| Symbol | Parameter | $T_C$ = –55°C | | $T_C$ = +25°C | | $T_C$ = +125°C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PLH}$ $t_{PHL}$ | $E_n$, $\overline{E}_n$ to $T_n$ (Transparent) | 2.3 | 6.4 | 2.4 | 5.6 | 2.6 | 6.3 | ns | *Figures 3, 4* | (Notes 12, 13, 14) |
| $t_{PLH}$ $t_{PHL}$ | LE to $T_n$ | 3.1 | 8.0 | 3.1 | 7.3 | 3.3 | 8.0 | ns | *Figures 3, 4* | |
| $t_{PZH}$ | OE to $T_n$ | 3.2 | 8.9 | 3.7 | 9.0 | 4.0 | 10.2 | ns | *Figures 3, 5* | (Notes 12, 13, 14) |
| $t_{PZL}$ | (Enable Time) | 3.6 | 9.4 | 4.0 | 9.3 | 4.3 | 10.4 | | | |
| $t_{PHZ}$ | OE to $T_n$ | 3.2 | 9.9 | 3.3 | 9.0 | 3.5 | 9.4 | ns | *Figures 3, 5* | |
| $t_{PLZ}$ | (Disable Time) | 3.0 | 9.7 | 3.4 | 8.8 | 4.1 | 10.6 | | | |
| $t_{PHZ}$ | DIR to $T_n$ | 2.6 | 9.4 | 2.8 | 8.8 | 2.9 | 9.1 | ns | *Figures 3, 6* | |
| $t_{PLZ}$ | (Disable Time) | 2.7 | 8.5 | 3.1 | 8.0 | 4.0 | 9.7 | | | |
| $t_S$ | $E_n$, $\overline{E}_n$ to LE | 2.5 | | 2.0 | | 2.5 | | ns | *Figures 3, 4* | (Note 15) |
| $t_H$ | $E_n$, $\overline{E}_n$ to LE | 3.0 | | 2.5 | | 3.0 | | ns | *Figures 3, 4* | |
| $t_{PW}$(H) | Pulse Width LE | 2.5 | | 2.0 | | 5.0 | | ns | *Figures 3, 4* | (Note 15) |

## Test Circuitry

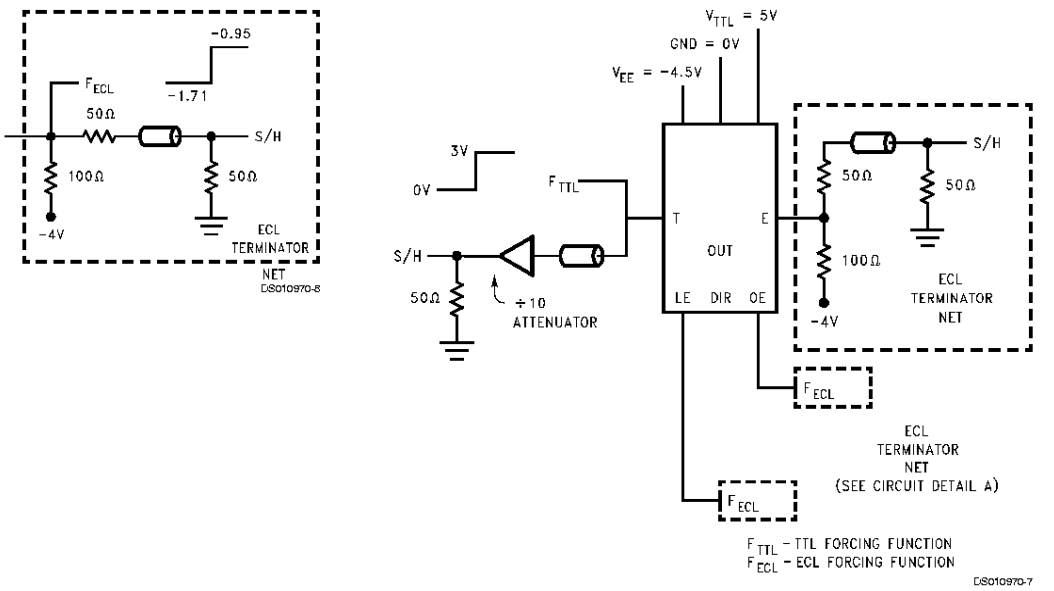
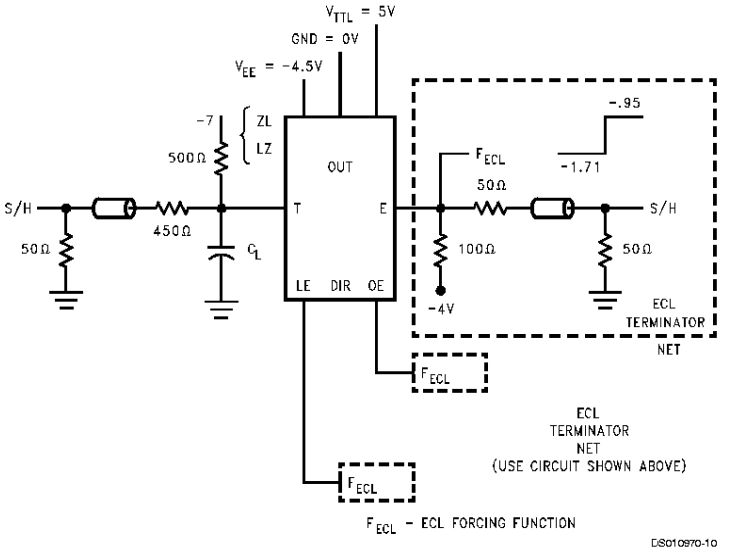



**FIGURE 1. TTL-to-ECL AC Test Circuit**




$C_L$ = 50 pF including stray and jig capacitance

**Note 16: Note:** 50Ω to ground termination **must be included** on ECL I/O pins **not** monitored by a 50Ω scope to prevent oscillatory feedback

**FIGURE 2. ECL-to-TTL AC Test Circuit**

## Switching Waveforms

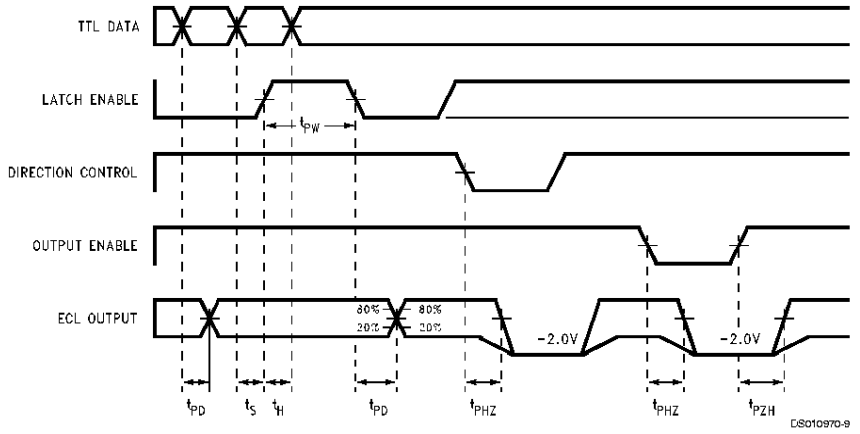
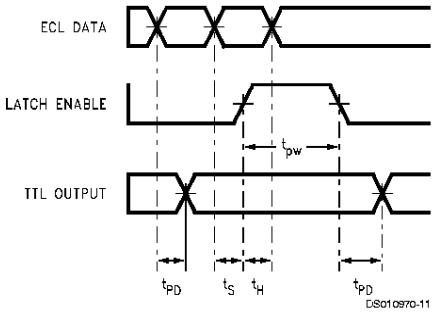
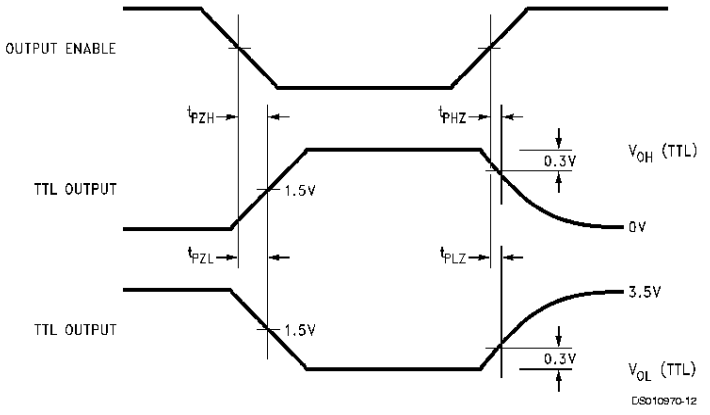



**FIGURE 3. TTL-to-ECL Transition—Propagation Delay and Transition Times**




**Note:** DIR is LOW and OE is HIGH

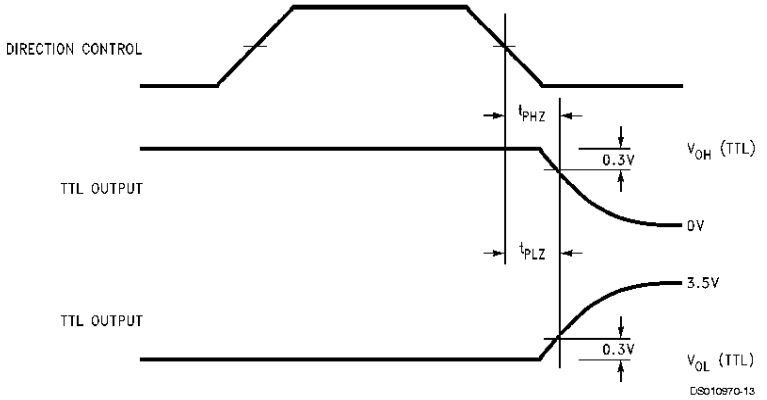
**FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times**




**Note:** DIR is LOW LE is HIGH

**FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times**

## Switching Waveforms (Continued)




**Note:** OE is HIGH LE is HIGH

**FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time**

## Applications

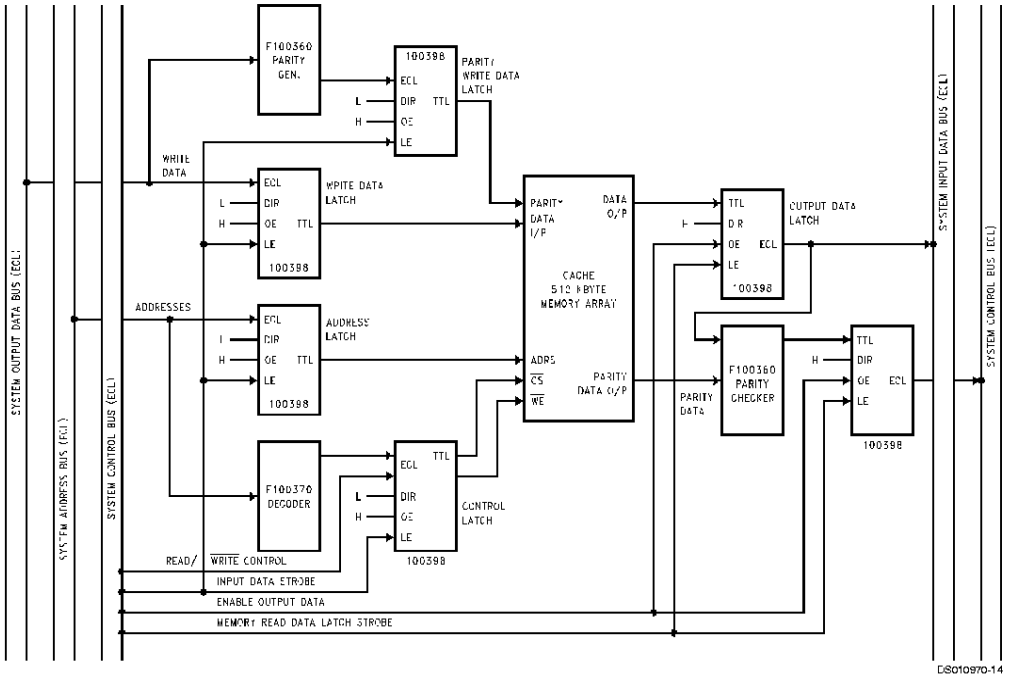
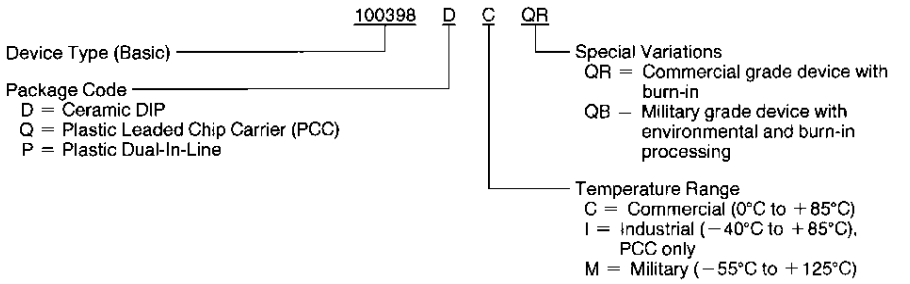



**FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100398 ECL–TTL Latched Translator**

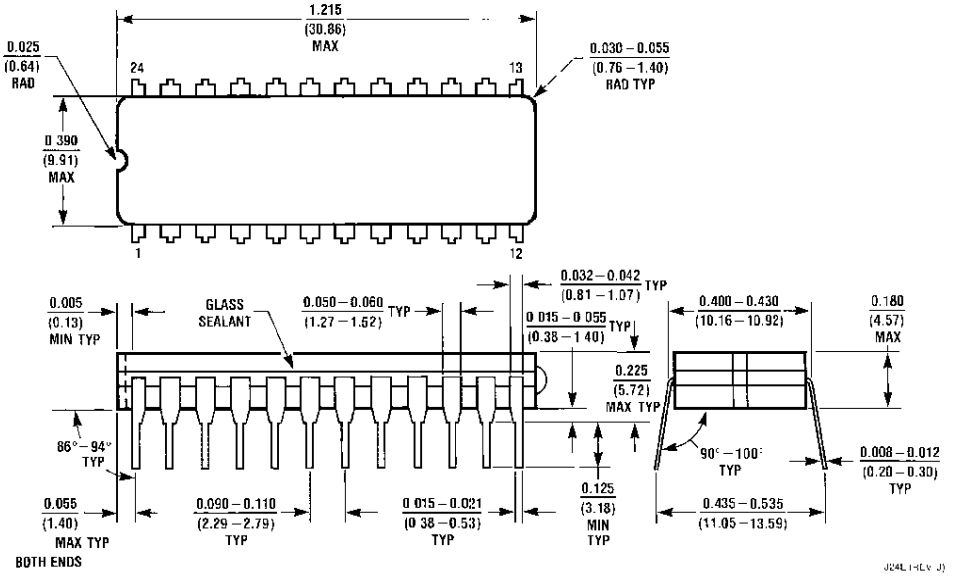
## Ordering Information

The device number is used to form part of a simplified purchasing code where A package type and temperature range are defined as follows:



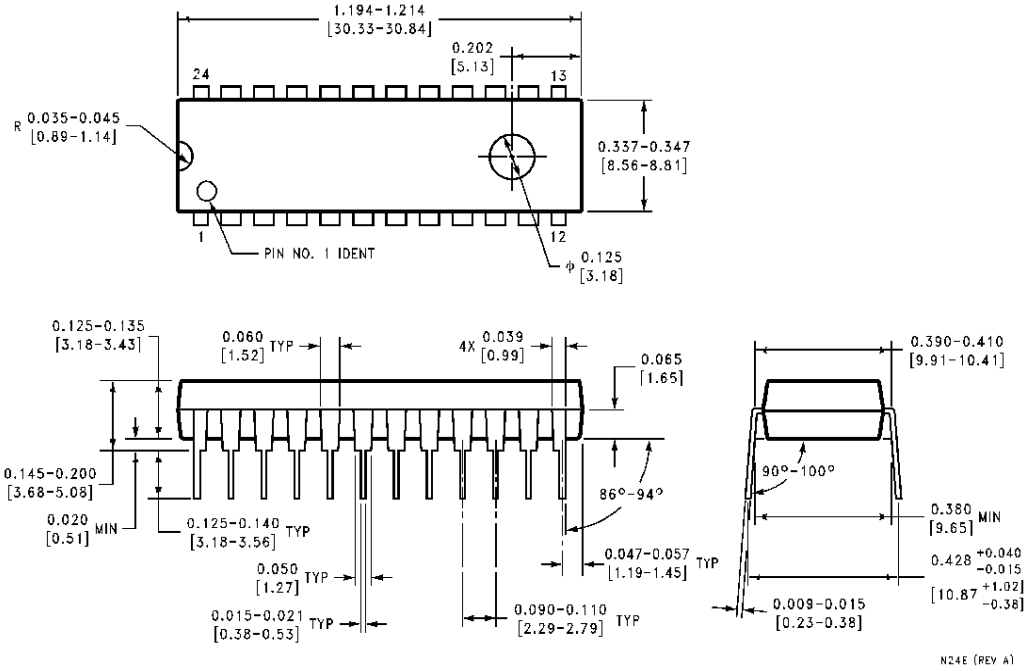

DS010970-15

## Physical Dimensions inches (millimeters) unless otherwise noted



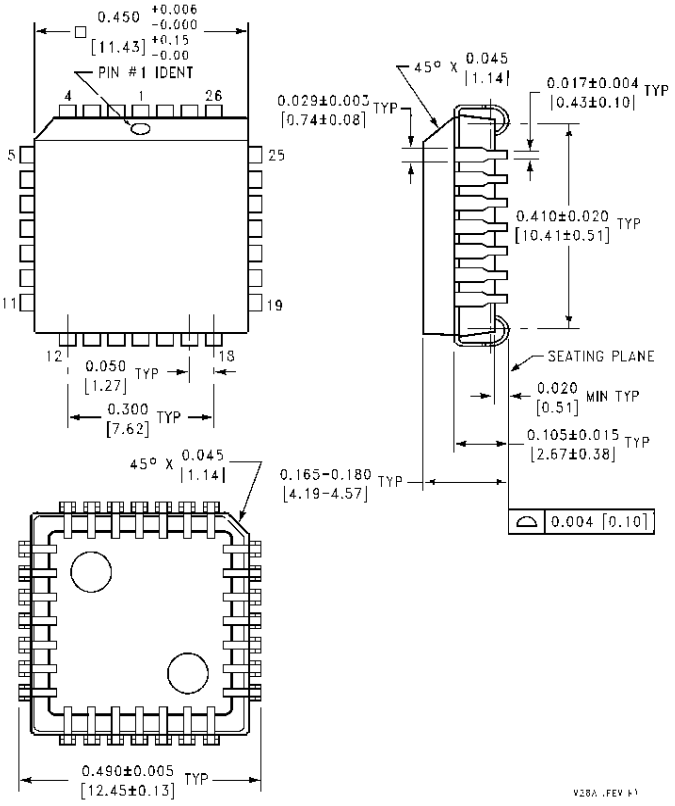

**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**
**Package Number J24E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Plastic Dual-In-Line Package (0.400" Wide) (P)**
**Package Number N24E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**28-Lead Plastic Chip Carrier (Q)**
**Package Number V28A**

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