Micro Linear

November 1995
PRELIMINARY

ML4878

ML4878 LCD Backlight Lamp Driver

GENERAL DESCRIPTION

The ML4878 is a controller IC for driving the miniature cold cathode fluorescent lamps (CCFL) typically used in liquid crystal display (LCD) backlight applications. It provides a high efficiency dimming control as well as fault protection for backlight applications.

The unique architecture of the ML4878 allows the implementation of a very low cost backlight inverter system. The single stage configuration uses only two external FET devices in a half bridge arrangement. The total bill of materials can be lower than for existing discrete inverters while resulting in considerably higher performance, more flexibility and control, and the addition of important safety features.

The ML4878 operates in a fixed frequency mode to eliminate interaction or beat frequency concerns typically found in variable frequency solutions. The optimum frequency of operation is set by the user.

A very high light output is achieved by driving the lamp in a differential configuration. This technique results in a much higher light output efficiency by reducing the loss due to the lamp and wiring parasitics.

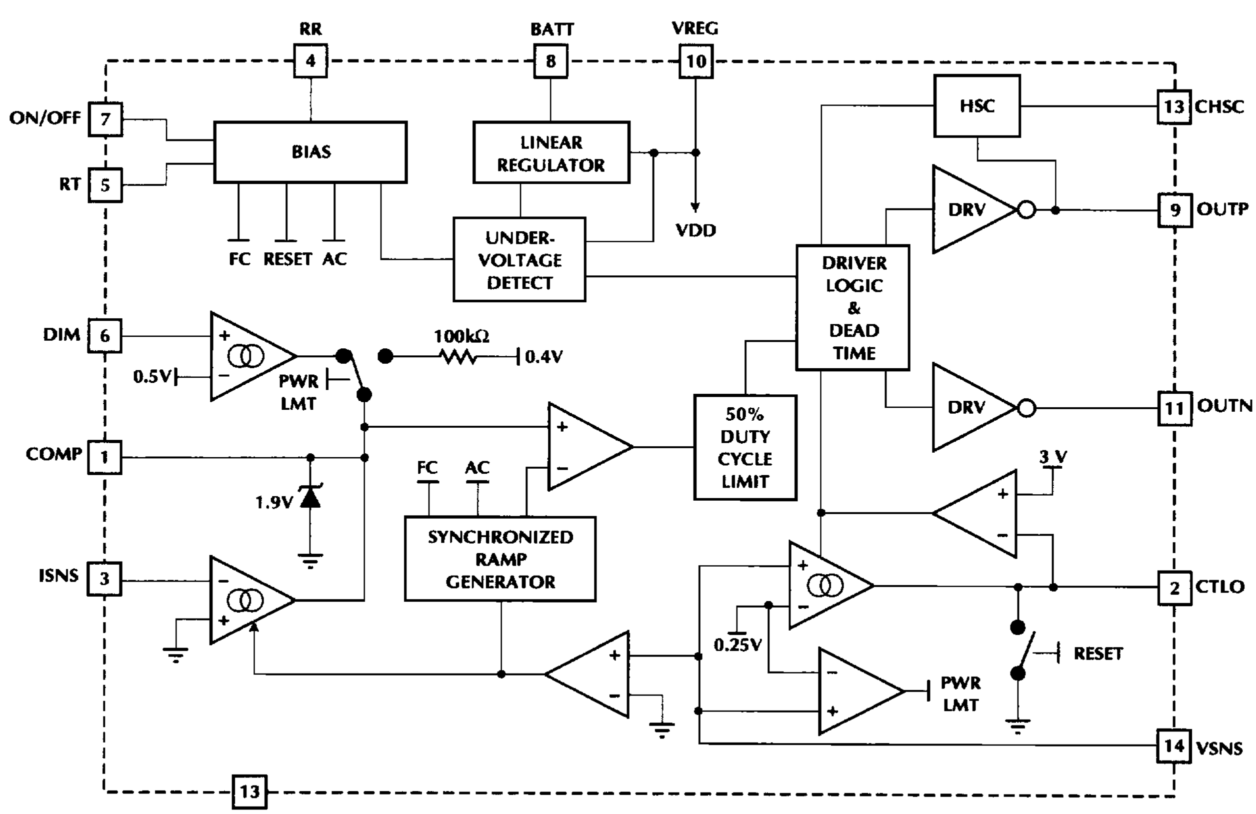
The ML4878 contains all the safety features necessary to implement an extremely reliable backlight lamp driver system that will easily meet UL requirements. The architecture of the ML4878 is inherently sturdy to faults and contains an adjustable, latching, lamp out detect circuit.

The ML4878 is available in a very small form factor 14 pin narrow SOIC package.

FEATURES

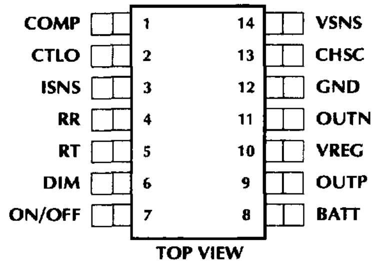
- Low cost LCD backlight driver solution
- High efficiency — 95% typical
- Differential lamp drive for increased light output
- Minimum external active component count — only 2 FET devices
- Lamp out detect with latch
- Inherent UL sturdiness
- Fixed frequency operation
- Operates down to 4.5 volts

BLOCK DIAGRAM



PIN CONFIGURATION

ML4878
14-Pin SOIC (S14N)



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	COMP	Compensation capacitor to ground sets the response of the duty-cycle control loop.
2	CTLO	Capacitor to ground sets the maximum time before a lamp out condition is detected.
3	ISNS	Lamp current sense input. Connects to the current sense resistor.
4	RR	A resistor to the battery voltage input adjusts the slope of the internal ramp voltage. It allows the circuit to track the changes in the battery input voltage level.
5	RT	Timing resistor. A resistor to ground sets the minimum slope of the internal ramp generator.
6	DIM	Voltage input to control the lamp brightness. Maximum brightness is achieved with 3V and minimum brightness (0), or off, with 0.5V. Can be driven directly with a PWM signal.
7	ON/OFF	Logic input to control whether the device is in the normal operating mode or in the power down, or off, mode. TTL compatible.
8	BATT	Battery power input to the IC. Input for on-chip linear regulator.
9	OUTP	P-channel MOSFET driver output.
10	VREG	DC output of on-chip linear regulator and power input for the on-chip circuitry. Nominally 6.0 volts.
11	OUTN	N-channel MOSFET driver output.
12	GND	Signal and power ground.
13	CHSC	Capacitor for high side driver input voltage transient correction.
14	VSNS	Lamp voltage sense input. Connects to voltage divider on primary of output transformer.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (BATT, VREG) 75mA
Output Current, Source or Sink (OUTN, OUTP) ... 250mA
Current into RT, RR .... ±1mA

Voltage on all pins except
BATT, RR .... –0.3V to VREG + 0.3V
Voltage on pin BATT 20V
Voltage on pin RR 23V
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering 10 Sec.) ....+260°C
Thermal Resistance (θ_{JA} Plastic SOIC 14) .... 105°C/W

OPERATING CONDITIONS

Temperature Range .... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

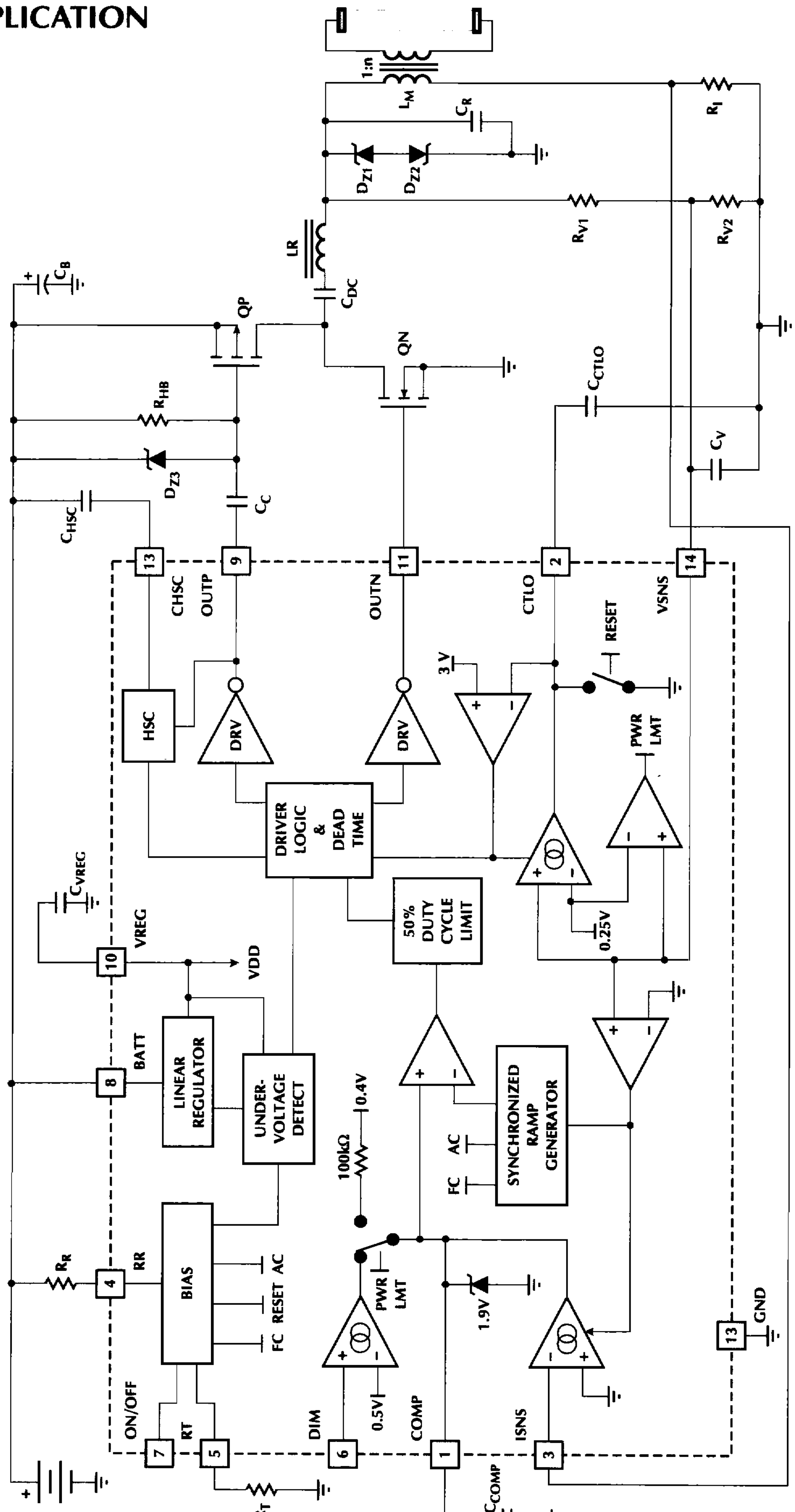
Unless otherwise specified, VREG = 6V ±5%, BATT = 12V ±5%, ON/OFF = "1", T_A = 0°C to +70°C, RT = 160KΩ, RR = 750KΩ, COMP = 10nF, CHSC = 1nF (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LAMP CONTROL SECTION (pins COMP, ISNS, DIM, VSNS)					
DIM Input Control Range	Minimum/Maximum Brightness	0.25		3.0	V
DIM Transconductance	VSNS = 0.15V, COMP = 1V	2.8	4	5.2	µA/V
DIM Input Offset Voltage	ISNS = 0	–100		100	mV
DIM Input High Voltage	Maximum Brightness	2.9	3.0	3.1	V
DIM Input Low Voltage	Minimum Brightness	0.4	0.5	0.6	V
ISNS Transconductance	DIM = 0.5V, COMP = 1V, Note 2	70	100	130	µA/V
DIM Gm/ISNS Gm Ratio	DC		25		
COMP Off Current	DIM = 0.5V, ISNS = –200mV, VSNS = 150mV, COMP = 1V	1			µA
COMP Clamp Voltage	ICOMP = 30µA, DIM = 3V	1.80	1.85	1.90	V
COMP Initial Voltage	VREG = 3.9V	300	330	360	mV
COMP Power Limit Voltage	VSNS = 300mV	390	400	410	mV
VSNS Zero Crossing Threshold hysteresis, Positive	DIM = 3V, ISNS = –200mV			20	mV
VSNS Zero Crossing Threshold hysteresis, Negative	DIM = 3V, ISNS = –200mV	–20			mV
VSNS Input Current			500		µA
OUTPUT DRIVER SECTION (pins OUTN, OUTP, CHSC)					
OUTN VOL	ISINK = 100mA, VREG = 6V			0.25	V
OUTP VOL	ISINK = 100mA, VREG = 6V			0.375	V
OUTN VOH	ISOURCE = 100mA, VREG = 6V	5.75			V
OUTP VOH	ISOURCE = 100mA, VREG = 6V	5.625			V
OUTN,OUTP Rise/Fall Time	C = 1nF		20	50	nS
OUTN, OUTP Dead Time	CTLO = 3.5V, CHSC = 0V,	100	150	200	nS
CHSC Min Low Pulse	OUTP = 0V, CTLO = 3.5V	350	500	650	nS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LAMP OUT DETECT SECTION (pins CTLO, VSNS)					
Lamp Out (VSNS) Detect Threshold	DIM = 3V, ISNS = 0V	225	250	275	mV
CTLO Sink/Source Current	CTLO = 0.5V	0.8	1.0	1.2	µA
CTLO Threshold		2.9	3.0	3.1	V
CTLO Reset Threshold		0.5	0.7	0.9	V
Lamp Out Detect Delay	CCTLO = 0.15µF		0.5		S
FREQUENCY, RAMP, AND LOGIC CONTROL SECTION (pins RR, RT, ON/OFF)					
Operating Frequency Range		20		100	KHz
Frequency Range Tolerance		–10		+10	%
Minimum Synchronization Frequency	RT = 160kΩ Nominal Network Frequency	–25			%
RT Voltage	RT = 160kΩ	1.95	2.00	2.05	V
RR Operating Voltage			0.7		V
ON/OFF VIH		2.0			V
ON/OFF VIL				0.8	V
ON/OFF Input Bias current	ON/OFF = 5V		5		µA
POWER SUPPLY, REGULATOR & UNDERVOLTAGE SECTION (pins BATT, VREG)					
BATT Supply Current	ON/OFF = "1", BATT = 18V, ILAMP = 0			1.5	mA
BATT Shutdown Current	ON/OFF = "0", BATT = 18V			10	µA
BATT Shutdown Current	ON/OFF = "0", BATT connected to VREG			100	µA
BATT Voltage Range		4.5		18	V
VREG Output Voltage	BATT = 18V, IVREG = 10mA	5.8	6.0	6.2	V
VREG Load Regulation	IVREG = 10mA, 0	–1		+1	%
VREG Line Regulation	BATT = 7V to 18V	–1		+1	%
VREG Dropout Voltage	BATT = 5V, IVREG = 10mA			300	mV
VREG Undervoltage Threshold (High to Low Transition)	BATT = VREG = ON/OFF	3.9	4.0	4.1	V
VREG Undervoltage Threshold Hysteresis	BATT = VREG = ON/OFF		330		mV

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
Note 2: The measured transconductance will be the specified number times the duty cycle, which is typically 50%.

TYPICAL APPLICATION



EXTERNAL COMPONENT SELECTION

This section is a reference guide for selecting the external components associated with the ML4878. Additional information, useful for optimizing the operation, can be found in the Functional Description section.

OUTPUT NETWORK (OUTP, OUTN pins)

The calculation of the values for the resonant inductor (LR), the resonant capacitor (CR), the DC blocking capacitor (CDC), and the turns ratio of the output transformer (To) is an iterative procedure. The values are derived by making some initial estimates, performing the calculations, checking the results, revising the estimates, and performing the calculations again. This process is repeated until satisfactory values of the components are achieved. The equations and procedure are shown below.

Choose or determine the appropriate values for the following:

f = Operating frequency

V_L = Lamp running voltage (RMS)

PL_{MAX} = Maximum lamp power

$BATT_{MIN}$ = Minimum battery voltage

η = Desired efficiency (be reasonable, try 95%)

A_L = Henrys/Turns^2 of Transformer

n_2 = # of turns on transformer secondary

k = Coupling coefficient of transformer

Lmp = Magnetizing inductance of the primary of the output transformer

Calculate these values:

n = Turns ratio of output transformer

n_1 = # of turns on primary of output transformer

LR = Resonant inductor

CR = Resonant capacitor

CDC = DC blocking capacitor

1. Calculate the turns ratio (n) and the # of turns on the primary (n1)

   Estimate values for the m and l constants.
   Try m = 5 and h = 3

$$m = \frac{C_{DC}}{C_R} \qquad h = \frac{L_{MP}}{L_R}$$

   Calculate n and n1

$$n = \frac{(1+h)\pi V_L}{BATT_{MIN}\, h\eta k\sqrt{2}\sqrt{1+\frac{1}{m}+\frac{1}{h}}} \qquad n_1 = \frac{n_2}{n}$$

2. Calculate Z_O and ω_O. (Z_O — Impedance of resonant network, ω_O — Angular resonant frequency of network.)

$$Z_O = \frac{V_L^2\eta}{n^2 P_{LMAX}} \qquad \omega_O = \frac{2\pi f}{\sqrt{1+\frac{1}{m}+\frac{1}{h}}}$$

3. Calculate component values.

$$L_R = \frac{Z_O}{\omega_O} \text{ Choose closest standard value}$$

$$C_R = \frac{1}{Z_O\omega_O} \text{ Choose closest standard value}$$

$$C_{DC} = mC_R \text{ Choose closest standard value}$$

4. Use the above values if they are close enough (less than the difference between standard values) to the values calculated during the previous iteration. If not calculate the values for m and h using the equations below and then go back to step 1.

$$m = \frac{C_{DC}}{C_R}$$

$$l = \frac{A_L n_1^2}{L_R}$$

The actual operating frequency will be given by the equation below.

$$f = \frac{\omega_O\sqrt{1+\frac{1}{m}+\frac{1}{h}}}{2\pi}$$

D_{Z1} and D_{Z2} — Zener Diodes

The breakdown voltage of these two zener diodes should be selected such that the total series voltage is about equal to the desired lamp striking peak voltage, plus tolerances, divided by the turns ratio (n) of the output transformer (T_O).

The circuit limits the maximum power to the zener diodes to about 1/5 of the maximum lamp power by controlling the duty cycle. Since this power is divided between two diodes each diode should be rated at about 1/10 of the maximum lamp power. This rating can be derated depending on the length of the lamp out detect delay. For example, with a lamp out detect delay of 0.5 seconds a typical power rating of the zener diodes can be derated by a factor of about 3 to 4 times. (Please refer to the time derating graph for your specific zener diode)

Another factor in selecting the power rating of the zener diodes is the time constant of the C_{COMP} capacitor. Maximum power could be delivered to the zener diodes during start-up transients on the COMP pin. This could be concern if the period of the time the power is applied is long enough. It is not an issue with the typical recommended value of C_{COMP} of 10nF since this value of capacitor yields a time of about 1ms time and the derating factor on the zener diodes for power applied during 1ms is about 25 to 30 times. A time calculation for a chosen value of C_{COMP}, and the resulting derating factor, should be performed when using larger values of C_{COMP}. The equation for the time calculation is given below.

$$\Delta t = 80k(C_{COMP})$$

D_{Z3} and R_{HB} and CC (OUTP pin)

The breakdown voltage of D_{Z3} should be roughly equal to the voltage on the VREG supply pin. If the zener voltage is selected too low, excessive current may flow in the CC capacitor increasing the losses. The value of the CC capacitor should be selected to be much larger than (> 10 times) the gate capacitance of the PMOS output FET. The RHB resistance can then be calculated from the following equation.

$$R_{HB} = 20M\Omega\left(\frac{C_{HSC}}{C_C}\right)$$

R_T resistor (RT pin) — Typical Value = 160KΩ

The resistor connected to the RT pin sets the minimum slope of the internal ramp voltage and the optimum frequency operating point. The actual frequency of operation is set by the external output network. The voltage at this pin is equal to 2V nominally. The resistor can be calculated by the equation below.

$$RT = \frac{8 \times 10^6}{f(KHz)}$$

R_R Resistor (RR pin) — Typical Value = 750KΩ

Resistor to the battery voltage input adjusts the slope of the internal ramp voltage. The slope of the internal ramp affects the operation of the circuit to input battery voltage changes. The proper value of RR sets the optimum response to input voltage changes. This optimum value of RR will minimize voltage changes at the COMP pin with changes in input battery voltage. In addition, it sets the duty cycle limit for high input voltages to limit the output power.

For optimum results the current into this pin should be equal to the current out of the RT pin at the minimum battery voltage. The value of RR can be calculated from the equation below.

$$RR = \frac{(BATT_{MIN} - 0.7)\,RT}{2}$$

C_{COMP} Capacitor (COMP pin) — Typical Value = 10nF

A capacitor to ground provides compensation for the duty-cycle control loop. It's value is not critical but should be about 10nF for typical applications. 10nF gives about a 1ms response which is adequate for most applications. Values greater than 50nF may not be completely initialized during the IC's start-up sequence, and the lamp might undergo two striking events during start-up which would be detrimental for lamp life. The IC's initialization sequence initializes the voltage on this capacitor to 300mV.

C_{CTLO} Capacitor (CTLO pin) — Typical Value = 0.33µF

A capacitor to ground programs the maximum amount of time that the circuit can be in the over voltage or striking mode. The charge and discharge current is 1uA and the part latches off when the pin's voltage exceeds 3V. A 0.33µF capacitor on this pin to ground will allow the part to strike for 1 second before the lamp is assumed to be malfunctioning and the IC turns off. If a capacitance larger than 1µF is used, the ON pin must stay low for a time longer than 40µs while VREG is still above 2V to ensure the circuit will reset properly.

$$C_{CTLO} = T_{DELAY}\,(0.3\mu F)$$

R_I Resistor (ISNS pin) — Typical Value = 0.33Ω

Lamp current sense resistor. An average voltage of 200mV on this resistor corresponds to full power; i.e. 3V on the DIM pin. Because of the small value of the resistor it is very important that it has a separate ground return to the IC and it be placed physically close to the IC pin. Voltage drops between the resistor and the IC pin connection will cause a degradation in the lamp current control accuracy. The value may be calculated by the following equation.

$$R_I = \frac{0.2V_L}{P_L nk}$$

where:

V_L = Lamp Running Voltage
P_L = Lamp Power
n = Output Transformer (TO) Turns Ratio
k = Coupling Coefficient of Transformer

C_{VREG} Filter Capacitor (VREG pin) — Typical Value = 1µF

A capacitor to ground filters the output of the on-chip linear regulator. This pin supplies the power for the internal circuits on the ML4878.

C_{CHSC} capacitor (CHSC pin) — Typical Value = 1nF

The capacitor of 1nF on this input will sense battery voltage surges and protect the high side driver from malfunctioning. This capacitor should always be less than 10nF.

R_{V1} and R_{V2} Voltage Divider Resistors and C_V (VSNS pin)

The ratio of these resistors sets the detect threshold for the lamp out function. The total source impedance seen at the VSNS pin should be 10kΩ or less. Higher values of source impedance will lower the bandwidth of this input. The ratio of the values should be chosen to ensure that sufficient signal is present at the VSNS pin to detect the zero crossings while also detecting lamp out conditions at the appropriate output voltage. The zero crossings are detected at 0 volts with ±10mV of hysteresis for noise rejection. The lamp out detect level should be set at a value somewhat less, to account for tolerances, than the total zener diode clamp network breakdown voltage (D_{Z1} + D_{Z2}). The lamp out threshold at the VSNS pin is set at 250mV nominally. The resistors may be calculated from the following equations.

$$R_{V1} = \frac{(V_{STRIKE} - V_{TOL})\,40K}{n}$$

$$R_{V2} = \frac{1}{\frac{1}{10K} - \frac{1}{R_{V1}}}$$

OR

Choose RV2 = 10kΩ

then RV1 can be calculated from the equation above.

The value of CV should be selected such that the cutoff (–3dB) frequency from CV and the source impedance of RV1 and RV2, is much larger that the operating frequency.

FUNCTIONAL DESCRIPTION

The ML4878 utilizes a voltage fed, half-bridge, duty cycle controlled topology. This type of architecture results in a highly efficient, low cost backlight lamp driver circuit. Some of the elements that contribute to the high efficiency are: a single stage configuration (only two active devices in the power path), resonant technology, and zero voltage switching. The low cost is realized because the single stage architecture yields a very low system parts count, and therefore low total system cost.

LAMP CONTROL

The control loop for the ML4878 consists of current sense and DIM input transconductance amplifiers, the voltage sense comparator, the ramp generator, the duty cycle limit, and drivers and drive logic. The lamp current is sensed in the primary of the output transformer via the voltage across a series resistor. The current in the primary will be directly proportional to the lamp current. This voltage is converted to a current in the ISNS transconductance amplifier. The output of this amplifier is modulated on and off by the comparator that senses zero crossings at the VSNS pin. This sampling rectifies the ac signal and cancels error-currents in the lamp current sense resistor due to the transformer's magnetizing inductance. The switching current output is subtracted from the current output of the DIM transconductance amplifier and then averaged by the capacitor connected to the COMP pin. This DC voltage is compared to a 50% duty cycle ramp voltage. The higher the DC voltage slices the ramp the larger the duty cycle. A larger duty cycle delivers more power to the output network and therefore more lamp current.

The DC voltage on the DIM input sets the absolute value of the lamp current. 3 volts on this pin will give full brightness. 0.5 volts will be minimum brightness, or off. In between these two points the control is mostly linear with 50% brightness at about 1.75 volts. The control loop will regulate the duty cycle to maintain the current at this setting. The DIM input transconductance is matched to the transconductance of the ISNS input to within a few percent, even thought the absolute value of the transconductance can vary by as much as ±30%.

A voltage of 3V or more on the DIM pin will cause 10uA to be sourced at the COMP pin. 0.5V or less on this pin will cause 1uA to be sunk at the COMP pin. The transconductance amplifier will not provide more current above 3 volts or less current below 0.5V. The input can therefore be driven directly with digital PWM signals because the voltage will automatically be integrated on the capacitor connected to the COMP pin.

The circuit operates in a fixed frequency mode over the majority of its operating range. The frequency of operation is set by the value of RT and by the resonant frequency of the output network. The control loop is prevented from operating at more than a 50% duty cycle. If the feedback dictates the circuit to operate at more than 50% duty cycle it will not increase further but instead enter a frequency mode. Increased load demands will be satisfied with a lowering of the operating frequency which will allow more power to be delivered to the lamp. Under normal circumstances the external components should be selected such that the ML4878 does not enter the frequency mode of operation. Variable frequency operation will complicate the filtering requirements and introduce the possibility of interaction or beat frequency problems with other signals in the system.

OUTPUT DRIVERS

The output circuit operates in a push-pull configuration, that is, the two output devices alternate turning on. The drive signals at OUTN and OUTP are actually in phase but the circuit will operate push-pull since the two output MOSFETs are of opposite polarity. The turn on of each output device is controlled to prevent cross-conduction. The two MOSFET output drivers are designed to drive one N-Channel and one P-Channel device. They are active pull up and active pull down. The drivers can handle 3nF loads, and have larger pull-up devices to handle any Miller currents entering the driver from high dv/dt on the drain of the external devices.

The high side driver has additional circuitry to compensate for voltage surges on the battery. This high side correction circuit senses the voltage on the CHSC pin through a capacitor connected to the battery input. Any sudden positive changes in voltage larger than approximately 1.5V on the battery will initiate a 500ns reset pulse to the high side driver. This pulse will cause the OUTP pin to go high for the this 500ns to ensure the high side MOSFET will stay in the off state to avoid cross conduction current flow in the output MOSFETs.

LAMP OUT DETECT

The ML4878 contains a lamp out detect circuit that will latch the circuit in the off state upon detection of a failed or open lamp connection. It has an adjustable time delay set by the value of the capacitor on the CTLO pin. This capacitor will set the maximum amount of time that the ML4878 will be in the over voltage or striking mode. A voltage of more than 0.25 volts nominal on the VSNS pin will initiate the charging of the capacitor on the CTLO pin. This capacitor is charged and discharged with a constant current of 1µA nominal. Once the voltage on the CTLO pin rises to approximately 3 volts the latch is set and the circuit enters a very low power state.

The lamp out detect circuit can be reset by either taking the ON/OFF-pin low momentarily or taking VREG below 4V nominally. Either of these will reset the latch, discharge the capacitor, and start a new striking sequence. If a capacitor larger than 1µF is used on CTLO the ON/OFF pin must be held low for at least 50µs while the voltage on VREG is above 2.0 volts to ensure that the capacitor will discharge and the circuit reset.

The latching mechanism operates with hysteresis on the 3V comparator. To reset the hysteresis, the CTLO pin must be taken to about 0.7 volts. To minimize the effect of the time-out feature, a small value (approx. 0.015µF) CCTLO capacitor may be used resulting in a very short delay of about 50ms. A minimum time delay of at least 10–20ms is necessary for proper operation of the circuit.

FREQUENCY, BIAS, AND LOGIC CONTROL

The bias circuit block contains the circuitry to set the frequency, the slope of the internal ramp voltage, and the on/off control for the chip. The minimum slope of the internal ramp voltage is set by the value of the resistor connected to the RT pin. This minimum slope, in conjunction with the external resonant network determines the nominal frequency of operation. The slope of this internal ramp voltage is adjusted by the value of the resistor connected to the RR pin. The slope of the ramp voltage determines the response to input voltage changes via the internal feedback loop that controls the lamp current. The proper value of RR will optimize the loop response to minimize the voltage changes seen on the COMP pin, and therefore minimize lamp current changes, due to battery voltage changes.

The value of the resistor connected to RR also sets the maximum duty cycle to limit the power at high battery voltages.

For optimum results, the current into the RR pin should be equal to the current out of the RT pin at minimum battery input voltage.

The ON/OFF input controls the operating mode of the ML4878. It operates by controlling the main biasing for the chip. With a logic "1" applied to the ON/OFF pin the circuit is in the normal, or operating, mode. With a logic "0" at this pin the device will be in a very low power shutdown mode. In this low power mode the oscillator is not running and the OUTP output is held high and the OUTN output is held low to ensure that the both of the output MOSFETs stay in the off state.

The threshold for the ON/OFF pin is TTL compatible. Floating the pin will turn the part off. A rising edge on the ON/OFF pin initializes a start-up sequence that resets the logic and initializes the voltages on the capacitors attached to the COMP and CTLO pins. The on off function of the IC can be disabled by connecting this pin to the BATT input.

POWER SUPPLY, REGULATOR & UNDERVOLTAGE DETECT

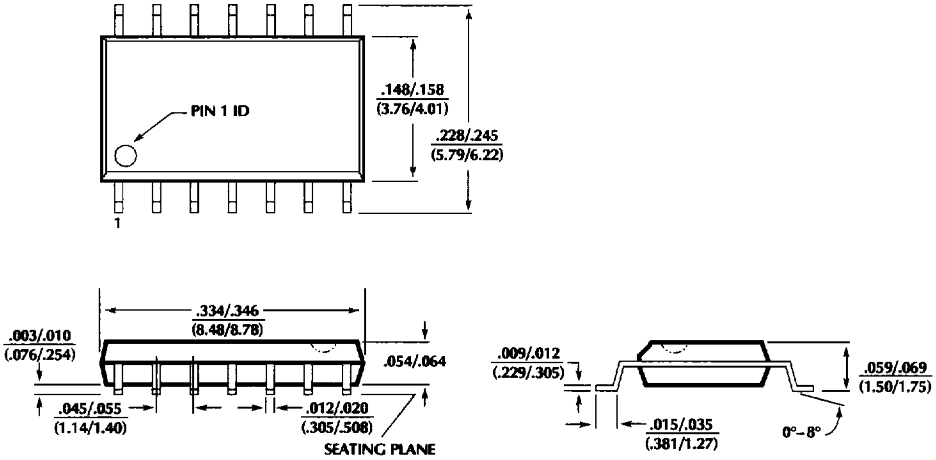
The power for the ML4878 is supplied by the battery voltage connected to the BATT input. This voltage is regulated by an on-chip, low drop out (LDO) linear regulator. The output of the LDO is nominally 6 volts and appears at the VREG pin. The output of the regulator has some capability to drive external circuits as defined in the electrical characteristics but is primarily intended to supply a regulated voltage for the circuits contained on the chip.

When the battery voltage drops below 6 volts the on-chip linear regulator ceases to regulate and enters a linear mode. The circuit will continue to operate properly down to the specified minimum with the VREG voltage tracking the battery voltage minus the drop out voltage of about 200mV. If a regulated 5 volt supply is available to power the IC the BATT input may be connected to the VREG pin to avoid the 0.2 volt nominal drop-out, but a it will result in an increase in the shutdown current.

The under voltage detect circuit block monitors the output of the linear regulator and detects an under voltage condition if this voltage drops below about 4 volts. There is about 330mV of hysteresis on this threshold so the low to high threshold transition will be higher by this amount. When an undervoltage condition is detected the internal oscillator is disabled and the output power goes to zero.

PHYSICAL DIMENSIONS inches (millimeters)

Package: S14N
14-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4878	0°C to +70°C	14-PIN SOIC (S14N)

2092 Concourse Drive
San Jose, CA 95131
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Micro Linear

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