Contents

CONTROLLER FOR REFLECTING ECB COLOR LCD S-4581A

The S-4581A is a medium-sized, simple dot matrix type LCD display controller for graphics display.
It can interface with an 8-bit MPU having a READY ($\overline{\text{WAIT}}$) input pin and accesses the VRAM by the cycle steal method so that the display screen is not disturbed. It contains all address/data control circuits for cycle stealing, so it does not require any external circuits. Since it has chip select output pins for the VRAM, it can be connected directly with eight 64K SRAMs or two 256K SRAMs without using an external decoder circuit.
Since the VRAM is mapped on the MPU memory, all display data can be addressed directly by the MPU and display data processes, such as drawing, can be performed quickly and efficiently.
The S4581A provides two display modes: 4- and 8-gradation display modes. When all 64KB of the VRAM are used, the maximum number of dots for display image data is 262,144 in the 4-gradation display mode and 131,072 in the 8-gradation display mode.

■ Features

- Can be controlled by an 8-bit (Intel) MPU.
- Can interface with an MPU with a READ ($\overline{\text{WAIT}}$) signal.
- The MPU accesses the VRAM by the cycle steal method.
  ⇒It does not affect the display screen.
- VRAM
  Mapping: MPU memory space
  Capacity: 64K bytes (2^{16})
- LCD display mode
  4- and 8-gradation display modes
- LCD panel
  Single-screen drive panel (4-bit data transfer)
- Maximum horizontal display width: 1024 dots (gradation display mode)
- Maximum number of vertical lines: 1024
- Maximum display screen (4-gradation mode and frame frequency 200 Hz)
  320 × 240 dots
- Vertical smooth scrolling is possible.
- VRAM chip select output pin
- CMOS operation
- Operating power supply voltage: 5 ± 0.5 V
- S-4581AF: 80-pin QFP
  (Pin pitch: 0.8 mm)

This product is tentative yet therefore specifications may be changed without notice.

■ Cautions

1. DO NOT apply a voltage or current that exceeds the absolute maximum ratings to terminals. If applied, the IC may malfunction or be destroyed.
   The standard values are set with sufficient margins, but use the IC within the recommended operating conditions to optimize device quality.
2. Measures against static electricity
   2.1 When transporting or storing ICs, use conductive containers or metal coated boxes.
   2.2 Check that there is no current leakage in electrical facilities, and be sure to ground them. Also ensure that workbenches and people who handle ICs are grounded.
3. Excessive external noise to the power supply or I/O terminals of CMOS ICs causes latch-up, leading to faults and damage. If latch-up has occurred, immediately turn off the device, eliminate the cause, and turn on the device again.
4. Keep the IC away from mechanical vibration, shock, and sudden changes in temperature. These may cause wires to break.
5. Environment
   5.1 Use and store ICs below the absolute maximum rated temperature.
   5.2 DO NOT use or store ICs where condensation can occur.
   5.3 DO NOT use ICs where they are directly exposed to dust, salt, or acid gas such as SO_2. These may cause leaks between element leads and cause corrosion.
   5.4 To store ICs for a long time, DO NOT process them. During storage, DO NOT apply any load to ICs.

■ Pin Description

External dimensions (Unit: mm)

S-4581AF: 80-pin QFP

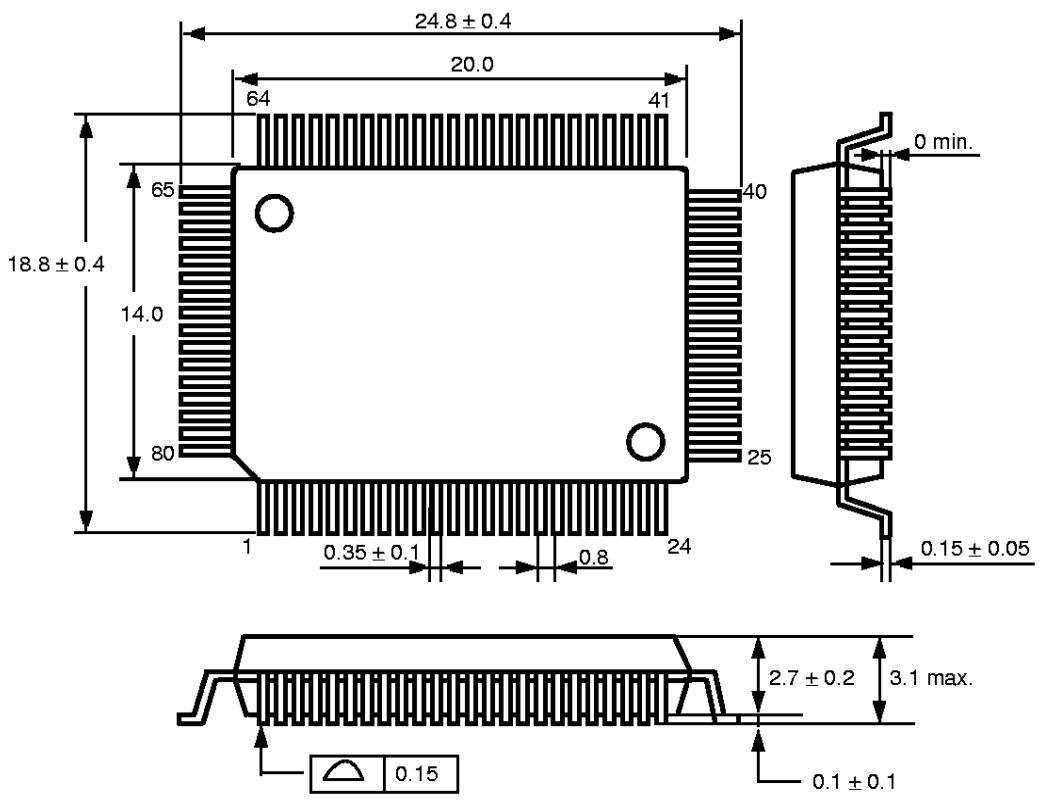


Figure 1-1 External Dimensions

■ S-4581A Pin Layout

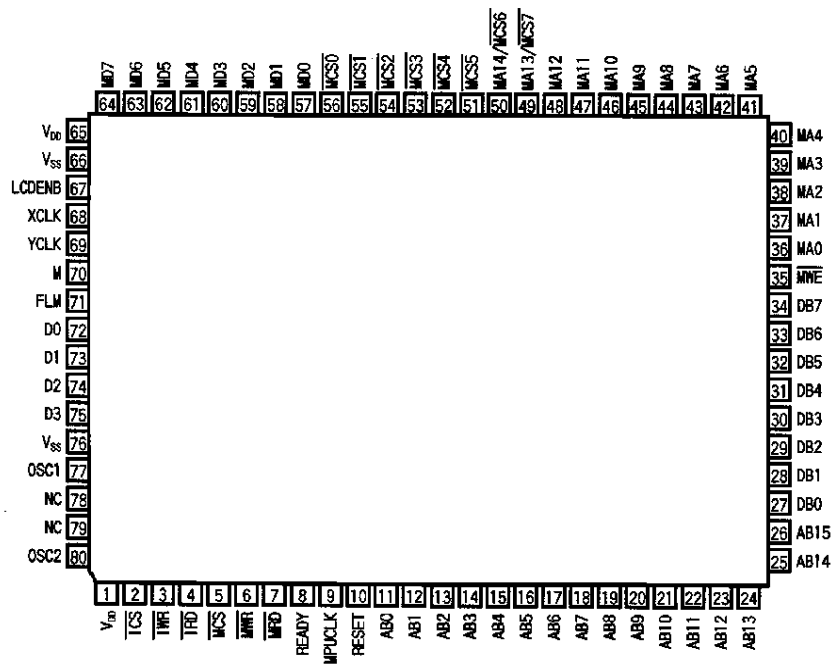


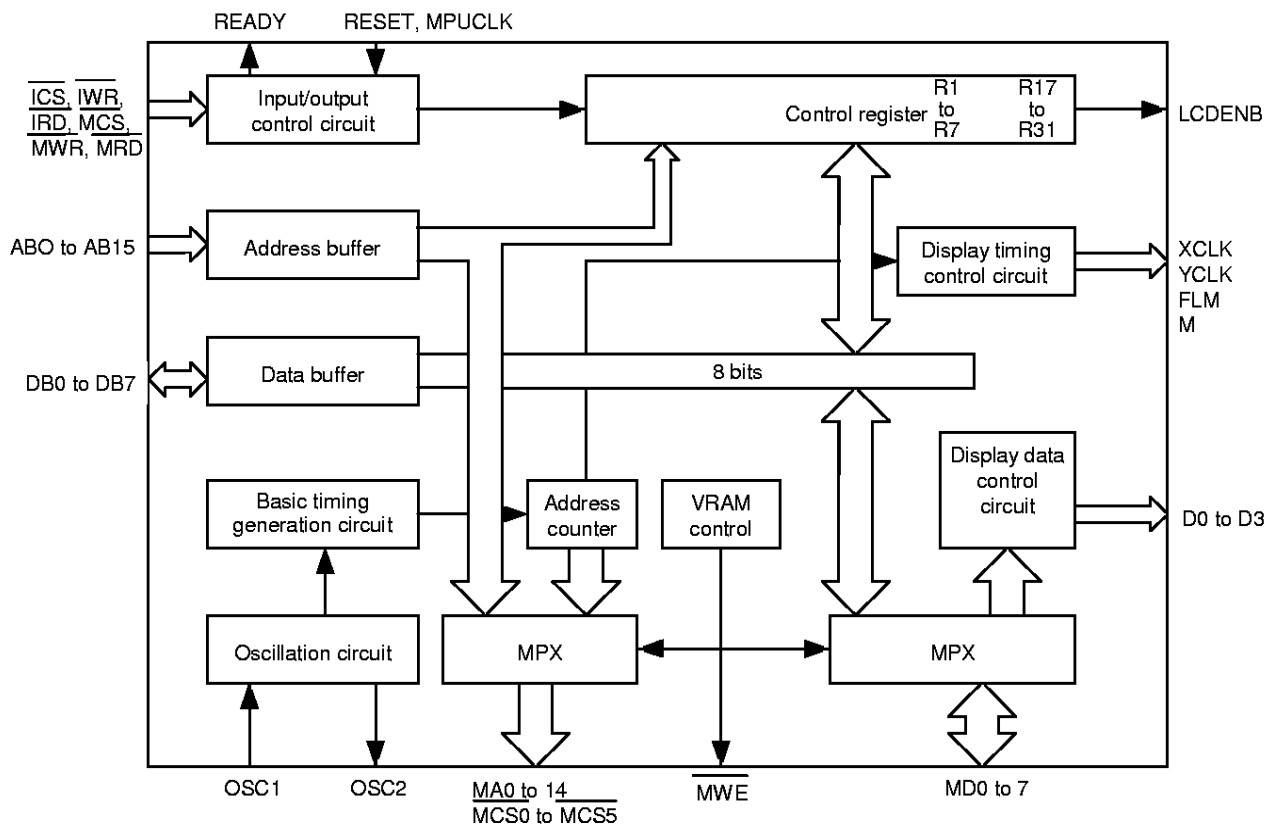
Figure 1-2 Pin Layout

■ Pin Functions

66, 76	VSS	Negative power supply pin Ground pin
1, 65	VDD	Positive power supply pin Normally connected to +5V.
2	$\overline{\text{ICS}}$	MPU interface select signal input pin Low: Active
3	$\overline{\text{IWR}}$	MPU interface write signal input pin Low: Active
4	$\overline{\text{IRD}}$	MPU interface read signal input pin Low: Active
5	$\overline{\text{MCS}}$	VRAM chip select input pin Low: Active
6	$\overline{\text{MWR}}$	VRAM write signal input pin Low: Active
7	$\overline{\text{MRD}}$	VRAM read signal input pin Low: Active
8	READY	MPU wait signal output pin CMOS output A low signal is output at a falling edge of the $\overline{\text{ICS}}$ or $\overline{\text{MCS}}$ signal. After internal processing ends, a high signal is output at a rising edge of MPUCLK. This pin may be connected directly to the $\overline{\text{WAIT}}$ pin of the MPU to wait the MPU.
9	MPUCLK	MPU clock signal input pin
10	RESET	Reset signal input pin Input the MPU RESET signal. The pulse width must to be 1μsec or more. ・ Command initialization/Internal register initialization R1: Initialization described later R2 to R7: All zeros R14, R15, R17, R18, R19: All zeros R21 to R31: All zeros R20: All ones
11 to 26	AB0 to AB15	MPU address bus input pin ・ Address setting at command input AB0=A0 : : : : AB4=A4 ・ VRAM address setting AB0=MA0 : : : : AB15=MA15 Note: If the address signal is multiplexed, latch and input it.
27 to 34	DB0 to DB7	MPU data bus input/output pin
35	$\overline{\text{MWE}}$	VRAM write enable output pin. Low: Active Output a write signal to the VRAM. Connect to the VRAM $\overline{\text{WE}}$ pin.
36 to 48	MA0 to MA12	VRAM address bus output pin
49 to 51	MA13/ $\overline{\text{MCS7}}$ to MA14/ $\overline{\text{MCS6}}$	VRAM address bus output VRAM chip select signal output pin ・ VRAM chip select signal output pins when 64K SRAM is selected MA13/$\overline{\text{MCS7}}$=$\overline{\text{MCS7}}$ MA14/$\overline{\text{MCS6}}$=$\overline{\text{MCS6}}$

		• VRAM address bus output pins when 256K SRAM is selected MA13/$\overline{MCS7}$=MA13 MA14/$\overline{MCS6}$=MA14
52 to 56	$\overline{MCS5}$ to $\overline{MCS0}$	VRAM chip select signal output pin
		• VRAM chip select signal output pin when 64K SRAM is selected $\overline{MCS5}$=$\overline{MCS5}$ $\overline{MCS4}$=$\overline{MCS4}$ $\overline{MCS3}$=$\overline{MCS3}$ $\overline{MCS2}$=$\overline{MCS2}$ $\overline{MCS1}$=$\overline{MCS1}$ $\overline{MCS0}$=$\overline{MCS0}$
		• VRAM address bus output pins when 256K SRAM is selected $\overline{MCS5}$=Unused $\overline{MCS4}$=Unused $\overline{MCS3}$=Unused $\overline{MCS2}$=Unused $\overline{MCS1}$=$\overline{MCS1}$ $\overline{MCS0}$=$\overline{MCS0}$
57 to 64	MD0 to MD7	VRAM data bus input/output pins Connect these pins to the VRAM data bus.
67	LCDENB	The LCD Enable mode setting command setting specified by D6 is output. The LCD pin goes low at reset.
68	XCLK	Display data transfer clock output pin Read display data D0 to D3 into the driver at a falling edge of XCLK.
69	YCLK	Display data latch signal output pin The clock for transferring display data latch signal and operation signal is input to the LCD driver IC. The signal is output after the data for one line for the display panel is transmitted. Transfer the display latch and operation signals at a falling edge of YCLK.
70	M	AC drive signal output pin
71	FLM	Frame start line output pin The common drive IC reads a high output signal from FLM at a falling edge of the YCLK signal. The FLM output has a 2-line return line period for the specified common count of the display panel, and the time of one frame is +2 lines.
72	D0	Display data output pin. 4-bits D0 to D3 are output in parallel to the LCD drive IC.
73	D1	
74	D2	
75	D3	
77	OSC1	Oscillation input pin External clock input pin
78	NC	
79	NC	
80	OSC2	Oscillation output pin Open when an external clock is input

■ Block Diagram



VRAM Address Assignment (1) (When 64K SRAM is used)

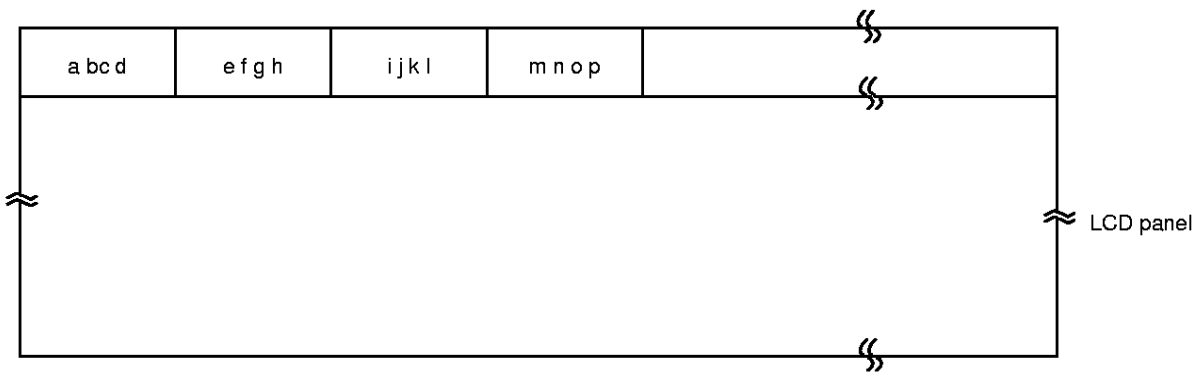
VRAM / S-4581A	VRAM pin: Address bus	VRAM pin: Chip select	Memory mapping
MA0	A0		
MA1	A1		
MA2	A2		
MA3	A3		
MA4	A4		
MA5	A5		
MA6	A6		
MA7	A7		
MA8	A8		
MA9	A9		
MA10	A10		
MA11	A11		
MA12	A12		
MA13 / $\overline{MCS7}$		$\overline{MCS7}$	E000H to FFFFH
MA14 / $\overline{MCS6}$		$\overline{MCS6}$	C000H to DFFFH
$\overline{MCS5}$		$\overline{MCS5}$	A000H to BFFFH
$\overline{MCS4}$		$\overline{MCS4}$	8000H to 9FFFH
$\overline{MCS3}$		$\overline{MCS3}$	6000H to 7FFFH
$\overline{MCS2}$		$\overline{MCS2}$	4000H to 5FFFH
$\overline{MCS1}$		$\overline{MCS1}$	2000H to 3FFFH
$\overline{MCS0}$		$\overline{MCS0}$	0000H to 1FFFH

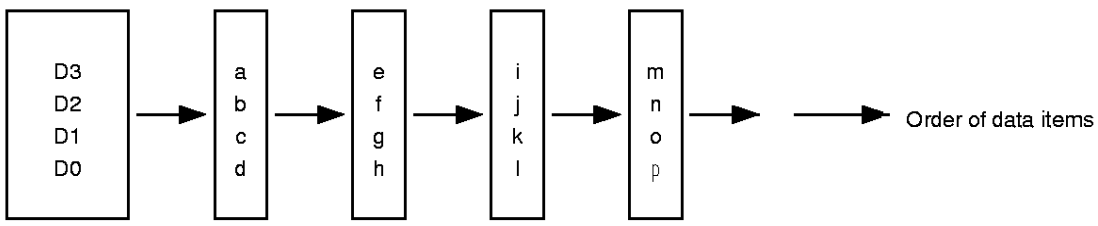
VRAM address assignment (2) (When 256K SRAM is used)

VRAM / S-4581A	VRAM pin: Address bus	VRAM pin: Chip select	Memory mapping
MA0	A0		
MA1	A1		
MA2	A2		
MA3	A3		
MA4	A4		
MA5	A5		
MA6	A6		
MA7	A7		
MA8	A8		
MA9	A9		
MA10	A10		
MA11	A11		
MA12	A12		
MA13 / $\overline{MCS7}$	A13		
MA14 / $\overline{MCS6}$	A14		
$\overline{MCS5}$			
$\overline{MCS4}$			
$\overline{MCS3}$			
$\overline{MCS2}$			
$\overline{MCS1}$		$\overline{MCS1}$	8000H to FFFFH
$\overline{MCS0}$		$\overline{MCS0}$	0000H to 7FFFH

- D0 to D3

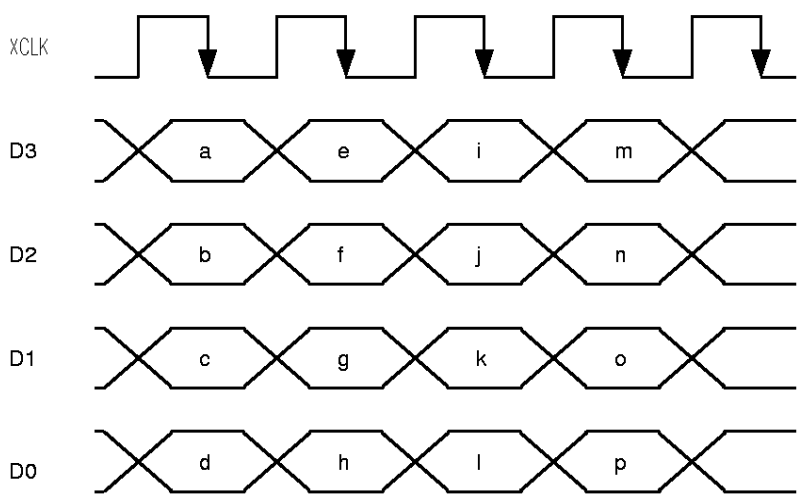
  D0 to D3 are LCD display data. The following are the display data output from the D0 to D3 pins and the panel display:





- XCLK

  A shift clock for display data transfer. The D0 to D3 display data is sent to the LCD at a falling edge ▼ of XCLK.



- YCLK

  This clock is used to transfer display data latch pulse and scan signals. It is output when one line of LCD data is transmitted. Latch the display data at a falling edge ▼ of YCLK. Also, latch the scan signal at a falling edge ▼ of YCLK.

- M

  A frame signal to drive the LCD.

- FLM

  Outputs a start pulse of a scan line. The signal is active when it is high, and the scan line drive IC should read FLM at falling edge ▼ of YCLK.

- LCDENB

  Outputs data set at bit 1 (D1) of the mode register (R1), which is one of control registers.

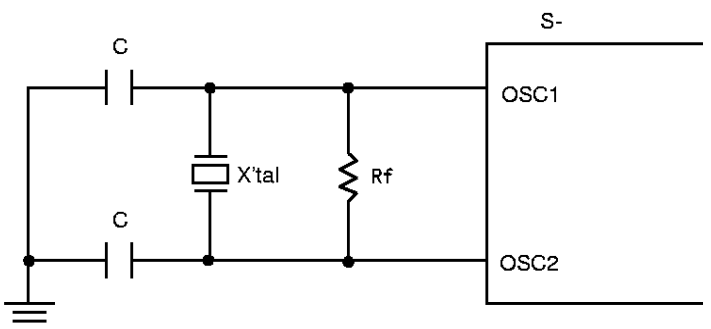
  The signal is low at reset and can be used to control the LCD power supply.

● Oscillation pins

- OSC1 and OSC2

  These pins output clocks for internal operations. OSC1 is an input pin and OSC2 is an output pin. The crystal oscillation clock can be output from OSC2 and external clocks can be input to OSC1.

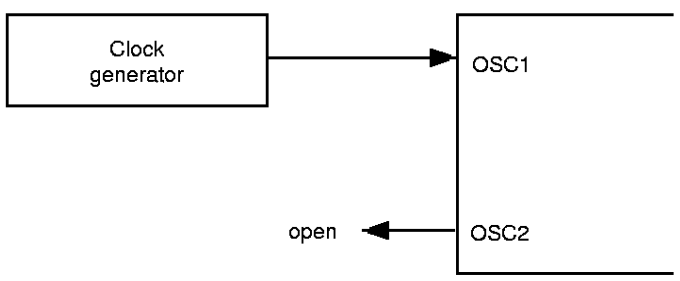
  (i) Crystal oscillation



Note: Install C, Rf, and X'tal close to the pin.

C ≅ 30pf Rf = 1MΩ

(ii) When external clocks are input



● Power supply pins

VDD, VSS

Each of the power supply pins has two pins. Supply positive power to V_{DD} and 0V to V_{SS}. Be sure to connect a capacitor near a pair of V_{DD} and V_{SS}.(4.7μF or more)

■ Control Registers

The S-4581A contains 22 registers to interface with various sizes of LCDs and display data freely.
Use $\overline{ICS}$, $\overline{IWR}$, and $\overline{IRD}$ for setting. The address of each register is defined by A0 to A4.

● Types of control registers

Register type		I/O address					Data									
No	Name	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Register function	R/W
R1	Mode register	0	0	0	0	1	DISP	REV	—	TST	GRAD	EX	LCDE	RAMS	Set the basic operation mode of the S-4581A.	W
R2	Horizontal display width register	0	0	0	1	0	← C/R →								Set the horizontal display width of each line.	W
R3	Horizontal synchronizing pulse width register	0	0	0	1	1	← YW →								Set the pulse width of the YCLK output for each line.	W
R4	Vertical line count register	0	0	1	0	0	← SLTL → (Lower)								Set the number of vertical lines of the LCD.	W
R5		0	0	1	0	1	*	*	*	*	*	*	← (Upper) SLTH		Set eight lower bits for SLTL and two upper bits for SLTH.	
R6	Screen display start address register	0	0	1	1	0	← SADL → (Low order)								Set the screen start address.	R/W
R7		0	0	1	1	1	← SADH → (High order)								Set eight lower bits for SADL and eight high-order bits for SADH.	R/W
R14 or R18	Gradation conversion code register GS1 (Note 2)	0 / 1	1 / 0	1 or 0	1 / 0	0 / 0	← GS1 →								Set gradation conversion code when gradations are displayed.	W
R15 or R19	Gradation conversion code register GS2 (Note 2)	0 / 1	1 / 0	1 or 0	1 / 1	1 / 1	← GS2 →								4-gradation mode (C1, C0)=(0, 0)⇒GS0 (C1, C0)=(0, 1) ⇒GS1	
R17	Gradation conversion code register GS0	1	0	0	0	1	← GS0 →								(C1, C0)=(1, 0) ⇒GS2 (C1, C0)=(1, 1) ⇒GS3	
R20	Gradation conversion code register GS3	1	0	1	0	0	← GS3 →								8-gradation mode (C2, C1, C0)=(0, 0, 0) ⇒GS0 (C2, C1, C0)=(0, 0, 1) ⇒GS1	W
R21	Gradation conversion code register GS4	1	0	1	0	1	← GS4 →								(C2, C1, C0)=(0, 1, 0) ⇒GS2 (C2, C1, C0)=(0, 1, 1) ⇒GS3 (C2, C1, C0)=(1, 0, 0) ⇒GS4	
R22	Gradation conversion code register GS5	1	0	1	1	0	← GS5 →								(C2, C1, C0)=(1, 0, 1) ⇒GS5 (C2, C1, C0)=(1, 1, 0) ⇒GS6 (C2, C1, C0)=(1, 1, 1) ⇒GS7	
R23	Gradation conversion code register GS6	1	0	1	1	1	← GS6 →									
R24	Gradation conversion code register GS7	1	1	0	0	0	← GS7 →									
R25	FLM register	1	1	0	0	1	ENB	← FLM →							Set the number of M reversing frames when the tailing prevention circuit is activated.	W
R26	CL1 register	1	1	0	1	0	← CL1 →								Set the number of M reversing lines when the tailing prevention circuit is activated.	W
R27	SLS register	1	1	0	1	1	ENB	← SLS →							Set the number of shift lines for each frame when the tailing prevention circuit is activated.	W
R28 . . R31	Test register	1 . . 1	1 . . 1	1 . . 1	0 . . 1	0 . . 1									IC test register. If this area is accessed, the function defined in the specification document cannot be implemented. DO NOT access it.	DO NOT access it.

Remark: Only control register addresses A4 to A0 are decoded. A7 to A5 are ignored.

Note 1: R14/R18: When either the R14 or R18 address is pointed, a value can be written into the CSI register.
This also applies to R15/R19.

- Description of registers
  - R1 : Mode register · · · · · Set the basic operation mode of the S4581.

Bit	Code	Function		At reset
D7	DISP	Turn the LCD on and off.	0 LCD off 1 LCD on	0
D6	REV	Turn the LCD on normally or reversibly.	0 Normal display 1 Reserved display	0
D5	—	DONT Care	0 — 1 —	—
D4	TST	Test bit	0 Normal state 1 Test state	0
D3	GRAD	LCD gradation display	0 4-gradation display 1 8-gradation display	0
D2	EX	Enable or disable the internal tailing prevention circuit.	0 Disable 1 Enable	0
D1	LCDE	Set the LCDENB pin output.	0 LCDENB=0 1 LCDENB=1	0
D0	RAMS	Select the type of SRAM to be used as VRAM.	0 64KSRAM 1 256KSRAM	0

DISP

- Set the display on/off.

  DISP = "0" : Display off

  DISP = "1": Display on

- DISP = "0" at reset and the display is set to off.
- If bit 6 (D6) REV of the mode register is "1" for reverse display, "1" is output for display data (D0 to D3) when DISP = "0. "

REV

- Set normal/reverse display.

  REV = "0": Normal display

  REV = "1": Reserve display

- REV = "0" at reset and the normal display is set.

TST

- TST = "0" at reset. DO NOT write any values other than "0" into this test bit.

GRAD

- Set the 4-gradation mode or 8-gradation mode for the LCD display.

  GRAD = "0": 4-gradation mode

  GRAD = "1": 8-gradation mode

- If the 4-gradation mode is set by setting GRAD="0, " one dot is displayed by two data bits of the VRAM.

VRAM data							
D7	D6	D5	D4	D3	D2	D1	D0
C1	C0	C1	C0	C1	C0	C1	C0

The gradation conversion code referenced by (C1,C0) is set by R17, R18, R19, and R20. R17 and R20 are initialized to all0 and all1, respectively, but can be modified by a program.

C1	C0	Display contents
0	0	Gradation display based on GS0 conversion code
0	1	Gradation display based on GS1 conversion code
1	0	Gradation display based on GS2 conversion code
1	1	Gradation display based on GS3 conversion code

If the 8-gradation display mode is set by setting GRAD="1,"one dot is displayed by three data bits of the VRAM.

VRAM data							
D7	D6	D5	D4	D3	D2	D1	D0
*	C2	C1	C0	*	C2	C1	C0

*: Don't care

The gradation conversion code referenced by (C2,C1,C0) is set by R17 to R24.

C2	C1	C0	Display contents
0	0	0	Gradation display based on GS0 conversion code
0	0	1	Gradation display based on GS1 conversion code
0	1	0	Gradation display based on GS2 conversion code
0	1	1	Gradation display based on GS3 conversion code
1	0	0	Gradation display based on GS4 conversion code
1	0	1	Gradation display based on GS5 conversion code
1	1	0	Gradation display based on GS6 conversion code
1	1	1	Gradation display based on GS7 conversion code

- At reset, GRAD becomes "0" and the 4-gradation display mode is set.

EX

- Set whether to use the internal tailing prevention circuit.

EX=0	Not use the internal tailing prevention circuit.
EX=1	Use the internal tailing prevention circuit.

- If the internal tailing prevention circuit is not used, the M signal shows the waveform that is reversed at each falling edge of FLM and YCLK.
  If the internal tailing prevention circuit is used, the M signal has a special waveform according to the FLM, CL1, and SLS registers as described in the other section.
- At reset, EX= "0" and the internal tailing prevention circuit is not used.

LCDE

- The data set in LCDE is output to the LCDENB pin. It is provided to control application of the LCD voltage. For example, when the power turns on, the LCDE is set to"1"after setting each register ends to supply voltage to the LCD. When the system power turns off, LCDE is set to"0"and then the LCD voltage turns off. This prevents application of an abnormal voltage (DC) to the LCD (The LCDENB output is used for control).
- This function is limited to the LCD and can be used as required.
- At reset, LCDE = "0" and "0" (VSS) is output from the LCDENB pin.

RAMS

- Set the type of SRAM to be used as VRAM. (⇒ R2 setting)

RAMS="0": 64KSRAM (8K×8)
RAMS="1": 256KSRAM (32K×8)

- If RAM="0" and 64K SRAM is set, the addresses must be set as shown in Table 5-2.
- If RAM="1" and 256K SRAM is set, the addresses must be set as shown in Table 5-3.
- At reset, RAMS="0" and 64K SRAM is set.

- R2 : Horizontal display width register

I/O address					Data							
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	← C/R →							

Set the horizontal display width per line $\frac{1}{4}$ of the number of actual display dots - 1 is set as the C/R value. For example, if the horizontal display dot count is set to 128, the C/R value is $\frac{128}{4}$ - 1 = 31 (1FH). If the value has fractions, they are rounded up. 0 to 2 cannot be set for the C/R. The maximum number of horizontal dots is 1024. The following condition must be satisfied due to the limit of the S4518A operation speed:

$$\text{Number of horizontal display dots (C/R + YW)} \times \text{(Number of vertical lines SLT + 2)} < \frac{8\ \text{MHz}}{\text{Frame frequency}}$$

The C/R, YW, and SLT show the register setting +1. 8 MHz is the maximum repetitive frequency of the OSC1 pin.

- R3: Horizontal synchronizing pulse width register

I/O address					Data							
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	← YW →							

Set the horizontal synchronizing pulse width per line.

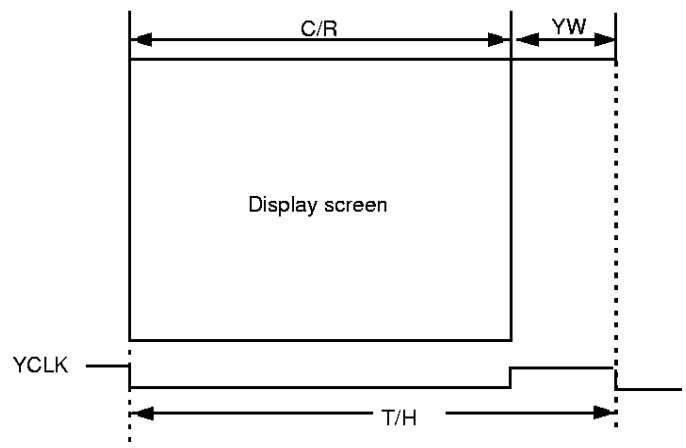
Set the horizontal synchronizing pulse width in the same unit as the horizontal display width (C/R).

If the horizontal synchronizing pulse width is set to 100 dots, the value of YW is $\frac{10}{4}$ - 1 = 24. 0 to 2 cannot be set for the YW.

The horizontal synchronizing pulse is output from the S-4581A YCLK pin and used for serial/parallel conversion of display data.

[Reference]

Relationship between the setting and horizontal display width (TH):



Since the TH time is changed by changing the value of YW, so the frame frequency can be changed.

Since two OSC1 clocks are required to access one byte of the VRAM, four dots of the LCD screen are produced by one byte in the 4-gradation mode and $\frac{1}{2\,fosc}$ time is required for each dot.

In the 8-gradation display mode, two dots indicate one byte, so $\frac{1}{fosc}$ time is required for each dot

The time required per horizontal display width (C/R) is $\frac{2}{fosc}$ in the 4-gradation mode. And $\frac{4}{fosc}$ in the 8-gradation mode.

Display mode	Required time per dot	Required time per horizontal display width (C/R)
4-gradation	$\frac{1}{2 \times fosc}$	$\frac{2}{fosc}$
8-gradation	$\frac{1}{fosc}$	$\frac{4}{fosc}$

(Unit: sec)

fosc is the frequency given to the OSC1 pin.

The required time per horizontal display width (C/R) is the same as the time per horizontal synchronizing pulse width (YW). The sum of these values indicates the time per line. The required time TH per line is calculated as follows:

- 4-gradation display mode

$$TH = \frac{2}{fosc} \times (C/R+YW)$$

- 8-gradation display mode

$$TH = \frac{4}{fosc} \times (C/R+YW)$$

The C/R and YW values show the register setting +1.

- R4, R5: Vertical line count register

I/O address					Data							
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	← SLTL →							
0	0	1	0	1	*	*	*	*	*	*	← SLTH →	

Set the number of vertical display lines of the LCD. Eight lower bits are assigned to SLTL and two upper bits are assigned to SLTH. The total data length is 10 bits. (0 to 1023)

Set the number of actual display lines -1.

The vertical line count register sets the LCD display drive duty. The actual drive duty is the vertical line count + 2. This value of 2 indicates the vertical return line period during which the S-4581A performs internal processing to switch frames. The LCD display drive duty that can be set by the S-4581A is 1/3 to 1/1026.

- R6, R7: Screen display start address register

R No.	I/O address					Data								R/W
	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R6	0	0	1	1	0	←			SADF				→	W
R7	0	0	1	1	1	←			SADL				→	W

Set the screen start address (SAD). Set eight lower bits to SADL and eight high-order bits are assigned to SADH. The value can be 0000H to FFFFH (64KB).

- R14, R15, R17 to R24: Gradation conversion code register

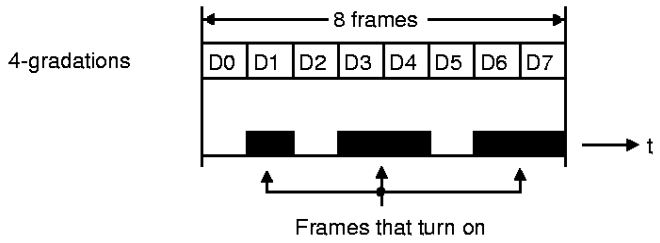
R No.	I/O address					Data								R/W
	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R14/18	0 1	1 0	1 0	1 1	0 0	←			GS1				→	W
R15/19	0 1	1 0	1 0	1 1	1 1	←			GS2				→	W
R17	1	0	0	0	1	←			GS0				→	W
R20	1	0	1	0	0	←			GS3				→	W
R21	1	0	1	0	1	←			GS4				→	W
R22	1	0	1	1	0	←			GS5				→	W
R23	1	0	1	1	1	←			GS6				→	W
R24	1	1	0	0	0	←			GS7				→	W

(At reset, R20 are all 1 and the other registers are all 0.)

Set the gradation conversion code in each gradation display mode. In the 4-gradation display mode, 2 bits of VRAM are assigned to display one dot, and 4-level gradations can be expressed. The four levels are set by GS0, GS1, GS2, and GS3. In the 8-gradation display mode, 3 bits of VRAM are assigned to display one dot, and 8-level gradations can be expressed. The eight levels are set by GS0, GS1, GS2, ... and GS7.
R14 and R18 are common registers to both 4- and 8-gradation modes. The newest values written to the registers become effective. This also applies to R15 and R19.

The gradation conversion code is used to change display density.
The gradation can be set by using eight continuous frames as a unit and omitting one or more of them. The eight frames correspond to D0 to D7 of data, and D0 corresponds to the first frame.
For example, if three of eight frames are omitted, there are 8C3 combinations, but the optimum conversion code for the LCD panel characteristics needs to be set. There is no restriction on the omission method, but dots should be omitted evenly.
DO NOT omit any continuous frames. To prevent display flickering, it is recommended to set the frame frequency to 100 Hz (10 msec) or higher depending upon the LCD panel characteristics.

Example: If three of eight frames are omitted



In this case, the conversion code is DAH.

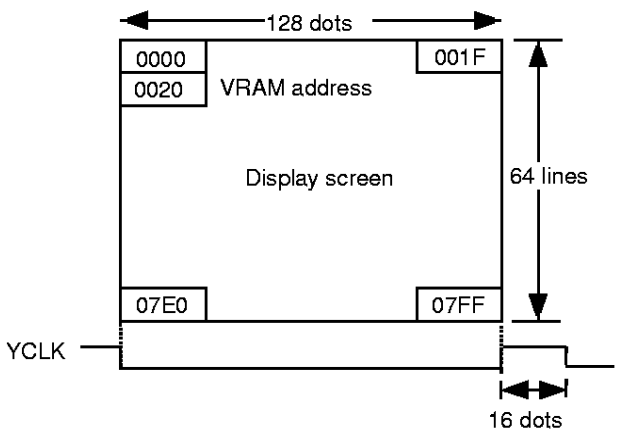
In addition, the gradation display mode can be used as a display mode having the dot on/off attribute function. For example, C1 of (C1, C0) data of the 4-gradation display mode is assigned as display data and C0 is used as an on/off attribute. In this case, GS1 and GS2 need to be 00H. The same also goes in the 8-gradation display mode. At reset, R20 (GS3) are all 1s and the other registers are all 0.

■ Display Mode

The S-4581A, 4- and 8-gradation display modes are described below.

- 4-gradation display mode

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	—	TST	GRAD	EX	LCDE	RAMS
*	*	*	0	0	*	*	*

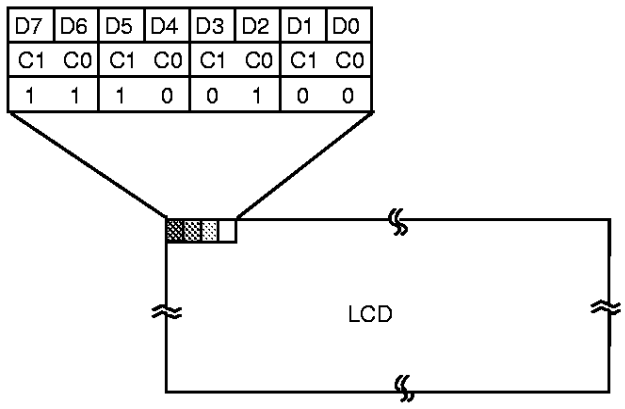


(Setting example)

128 × 64 dot display
C/R=31(1FH)
YW=3(03FH)
SLT=63(3FH)
SAD=0000H
GS0=00H
GS1=AAH
GS2=EEH
GS3=FFH
GS0 to GS3 depend upon the type of LCD.

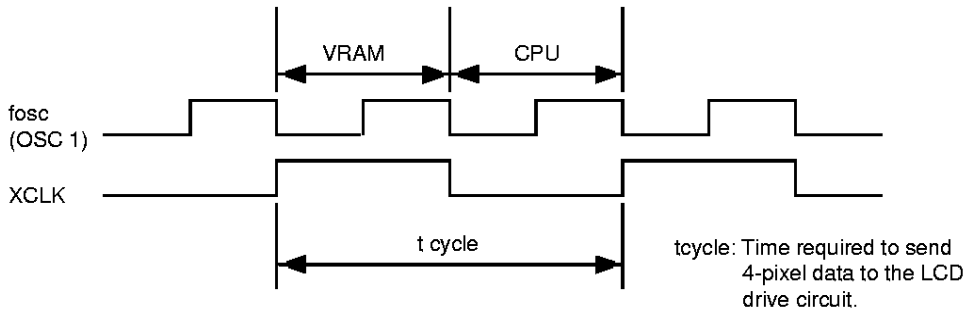
- Relationship between VRAM data and display (4-gradation display mode)

D7	D6	D5	D4	D3	D2	D1	D0
C1	C0	C1	C0	C1	C0	C1	C0
1	1	1	0	0	1	0	0



Remark: VRAM data becomes display data by converting GS0 to GS3 corresponding to (C1, C0).

- Basic timing (4-gradation display mode)



For the basic timing of the S-4581A, the basic cycle is two fosc clocks, and the first clock is used to read display data from the VRAM and the second clock is used to access from the CPU.

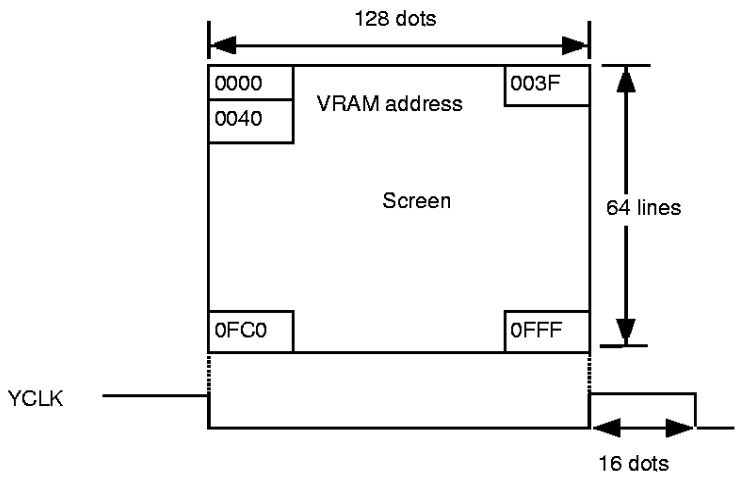
When the frame frequency f_{FLM} is 100 Hz, the oscillation frequency fosc is calculated as follows:

$$\text{fosc} = (C/R + YW) \times (SLT + 2) \times f_{FLM} \times 2$$
$$= (32 + 4) \times (64 + 2) \times 100 \times 2$$
$$\cong 475\ kH_Z$$

Remark: The C/R, YW, and SLT show the register setting + 1.

- 8-gradation display mode

Mode register (R1)							
D7	D6	D5	D4	D3	D2	D1	D0
DISP	REV	—	TST	GRAD	EX	LCDE	RAMS
*	*	*	0	1	*	*	*



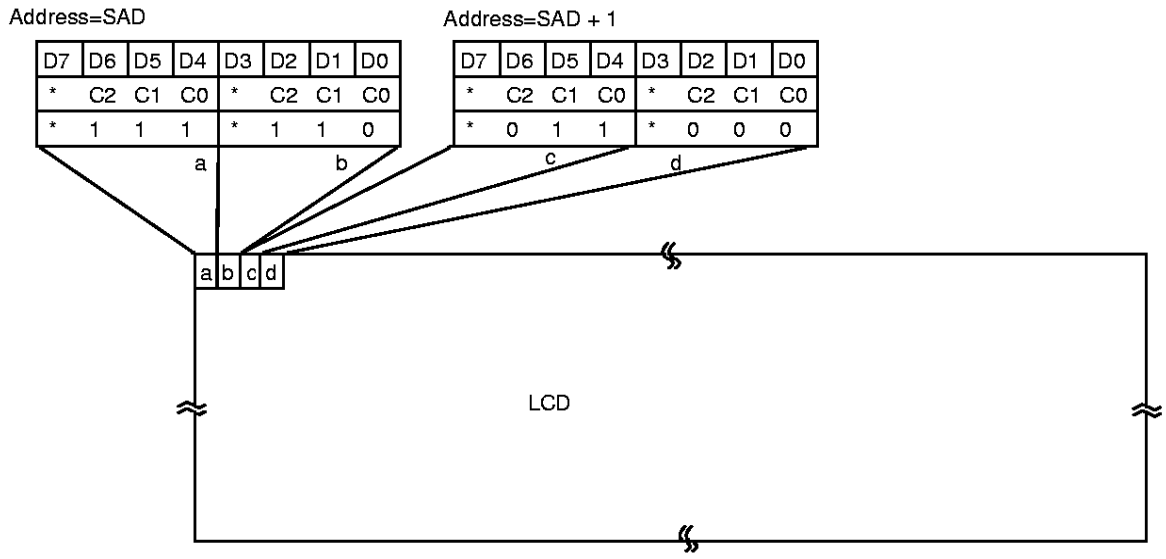
(Setting example)
128 × 64 dot display

C/R=31(1FH)
YW=3(03H)
SLT=63(3FH)
SAD=0000H

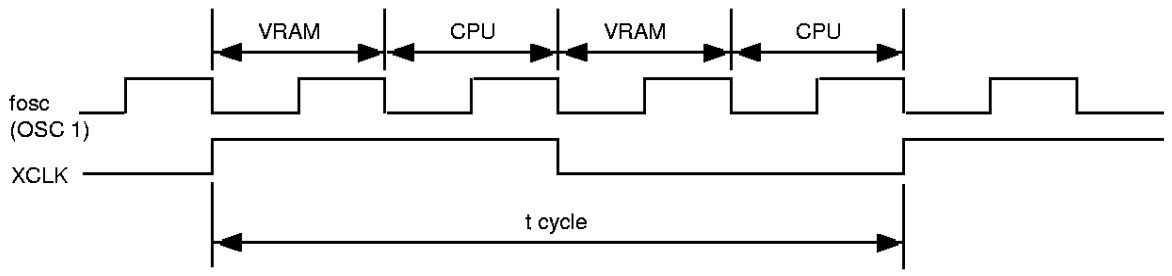
GS0=00H
GS1=03H
GS2=07H
GS3=0FH
GS4=1FH
GS5=3FH
GS6=7FH
GS7=FFH

GS0 to GS7 depend upon the type of LCD.

・ Relationship between VRAM data and display (8-gradation display mode)



・ Basic timing (8-gradation display mode)



To process two bytes of VRAM in the same cycle, two basic cycles, i.e., four fosc clocks are used as one cycle.

When the frame frequency f_{FLM} is 100 Hz, the oscillation frequency fosc is calculated as follows:

$$\begin{aligned} fosc &= (C/R+YW) \times (SLT+2) \times f_{FLM} \times 4 \\ &= (32+4) \times (64+2) \times 100 \times 4 \\ &\simeq 950KHz \end{aligned}$$

Remark: The C/R, YW, and SLT show the register setting +1.

Tailing prevention circuit

If mode register 1 EX = 1, the S-4581A M pin outputs a different waveform according to the values of the FLM, CL1, and SLS registers. If EX = 0, the M signal reverses at each falling edge of FLM and YCLK.
The values of the FLM, CL1, and SLS registers at this time are omitted.

R25: FLM register

This register reverses or controls the M signal for every some frames. The D7 (ENB) bit is an enable bit. If this bit is 0, the signal does not reverse.
The D6 to D0 bits set the number of reversed frames. The FLM register becomes 00H when a reset signal is input. The setting value is the actual value -1.

Relationship between FLM register and reversing frame

FLM								Number of M reversing frames
D7	D6	D5	D4	D3	D2	D1	D0	
ENB	◄ FLM ►							
0	*	*	*	*	*	*	*	Not reverse.
1	0	0	0	0	0	1	0	Reverse in each frame.
1	0	0	0	0	0	0	1	Reverse in every two frames.
				⋮				⋮
1	1	1	1	1	1	1	1	Reverse in every 128 frames.

- R26: CL1 register:

  The CL1 register reverses or controls the M signal for each line in a frame. This register becomes 00H when a reset signal is input.

Relationship between CL1 register and the number of M reversing lines

CL1								Number of M reversing lines in one frame
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Not use
0	0	0	0	0	0	0	1	One line
0	0	0	0	0	0	1	0	Two lines
				⋮				⋮
1	1	1	1	1	1	1	1	255 lines

- R27SLS register:

  This register sets the number of lines to be shifted for each line set by the value of the CL1 register for each frame. The D7 (ENB) bit is an enable bit. If this bit is 0, no lines are shifted. The SLS register becomes 00H when a reset signal is input.

Relationship between SLS register and the number of lines to be shifted

SLS								Number of lines to be shifted in every frame
D7 (ENB)	D6	D5	D4	D3	D2	D1	D0	
0	*	*	*	*	*	*	*	Not shift any lines.
1	0	0	0	0	0	0	0	Not use
1	0	0	0	0	0	0	1	Shift one line.
1	0	0	0	0	0	1	0	Shift two lines.
				⋮				⋮
1	1	1	1	1	1	1	1	Shift 127 lines.

CL1 and SLS must satisfy the following conditions: SLT > CL1 ≥ SLS.

If lines are reversed or shifted, follow the procedures below:

(1) If lines are reversed or shifted after a reset signal is input

  ··· After setting data in the CL1 register, set data in the SLS register.

(2) After a reset signal is input, set each register value by the method (1), then each register value is updated:

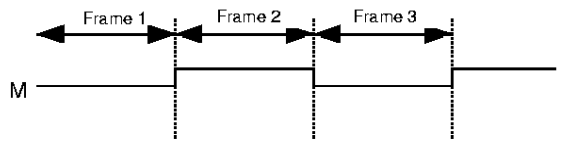
··· ① Set 00H for the CL1 register and 00H for the SLS register.

  ② Wait (frame period calculated from the setting) × 2.

  ③ Set data for the CL1 register and SLS register.

If this procedure is not satisfied, the M signal does not have the expected waveform until the reversal of the signal set by the FLM register occurs. Two or three register values and examples of M signal waveforms are shown the next pages.

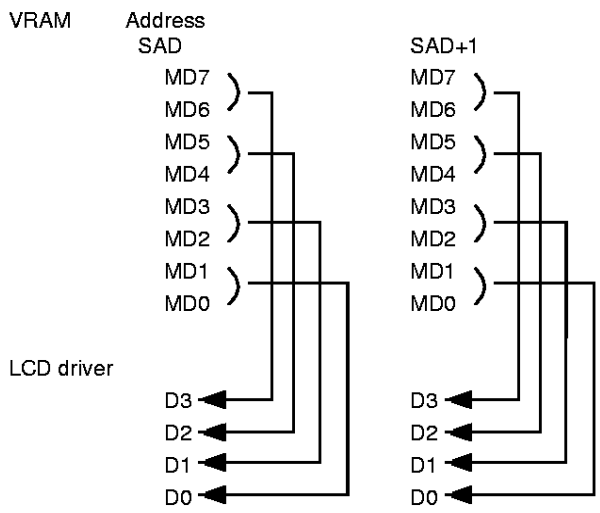
(Example): Mode register EX=0



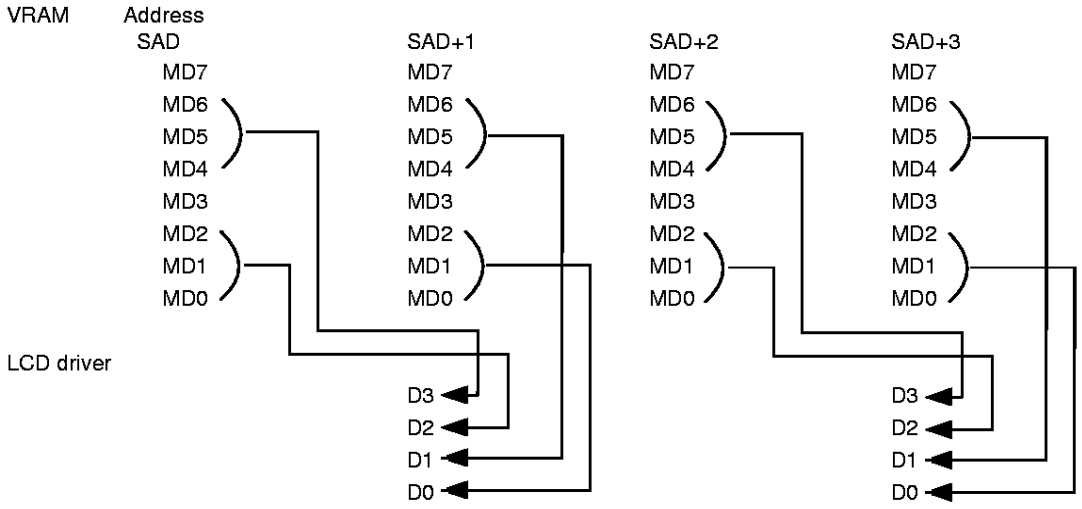
- Relationship between VRAM and LCD driver data

  The relationship between 4- and 8-gradation VRAM data and LCD driver data is shown below:

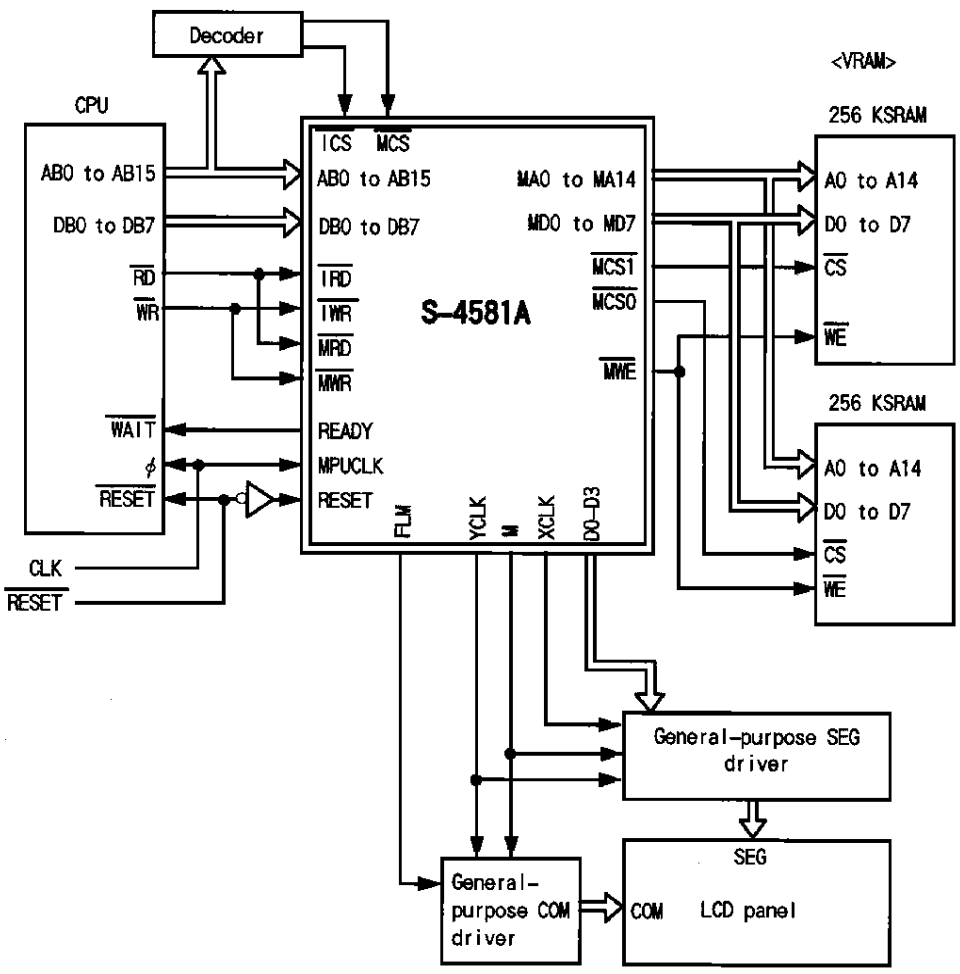
  (1) 4-gradation



  (2) 8-gradation

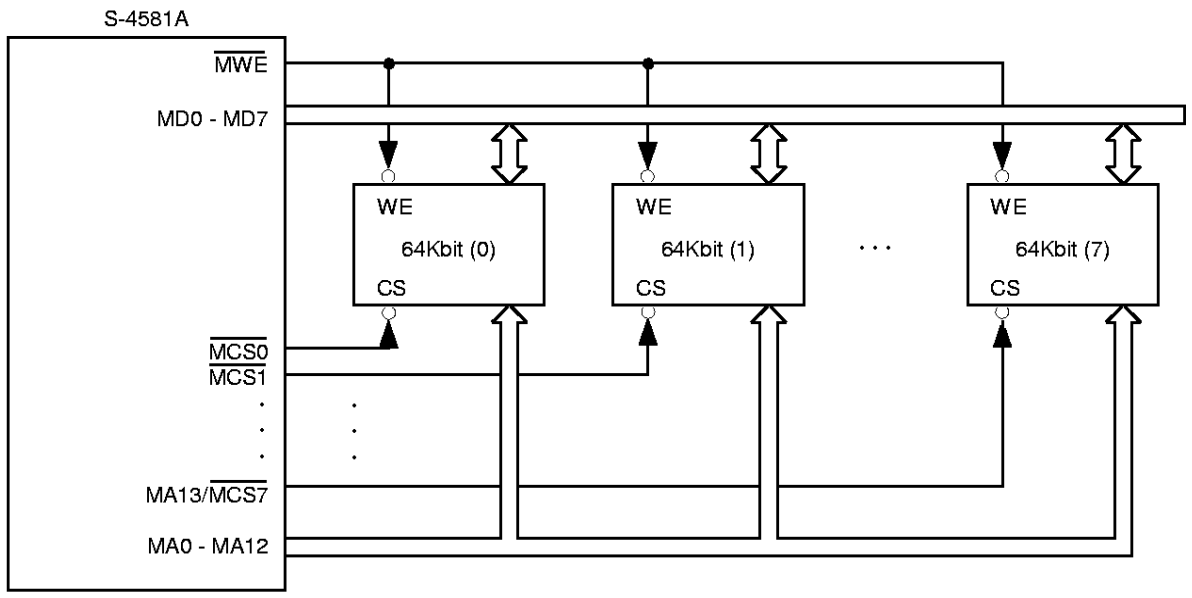


■ Example of Connection with Peripheral Devices



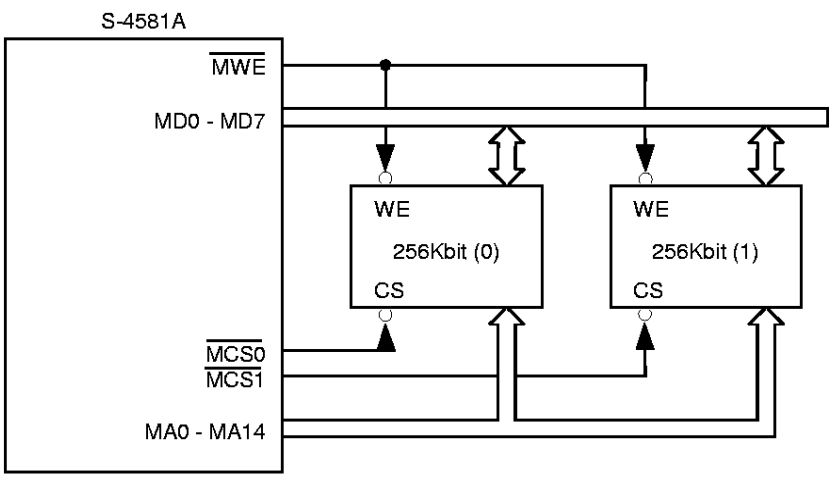
■ VRAM Interface

- 8-bit MPU, 64KSRAM



Note: Set bit 0 (D0) of the mode register (R1) to"0".

- 8-bit MPU, 256 KSRAM



Remark: Set bit 0 (D0) of the mode register (R1) to"1"

■ Electrical Characteristics

S-4581A

● Absolute maximum rating

Item	Code	Rating	Unit
Power supply voltage	V_{DD}	V_{SS}-0.3 to 7.0	V
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	V_{SS}-0.3 to V_{DD}+0.3	V
Output current/pin	I_{OUT}	±10	mA
Permissible loss	P_D	200	mW
Power supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	-65 to 150	°C

Remark: Power supply current --- Permissible current flowing into or out of the power supply pin (VD0 or VSS)

V_{SS}=0[V]

● Recommended operating conditions

Item	Code	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage	V_{IN}	V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}	-20	—	75	°C

V_{SS}=0[V]

● DC characteristics (Ta=-20°C to 75°C)

Item	Code	Condition	Min	Typ	Max	Unit	Applicable pin
Static current		V_{IN}=V_{DD}, V_{SS} V_{DD}=MAX I_{OH}=I_{OL}=0	—	0.1	10	µA	
Input leak current		V_{DD}=MAX V_{IH}=V_{DD} V_{IL}=V_{SS}	-1	—	1	µA	Note 1
"H" level input voltage "L" level input voltage		V_{DD}=MAX V_{DD}=MIN	3.5 —	— —	— 1.0	V V	OSC1
"H" level input voltage "L" level input voltage		V_{DD}=MAX V_{DD}=MIN	2.0 —	— —	— 0.8	V V	Note 2
"H" level input voltage "L" level input voltage Hysteresis voltage		V_{DD}=MAX V_{DD}=MIN V_{DD}=TYP	4.0 — 0.3	— — —	— 0.8 —	V V V	Note 3
"H" level output voltage "L" level output voltage		V_{DD}=MIN I_{OH}=1mA I_{OL}=2mA	V_{DD}-0.4 —	— —	— V_{SS}+0.4	V V	Note 4
"H" level output voltage "L" level output voltage		V_{DD}=MIN I_{OH}=50µA I_{OL}=50µA	V_{DD}-0.4 —	— —	— V_{SS}+0.4	V V	OSC2

Note 1: $\overline{MCS}$, $\overline{MWR}$, $\overline{MRD}$, $\overline{ICS}$, $\overline{IWR}$, $\overline{IRD}$, MPUCLK, AB0 to AB15, RESET, OSC1

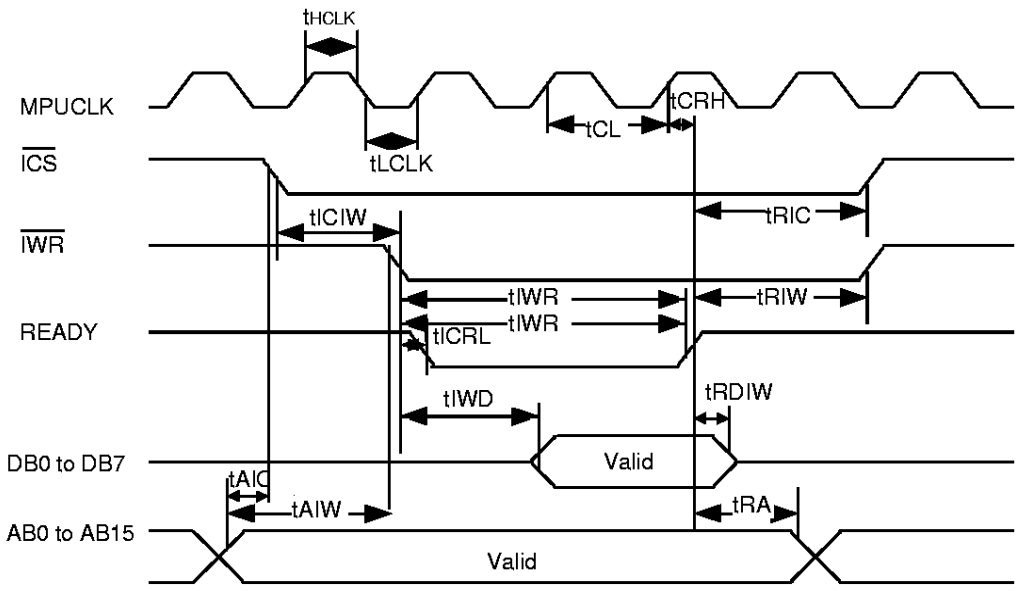
Note 2: $\overline{MCS}$, $\overline{MWR}$, $\overline{MRD}$, $\overline{ICS}$, $\overline{IWR}$, $\overline{IRD}$, MPUCLK, AB0 to AB15, DB0 to DB7, MD0 to MD7

Note 3: RESET

Note 4: DB0 to DB7, READY, MA0 to MA 14, $\overline{MCS0}$ to $\overline{MCS5}$, MD0 to MD7, MWE, $\overline{XCLK}$, YCLK, M, FLM, D0 to B3, LCDENB

- AC characteristics
  - $\overline{IWR}$ timing

    (Writing into the control register)

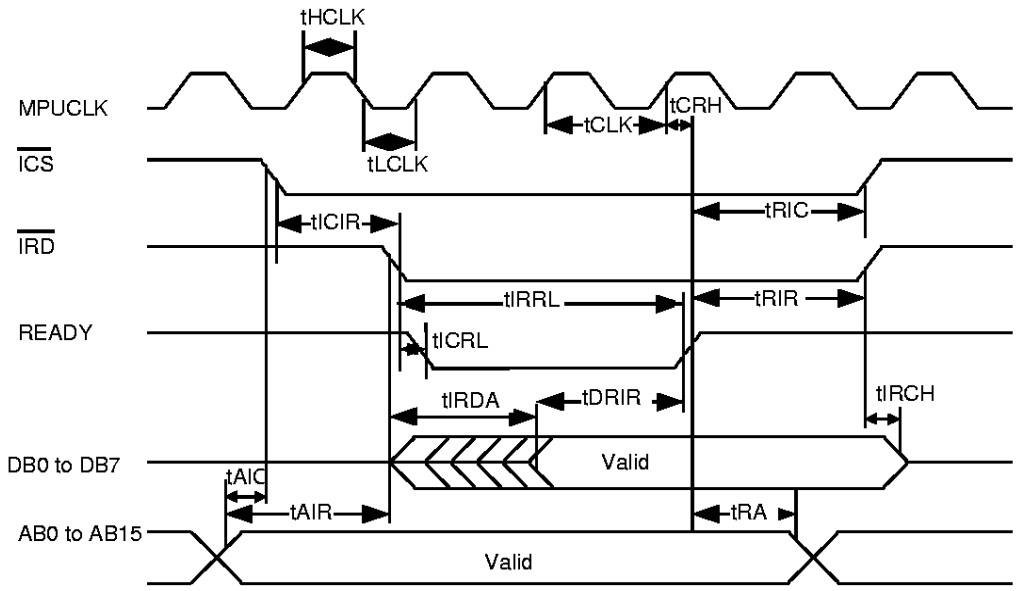


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
tCLK	MPUCLK period	80	—	—	nsec
tHCLK	MPUCLK . H. pulse width	20	1/2 · tCLK	—	nsec
tLCLK	MPUCLK . L. pulse width	20	1/2 · tCLK	—	nsec
tAIC	$\overline{ICS}$ address setup time	0	—	—	nsec
tAIW	$\overline{IWR}$ address setup time	0	—	—	nsec
tICIW	$\overline{ICS}$ ↓ → $\overline{IWR}$ ↓	0	—	—	nsec
tIWD	$\overline{IWR}$ ↓ → Write data determination	—	—	0.5 · tOSC	nsec
tICRL	$\overline{IWR}$ ↓ → Not Ready	—	—	30	nsec
tIWRL	$\overline{IWR}$ ↓ → Ready period	tosc	—	3tosc+tCLK	nsec
tCRH	MPUCLK ↓ → Ready	—	—	20	nsec
tRIC	READY ↑ → $\overline{ICS}$ retention time	0	—	—	nsec
tRIW	READY ↑ → $\overline{IWR}$ retention time	0	—	—	nsec
tRDIW	READY ↑ → Write data retention time	0	—	—	nsec
tRA	READY ↑ → Address retention time	0	—	—	nsec

· $\overline{IRD}$ timing

(Reading from control register)

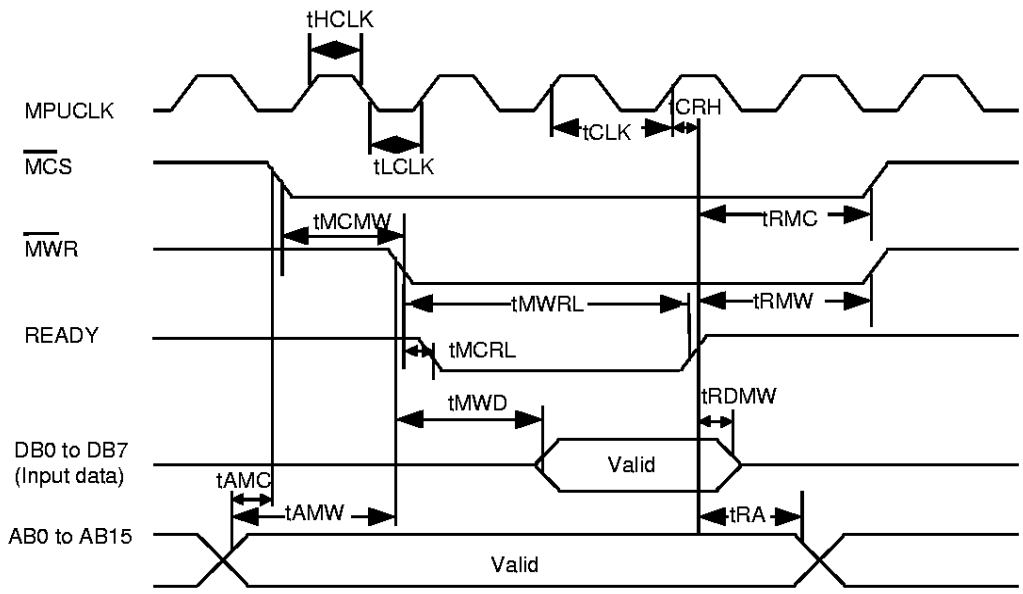


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
t_{CLK}	MPUCLK period	80	—	—	nsec
t_{HCLK}	MPUCLK . H. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{LCLK}	MPUCLK . L. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{AIC}	$\overline{ICS}$ address setup time	0	—	—	nsec
t_{AIR}	$\overline{IRD}$ address setup time	0	—	—	nsec
t_{ICIR}	$\overline{ICS}\downarrow \rightarrow \overline{IRD}\downarrow$	0	—		nsec
t_{ICRL}	$\overline{IRD}\downarrow \rightarrow$ Not Ready	—	—	30	nsec
t_{IRRL}	$\overline{IRD}\downarrow \rightarrow$ Not Ready period	tosc	—	3 · tosc+t_{CLK}	nsec
t_{CRH}	MPUCLK $\downarrow \rightarrow$ Ready	—	—	20	nsec
t_{IRDA}	$\overline{IRD}\downarrow \rightarrow$ Read data determination	0.5 · tosc+50	—	2.5 · tosc+50	nsec
t_{DRIR}	Read data determination $\rightarrow$ READY $\uparrow$	0	—	—	nsec
t_{IRDH}	$\overline{IRD}\downarrow \rightarrow$ Read data retention time	0	—	—	nsec
t_{RIC}	READY $\uparrow \rightarrow \overline{ICS}$ retention time	0	—	—	nsec
t_{RIR}	READY $\uparrow \rightarrow \overline{IRD}$ retention time	0	—	—	nsec
t_{RA}	READY $\uparrow \rightarrow$ Address retention time	0	—	—	nsec

- $\overline{\text{MWR}}$ timing

  (Writing into the VRAM)

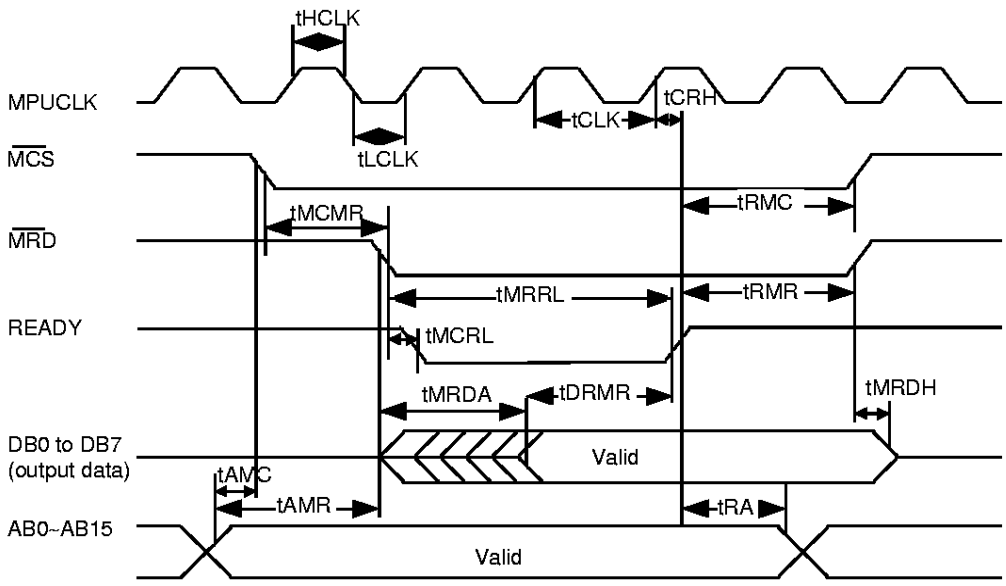


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
t_{CLK}	MPUCLK period	80	—	—	nsec
t_{HCLK}	MPUCLK . H. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{LCLK}	MPUCLK . L. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{AMC}	$\overline{\text{MCS}}$ address setup time	0	—	—	nsec
t_{AMW}	$\overline{\text{MWR}}$ address setup time	0	—	—	nsec
t_{MCMW}	$\overline{\text{MCS}}\downarrow \rightarrow \overline{\text{MWR}}\downarrow$	0	—	—	nsec
t_{MWD}	$\overline{\text{MWR}}\downarrow \rightarrow$ Write data determination	—	—	0.5 · tosc	nsec
t_{MCRL}	$\overline{\text{MWR}}\downarrow \rightarrow$ Not Ready	—	—	30	nsec
t_{MWRL}	$\overline{\text{MWR}}\downarrow \rightarrow$ Ready period	tosc	—	3 · tosc+t_{CLK}	nsec
t_{CRH}	MPUCLK $\uparrow \rightarrow$ Ready	—	—	20	nsec
t_{RMC}	READY $\uparrow \rightarrow \overline{\text{MCS}}$ retention time	0	—	—	nsec
t_{RMW}	READY $\uparrow \rightarrow \overline{\text{MWR}}$ retention time	0	—	—	nsec
t_{RDMW}	READY $\uparrow \rightarrow$ Write data retention time	0	—	—	nsec
t_{RA}	READY $\uparrow \rightarrow$ Address retention time	0	—	—	nsec

· $\overline{MRD}$ timing

(Reading from the VRAM)

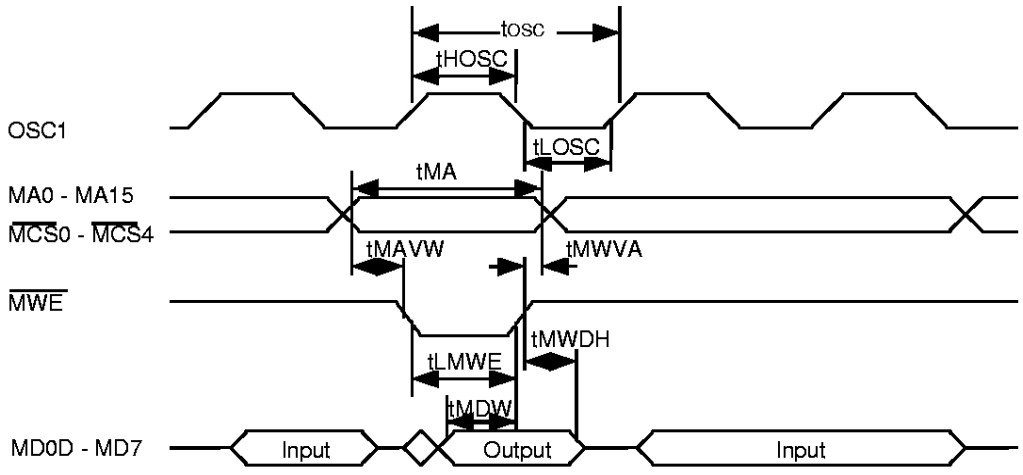


(Ta=-20°C to 75°C)

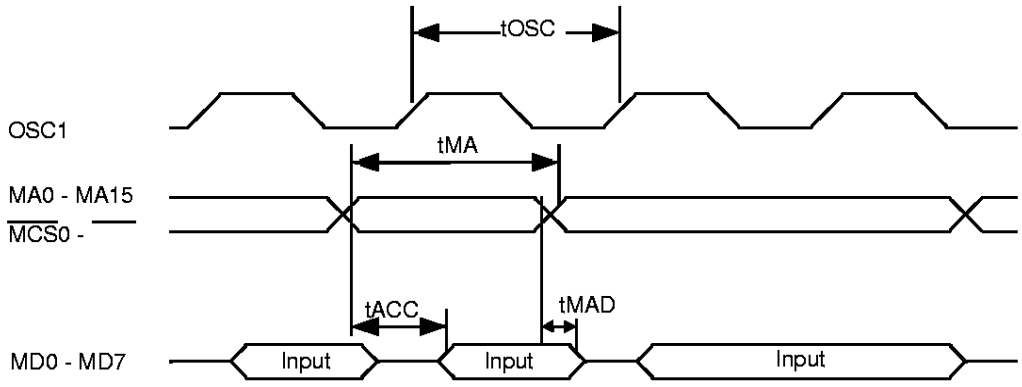
Code	Item	Min	Typ	Max	Unit
t_{CLK}	MPUCLK period	80	—	—	nsec
t_{HCLK}	MPUCLK. H. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{LCLK}	MPUCLK. L. pulse width	20	1/2 · t_{CLK}	—	nsec
t_{AMC}	$\overline{MCS}$ address setup time	0	—	—	nsec
t_{AMR}	$\overline{MRD}$ address setup time	0	—	—	nsec
t_{MCMR}	$\overline{MCS}$ ↓ → $\overline{MRD}$ ↓	0	—	—	nsec
t_{MCRL}	$\overline{MRD}$ ↓ → Not Ready	—	—	30	nsec
t_{MRRL}	$\overline{MRD}$ ↓ → Ready period	2 · tosc	—	4 · tosc+t_{CLK}	nsec
t_{CRH}	MPUCLK ↑ → Ready	—	—	20	nsec
t_{MRDA}	$\overline{MRD}$ ↓ → Read data determination	0.5 · tosc+50	—	3 · tosc+50	nsec
t_{DRMR}	Read data determination → READY ↑	0	—	—	nsec
t_{MRDH}	$\overline{MRD}$ ↑ → Read data retention time	0	—	—	nsec
t_{RMC}	READY ↑ → $\overline{MCS}$ retention time	0	—	—	nsec
t_{RMR}	READY ↑ → $\overline{MRD}$ retention time	0	—	—	nsec
t_{RA}	READY ↑ → Address retention time	0	—	—	nsec

· VRAM interface timing

(Writing into the VRAM)



(Reading from the VRAM)

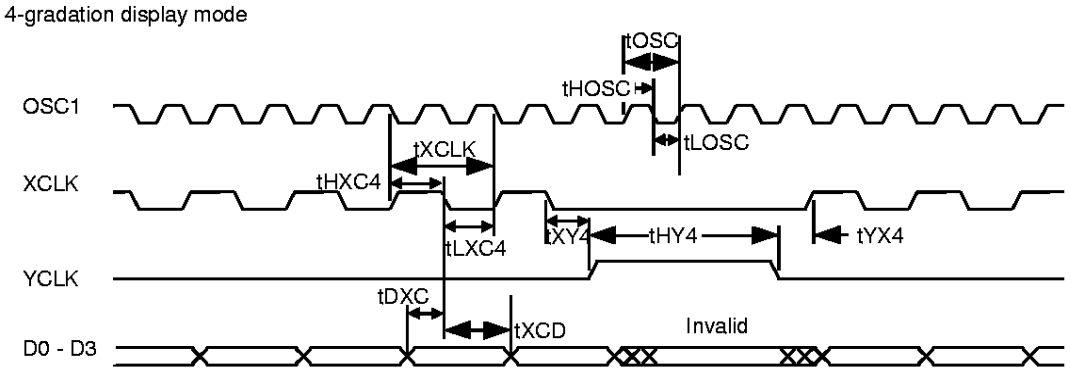


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
tOSC	OSC1 period	125	—	—	nsec
tHOSC	OSC1. H. pulse width	—	1/2·tosc	—	nsec
tLOSC	OSC1. L. pulse width	—	1/2·tosc	—	nsec
tMAVW	$\overline{\text{MWE}}$ address setup time	1/2·tosc-20	1/2·tosc	—	nsec
tMWVA	$\overline{\text{MWE}}$ address hold time	0	—	—	nsec
tLMWE	$\overline{\text{MWE}}$. L. pulse width	1/2·tosc-20	1/2·tosc	—	nsec
tMDWS	$\overline{\text{MWE}}$ data setup time	1/2·tosc-25	1/2·tosc	—	nsec
tMWDH	$\overline{\text{MWE}}$ data hold time	0	—	20	nsec
tMA	VRAM address cycle time	tosc	—	—	nsec
tACC	VRAM address access time	—	—	tosc-60	nsec
tMAD	VRAM read data retention time	0	—	—	nsec

· LCD interface timing (1)

4-gradation display mode

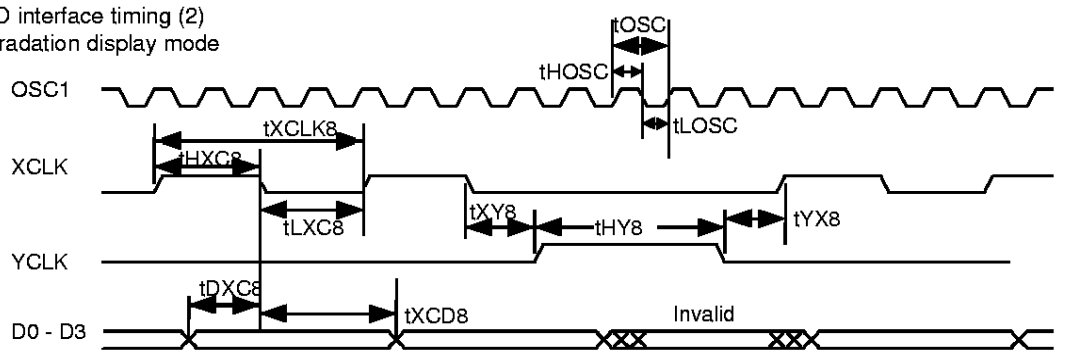


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
tOSC	OSC1 clock period	125	—	—	nsec
tHOSC	OSC1. H. pulse width	1/2 · tosc-10	—	—	nsec
tLOSC	OSC1. L. pulse width	1/2 · tosc-10	—	—	nsec
tXCLK4	XCLK period	2tosc-20	—	—	nsec
tHXC4	XCLK. H. pulse width	tosc-10	—	—	nsec
tLXC4	XCLK. L. pulse width	tosc-10	—	—	nsec
tXY4	XCLK ↓ → YCLK ↑	1/2 · tosc-10	—	—	nsec
tYX4	YCLK ↓ → XCLK ↑	tosc-10	—	—	nsec
tDXC4	Data determination → XCLK ↓	tosc-10	—	—	nsec
tXCD4	XCLK ↓ → Data retention time	tosc-20	—	—	nsec
tHY4	YCLK. H. pulse width (Note 1)	(2n-1/2) tosc-20	—	—	nsec

Note 1: n is the value of YW.

· LCD interface timing (2)
8-gradation display mode

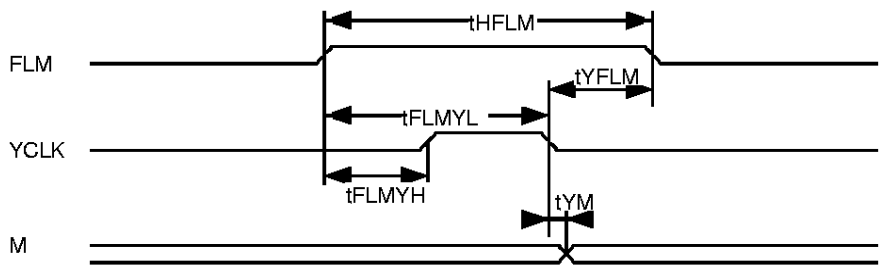


(Ta=-20°C to 75°C)

Code	Item	Min	Typ	Max	Unit
tOSC	OSC1 clock period	125	—	—	nsec
tHOSC	OSC1. H. pulse width	1/2 · tosc-10	—	—	nsec
tLOSC	OSC1. L. pulse width	1/2 · tosc-10	—	—	nsec
tXCLK8	XCLK period	4tosc-20	—	—	nsec
tHXC8	XCLK. H. pulse width	2tosc-20	—	—	nsec
tLXC8	XCLK. L. pulse width	2tosc-20	—	—	nsec
tXY8	XCLK ↓ → YCLK ↑	1.5tosc-10	—	—	nsec
tYX8	YCLK ↓ → XCLK ↑	tosc-10	—	—	nsec
tDXC8	Data determination → XCLK ↓	2tosc-10	—	—	nsec
tXCD8	XCLK ↓ → Data retention time	2tosc-20	—	—	nsec
tHY8	YCLK . H. pulse width (Note 1)	(4n-1/2) tosc-20	—	—	nsec

Note 1: n is the value of YW.

· LCD interface timing (3)



(Ta=-20°C to 75°C)

Code	Item		Min	Typ	Max	Unit
t_{HFLM}	FLM. H. pulse width	(Note 1)	(m+n) 2tosc-20	—	—	nsec
		(Note 2)	(m+n) 4tosc-20	—	—	nsec
t_{FLMYH}	FLM ↑ → YCLK ↑	(Note 1)	4.5 · tosc-20	—	—	nsec
		(Note 2)	5.5 · tosc-20	—	—	nsec
t_{FLMYL}	FLM ↑ → YCLK ↓	(Note 1)	(n+2) · 2tosc-20	—	—	nsec
		(Note 2)	(n+5/4) · 4tosc-20	—	—	nsec
t_{YFLM}	YCLK ↓ → FLM ↓	(Note 1)	(m-2) · 2tosc-20	—	—	nsec
		(Note 2)	(m-5/4) · 4tosc-20	—	—	nsec
t_{YM}	YCLK ↓ → M ↑ ↓		-100	—	—	nsec

Remarks: m is the value of C/R.

n is the value of YW.

Note 1: Applicable to the 4-gradation display mode.

Note 2: Applicable to the 8-gradation display mode.