NATIONAL HYBRID, Inc.

Multi-Protocol Data Bus Interface

NHi-RT Expanded Memory Remote Terminals

User's Manual

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TABLE OF CONTENTS

TABLE OF CONTENTS(continued)

TABLE OF CONTENTS(continued)

1.0.0 SCOPE

This document defines the functional and electrical specification for National Hybrid's series of MIL- STD- Data Bus Expanded Memory Remote Terminals (NHi- RT).

2.0.0 NHi-RT PROTOCOL COMPLIANCE

MIL- STD- 1553A
MIL- STD- 1553B Notices I and II
MIL- STD- 1760B
MCAIR MDC A3818, A5690, A4905, A5332
EFA/ STANAG- 3838 requirements for Eurofighter Aircraft

3.0.0 INTRODUCTION

The NHi- RT is a low cost complete **Multi-Protocol** Mil- Std- Data Bus Interface between a dual redundant bus and a host processor. The device functions as a programmable Remote Terminal containing a protocol chip, two +5V monolithic transceivers and 16K word SRAM. The unit is available packaged in a 1.1" x 1.1" 69 pin ceramic PGA, or 1.1" x 1.1" 68 pin ceramic quad flatpack. The only external components required are two coupling transformers.

The NHi- RT appears to the host computer as 16K words of 16 bit wide memory controlled by standard RAM signals. The device can thus be easily interfaced with all popular processors and buses. The built in interrupt controller supports an internal FIFO which retains header information for queuing up to 6 pending interrupt requests plus an overflow interrupt.

All modes of operation access data tables via pointers residing in RAM which facilitates multiple buffering. This allows buffers to change without moving data and promotes efficient use of RAM space. The data tables have programmable sizes and locations.

The NHi-RT is plug in compatible with the popular NHi-ET full function family and the 4K word remote terminal family with no changes to hardware or software required.

3.1.0 FEATURES

The NHi- RT 16K word family is form, fit, and function compatible to all the NHi- data bus interface parts. This interchange ability gives the user a high degree of flexibility when configuring a system around the NHi family of parts.

3.1.1 GENERAL FEATURES

- Mulit-Protocol Interface
- Single +5 volt supply.
- Operates from 10 Mhz clock.
- Contains two monolithic +5V transceivers
- Appears to host as a Dual Port Double Buffered 16K x 16 SRAM
- Footprint less than 1.00 square inches
- Ensures integrity of all shared data and control structures
- Built- in interrupt controller
- Internal FIFO is configurable to retain header information for queuing up to 6 pending interrupt requests plus an overflow interrupt, or as a 7 interrupt revolving FIFO
- Provides interrupt priority input and output pins for daisy- chaining interrupt requests
- Contains a Timer Unit which provides 32 bit RTC (Real- Time- Clock) with 1, 2, 4, 8, 16, 32 and 64 uS internal, or user provided external clock resolution for data and event time tagging.
- Interfaces with an 8 bit discrete I/ O bus
- Selectable 768/ 672 us Failsafe Timer with complete Testability
- Low power CMOS technology

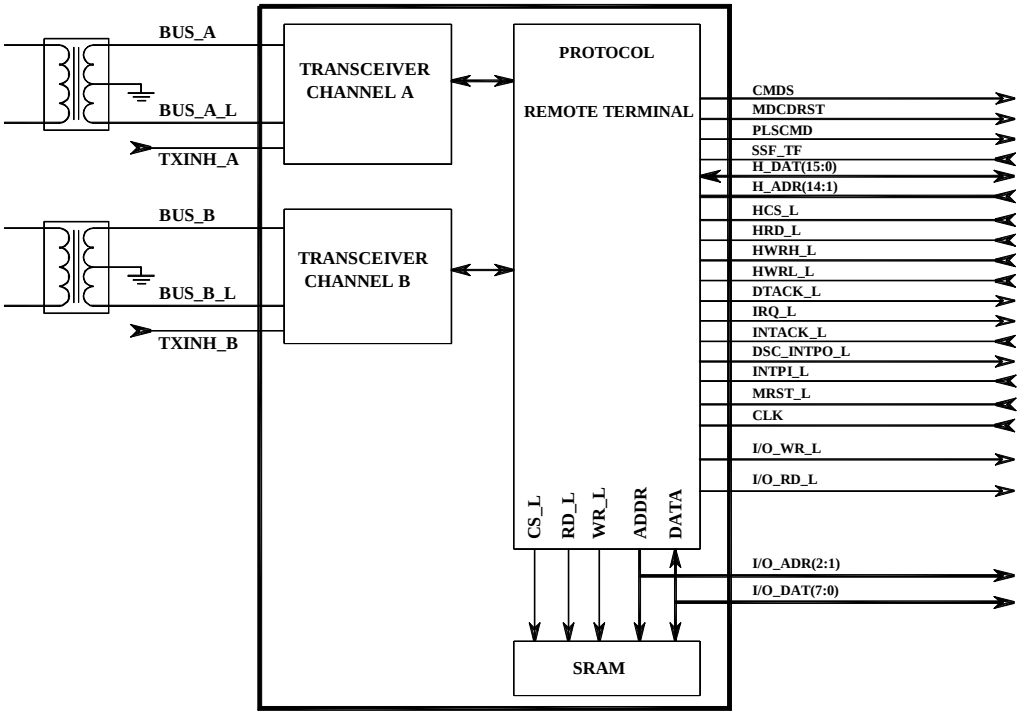
3.1.2 REMOTE TERMINAL HIGHLIGHTS:

- DBCA_ L bit is controlled in configuration register.
- Message Illegality is internally programmable. DOES NOT require external PROMS or glue logic.
- Employs data tables with individual tag words which indicate whether or not the data is valid, updated since last read, in the process of being updated, was received via broadcast command, or has been lost (i. e. updated more than once by a receive message before being read).
- Optionally sets the subsystem flag bit whenever stale data is transmitted or received data is overwritten.
- Issues interrupts on any subset of T/ R bit, subaddresses, mode commands, broadcast messages and errors.
- Provides interrupt priority input and output pins for daisy- chaining interrupt requests. messages.
- Optionally resets the real- time clock in response to a "Synchronize" mode command.
- Optionally updates the lower 16 bits of the real- time clock in response to a "Synchronize WithData" command.
- Indicates the reception of specific commands by outputting pulses on any one of 8 pins.
- Internally loops- back messages under host control for test purposes.
- Employs a decoder algorithm which ensures high noise immunity and a low error rate.
- Software RT Address Lockout.
- MDC3818 Status Response, Error Handling, Status Bit Definition, Mode Code Operation.
- Separate Broadcast Interrupts.

3.2.0 BLOCK DIAGRAM

The NHi- RTs contains two +5 volt transceivers, an ASIC, and an SRAM. The ASIC performs all multi protocol functions of a REMOTE TERMINAL. It controls accesses to the RAM such that it appears to the host CPU 16bit wide dual port memory.

Since the NHi- RT appears to its host as RAM, no external logic is required when interfacing to the device. It is simply connected to the CPU's address bus, Mil Bus, and control lines. There are NO EPROMS required to illegalize commands. Illegalization is performed internal to the protocol chip in the NHi- RT.The user sets up command illegalization when the NHi- RT is initialized. See sections on Message Illegalization and Host Initialization.



NHi-RT EXPANDED MEMORY FUNCTIONAL BLOCK DIAGRAM

The NHi- RT can be interfaced to an 8 bit data bus by folding the upper and lower bytes on top of each other and performing byte wide data transfers.

By default, the host has priority in accessing the I/ O bus. When the host requests access to a device already in use by the protocol chip, the host *DTACK signal is delayed by the NHi- RT. If either side (protocol chip or host) waits for access during the current cycle, it is automatically granted priority for the next cycle. The host can retain priority for successive cycles accessing the same address (this is required to guarantee the proper operation of host read- modify- write instructions - see pin *HCS for details) by keeping *HCS low.

3.3.0 PROTOCOL CHIP DESCRIPTION

The protocol chip contains the following modules:

Host Bus Interface Unit	(HBIU)
I/ O Bus Interface Unit	(IBIU)
Interrupt Controller Unit	(ICU)
Dual Redundant Multi Protocol Front End	(DRFE)
Message Processor Unit	(MPU)

3.3.1 HOST BUS INTERFACE UNIT

The HBIU provides a standard RAM interface to the host bus. The module performs the following functions:

Provides NHi- RT device select and decodes host address to select registers.
Transfers data between the NHi-RT and the host (word and byte mode as well as read-modify- write are supported).
Provides priority input and output for daisy chaining host interrupts.
Outputs *DTACK signal indicating end of bus cycle.

3.3.2 I/O BUS INTERFACE UNIT

The IBIU controls the RAM and I/ O residing on the I/ O bus so that it appears to the host as a pseudo dual port RAM (i. e., shared memory). The unit implements the following functions:

Arbitrates between host and protocol chip initiated accesses to the RAM and host data bus.
Decodes address lines to select device (e. g. RAM, external byte- wide I/ O, external terminal address buffer, command output register).
Generates control signals to access the selected device.

3.3.3 INTERRUPT CONTROL UNIT

The ICU is an 8 input vectored interrupt controller. It contains eight registers as well as a FIFO for storing pending interrupt vectors.

3.3.3.1 ICU REGISTERS

The ICU contains the following registers

INTERRUPT REQUEST register (IRR)
INTERRUPT MASK register (IMR)
INTERRUPT VECTOR register (IVR)
AUXILIARY VECTOR register (AVR)

The INTERRUPT REQUEST register samples 8 inputs originating from internal modules. Since the host can write to this register, all interrupt sequences can be software driven for program debugging. The inputs and their priorities (level 7 has highest priority) are described in the following table.

3.3.3.1.1 INTERRUPT DEFINITION TABLE

PRIORITY	RTU INTERRUPT
0	VALID TX/RX EOM
1	INVALID TX/RX EOM
2	VALID MODE CODE
3	INVALID MODE CODE
4	FIFO OVERFLOW
5	VALID BROADCAST
6	INVALID BROADCAST
7	FAILSAFE TIMEOUT

Note: RT Interrupts 5 & 6 are enabled only when separate Broadcast Tables are used. Masking interrupt 4 creates a revolving Fifo.

As soon as an interrupt is requested, its vector is pushed onto the FIFO - so the chronological

order of the requests normally determines the order in which they will be serviced. Simultaneous requests, however, are pushed onto the FIFO according to the priority of the pending interrupts.

The INTERRUPT MASK register masks the corresponding inputs to the INTERRUPT REQUEST register. The INTERRUPT VECTOR register holds the 3 bit interrupt priority level and an additional 5 bit field (see paragraph on INTERRUPT VECTOR register for details).

The AUXILIARY VECTOR register contains an additional byte of information related to the interrupt request (see paragraph on AUXILIARY VECTOR register for details).

3.3.3.2 ICU FIFO

The ICU FIFO is 16 bits wide and 7 words deep. Whenever an unmasked interrupt request is issued by the message processor, a word is pushed onto the FIFO. When an interrupt is acknowledged by the host, a word is popped from the FIFO and used to update the IVR and the AVR.

The host can read the FIFO by simply popping its contents. This is done by reading the FIFO located at address 8 (refer to address map). The interrupt request output, *IRQ, will go inactive after the FIFO is emptied in this way.

The host can mask the *IRQ output by resetting the INTERRUPT REQUEST ENABLE bit in the CONTROL register; however this does not prevent the device from pushing interrupt requests onto the FIFO.

If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the vector which caused the overflow is pushed onto the FIFO. As a result, the 2 oldest vectors are lost. All further pushes are then inhibited until the host pops the vector indicating the overflow.

The above mechanism ensures that the host will always be notified of FIFO overflows and will always obtain the 2 interrupt vectors immediately preceding the overflow condition.

If interrupt 4 is masked, the FIFO operates in the revolving mode; vectors are continuously pushed onto the FIFO. After the 7th vector is pushed without any pops, each additional vector pushed causes the oldest vector to be lost.

The FIFO can be emptied by writing (any value) to address 8 (in words).

3.3.4 DUAL REDUNDANT FRONT END

The DRFE performs serial to parallel and parallel to serial conversion as well as basic format and timing validation. The unit contains the following:

Manchester encoders/ decoders
Gap counter
No response counter
Minimum response time counter
Timeout counter

3.3.4.1 MANCHESTER DECODER

The decoder translates serial Manchester bi- phase signals to 16- bit words and outputs the following signals:

Valid command word received
Valid data word received
Invalid word received (parity, incorrect bit count, invalid Manchester encoding, gap)
Broadcast command received

Begin new message (i. e., end of a valid legal command for this Remote Terminal)

3.3.4.2 MANCHESTER ENCODER

The encoder receives 16 bit words and transmits them with the appropriate sync and parity as a serial Manchester bi- phase signal. The outputs of the encoder can be loop- backed into either decoder for test purposes.

3.3.4.3 GAP COUNTER

The gap counter checks contiguity of successive words. If the time between "contiguous" words (measured from zero- cross of parity to zero- cross of sync) exceeds 3.5 - 3.7 microseconds, the message is invalidated.

3.3.4.4 RT - RT NO RESPONSE COUNTER

The no response counter checks the response time of the transmitting RT in a RT to RT transfer. If the response time is exceeded, the message is invalidated. The response time is software programmable (14, 18, 26, 42 microseconds) to accommodate systems with long cables and/ or slow terminals.

3.3.4.5 MINIMUM RESPONSE TIME COUNTER

The minimum response time counter ensures that the response will be no sooner than 4 microseconds
(measured from zero- cross of parity to zero- cross of sync).

3.3.4.6 FAIL -SAFE TIMEOUT COUNTER

This counter inhibits the encoder outputs and issues a TIMEOUT interrupt whenever continuous transmission exceeds 768/ 672 microseconds. Transmission will remain inhibited until a command is received on the same bus or the part is reset.

3.3.5 MESSAGE PROCESSOR UNIT

The MPU forms the heart of the protocol chip and controls the operation of the Decoders, Encoders, and Interrupt Controller. This unit is activated by the reception of a valid legal command addressed to the RT.

The MPU performs the following functions:

Recognizes the various message types for the RT and responds with the appropriate sequence of control signals.
Validates format and timing of received data words.
Checks command legality.
Responds with status/ data.
Calculates all addresses for accessing the RAM and discrete I/ O.
Updates RAM data table contents, including tag words.
Optionally time tags data tables.
Issues interrupt requests to the ICU.
The maximum response time of the NHi- RT less than 6.0 microseconds (measured from zero- cross to zero- cross).

3.4.0 RT HARDWIRE TERMINAL ADDRESS

The terminal address of the NHi- RT can be hardwired using I/ O DAT(5: 0). I/ O DAT(4: 0) are used for the terminal address, I/ O DAT0 being the LSB, and I/ O DAT5 is used to set odd parity in the address. These pins CANNOT be directly connected to +5 or ground since the I/ O data bus drives the NHi- RT's internal RAM.

The address must be wired using pull- up and pull- down resistors. There are 64K internal pull- up resistors in the protocol chip, so only external pull- down resistors of 4.7K are required. The Hardwire Address is read and loaded into the terminal at Power- On Reset, Hardware Reset, and Software Reset.

The terminal address can be changed at any time through software by writing a new address to the Basic Status Register, however, if any of the above resets occur, the Hardwire Address will be re- loaded into the terminal. The software address can be locked out by setting Bit2 in Configuration Register 1.

4.0.0 DATA STRUCTURE

4.1.0 ADDRESS MAP

The NHi- RT appears to the host as 16K words of memory divided into the following blocks:

ADDRESS RANGE	DESCRIPTION
0 -- 30	INTERNAL REGISTERS
31	I/O TAG WORD
32 -- 35	I/O SPACE
64 -- 16383	SHARED RAM

INTERNAL REGISTER MAP

ADDRESS	REGISTER DEFINITION	ACCESS
0	CONTROL	R/W
1	POINTER TABLE ADDRESS	R/W
2	BASIC STATUS	R/W
3	INTERRUPT MASK(lower byte)	R/W
3	INTERRUPT VECTOR(upper byte)	R
3	INTERRUPT REQUEST(upper byte)	W
4	INTERRUPT VECTOR(lower byte)	R/W
4	AUXILLARY VECTOR(upper byte)	R
4	RESERVED(upper byte)	W
5	REAL TIME CLOCK HIGH WORD	R
6	REAL TIME CLOCK LOW WORD	R
7	REAL TIME CLOCK CONTROL	R/W
8	READ FIFO	R
8	RESET FIFO	W
9	CONFIGURATION 1	R/W
10	RESERVED	
11	LAST COMMAND	R
12	LAST STATUS	R
13	RESERVED	
14	RESERVED	
15	RESET TERMINAL(both bytes)	W
16	RESERVED	
17	RESERVED	
18	ENCODER STATUS	R
19	CONDITION	R
20	RESERVED	
21	CONFIGURATION 3	R/W
22	RESERVED	
23	ENCODER DATA*	R/W
24	ENCODER DATA TX REQUEST*	W
25	ENCODER COMMAND TX REQUEST*	W
26	RESERVED	
27	RESERVED	
28	RESERVED	
29	RESERVED	
30	EXTERNAL RTU ADDRESS BUFFER(lowre byte)	R
30	COMMAND OUTPUT PINS	W
31	I/O TAG WORD	R/W

DO NOT WRITE TO RESERVED REGISTERS.

*In order to write to addresses 23, 24, or 25, the RT must be in loop- back mode (see CONTROL register for details).

4.2.0 INTERNAL REGISTERS

4.2.1 CONTROL Address: 0 R/ W

This register controls the general operation of the NHi- RT.

15	14	13	12	11	10	9	8
HWD	RSP1	RSP0	TSTFST	NBCST	TXINH	LOOPB	LOOPA
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IRE	MIO	CMDO	SRQRST	SSF_TF	NTAG	BINH	AINH

HWD **Bits: 15**

1 = Enables high word detection.
This option allows extra words in a message to be detected,as required by some protocols.
0= Tterminal does not detect high word errors.

RSP1, RSP0 **Bits: 14,13**

These bits define the response timeout for RT- RT messages:

RSP1	RSP0	TIMEOUT(us)
0	0	14
0	1	18
1	0	26
1	1	42

TSTFST **Bits: 12**

1= Enables testing of the FAIL SAFE time out.
When this feature is enabled, the RT will transmit continuously once it is enabled by a valid message. The encoder will be inhibited after 768/ 672us. It will be enabled by a reset or the reception of another valid message. If this bit is set to 0 during an RT transmission, before the required number of words have been transmitted, the encoder will return to normal operation and stop at the proper message length.. If it is set to 0 after the message length has been exceeded, the current word will be completed and normal operation resumed.
This feature can be used in the LOOPBACK mode to automatically transmit data words.
The RT encoder will remain in the tester mode until the CPU sets this bit to 0.

The TSTFST Bit Must Always Be Set to Zero During Normal Operation!!!

NBCST **Bits: 11**

1= Specifies that broadcast commands WILL be ignored by the RT.

TXINH **Bits: 10**

1= Inhibits transmission by forcing TXA= TXAN= 0 and TXB= TXBN= 0.

LOOPA(B) **Bits: 9, 8**

1= Defines that decoder A (B) inputs shall be connected internally to the encoder outputs rather than the transceiver for test purposes.

IRE **Bits: 7**

1= Globally enables the interrupt request output, *IRQ.
0= Disables all interrupt requests; however, interrupt vectors are still pushed onto the FIFO.

MIO **Bits: 6**

1= Defines that certain reserved mode commands with data shall be legal and access the I/ O bus without dependence on host initialization or the BUSY bit in the BASIC STATUS register. This feature can be used, for example, to set a watchdog timer or read a hardware status register via the Mil bus even though the host's state may be undefined.

The I/ O operations are restricted to the data word's lower byte. The mode commands and their corresponding I/ O addresses in decimal are as follows:

T/R	MODE CODE	I/O ADR(2,1)	I/O WR_L	I/O RD_L
T	24	00	1	0
T	25	10	1	0
R	27	10	0	1
R	28	00	0	1

CMD0 **Bits: 5**

0= Specifies that after a legal valid command is received, a pulse shall be outputted on a pin specified by the PULSE field in the corresponding data table tag word. The pulse is activated together with 2 I/ O control signals (CMDS= 1 and *I/ O WR = 0).

1= Specifies that after a valid legal command is received, the word count/ mode code field (together with CMDS= 1 and *I/ O WR = 0) shall be outputted on the 5 least significant bits of the discrete I/ O bus. (Although the protocol chip outputs the entire command, only 5 bits are outputted by the NHi- RT due to pin- out restrictions).

SRQRST **Bits: 4**

1= Specifies that the service request bit in the STATUS word will be reset upon reception of a valid "Transmit Vector Word" mode command.

SSF_ TF **Bits: 3**

0= Specifies that the Sub- System Flag in the 1553 status word will be determined by the value of the SSF_ TF pin.

1= Specifies that the Terminal Flag in the 1553 status word will be determined by the value of the SSF_ TF pin.

NTAG **Bits: 2**

1= Specifies that all the data tables shall be without tag words. This mode of operation can be used to store received data from several subaddresses into a contiguous block without interspersed tag words. This feature can facilitate, for example, software upload.

BINH **Bits: 1**

1= Disables reception on bus B.

AINH **Bits: 0**

1= Disables reception on bus A.

4.2.2 POINTER TABLE ADDRESS Address: 1 R/ W

This register holds the address of the table of pointers used by the RT when accessing data tables. The address is specified as a word address in the lower 4K of the memory space. After POR the register is initialized to 1000 (hex), with D1 as the LSB of the word address. D0 is a DON'T CARE and should be set to 0.

Note: The RT pointer table must always be located in the lower 4K words of memory.

4.2.3 BASIC STATUS Address: 2 R/ W

This register defines the terminal address as well as default values for all status bits. The 1553 status word is OR'ed with this register before transmission. The bits in the BASIC STATUS register correspond to the bits in the STATUS register and their function is defined in MIL- STD-1553B. They can be redefined for other protocols.

15	14	13	12	11	10	9	8
TADR4	TADR3	TADR2	TADR1	TADR0	M_ERR	INSTR	SREQ
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD2	RSVD1	RSVD0	BCR	BUSY	SSF	DBCA	TF

The mechanism employed by the protocol chip for initializing the terminal address is designed to avoid dedicated pins. Upon POR the terminal address and its parity are automatically read from address 30 on the I/ O bus. The value can be supplied in 2 ways: by enabling the output of an external terminal address buffer or by employing pull- up/ down resistors to define a default value for the 6 least significant bits of the I/ O data bus. Odd parity is used to define a valid terminal address; even parity will inhibit reception on both buses. After POR, the host can change the terminal address through software by writing to the TADR field with any desired value. In addition, this operation will enable reception. Providing Bit 2 of Configuration Register is set to "0".

The host can check the validity of the parity bit obtained from the I/ O bus by reading address 30; if the most significant bit in the lower byte equals 1, the parity is invalid.

If the TADR is not defined externally (by pull- down resistors or a buffer), there is no danger of a false response before host initialization because internal pull- up resistors on the I/ O bus guarantee an incorrect terminal address parity.

When BUSY= 1, 1553 message accesses to the RAM are inhibited, however the RT will respond with status as required by MIL- STD- 1553B. The mode commands "Transmit Status Word", "Transmit Last Command Word", "Reset Remote Terminal", "Transmitter Shutdown", "Override Transmitter Shutdown" and the reserved mode commands legalized by MIO (see the CONTROL register for details) are not affected by BUSY. In addition, all output pulses issued after valid command reception are inhibited when BUSY= 1 (except for the signal MDCDRST which is pulsed after receiving the mode command "Reset").

After POR(MRST), BUSY is set to "1"; this prevents the RT from using undefined pointers before the host has had a chance to initialize the POINTER TABLE. The default value for all other status bits is "0" and the TADR field is loaded with the hardwired address.

The BUSY Bit in the LAST STATUS REGISTER is cleared on receipt of the first command after a RESET, except if that command is TRANSMIT LAST STATUS or TRANSMIT LAST COMMAND mode command.

The BUSY Bit in the LAST STATUS REGISTER can be cleared by bit using BIT 5 in the RTC CONTROL REGISTER. See RTC CONTROL REGISTER for details.

4.2.4 INTERRUPT REQUEST Address: 3(Ubyte) W

The INTERRUPT REQUEST register holds 8 types of interrupt requests (see section on INTERRUPT CONTROL UNIT for details). Interrupt requests are active high and upon POR the register is cleared (see initialization section).

15	14	13	12	11	10	9	8
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0

4.2.5 INTERRUPT MASK Address: 3 Lbyte R/ W

The INTERRUPT MASK register masks the corresponding interrupts. Upon POR, all interrupts are masked (see initialization section).

7	6	5	4	3	2	1	0
IMSK7	IMSK6	IMSK5	IMSK4	IMSK3	IMSK2	IMSK1	IMSK0

4.2.6 INTERRUPT VECTOR Address: 3(Ubyte) R
INTERRUPT VECTOR Address: 4(Lbyte) R/ W

The IVR is read only in the upper byte at address 3 and is read/ write in the lower byte at address 4. It contains interrupt header information which is popped off the FIFO.

ADDR3(4)	15(7)	14(6)	13(5)	12(4)	11(3)	9(2)	10(1)	8(0)
BIT	D4	D3	D2	D1	D0	L2	L1	L0

The Interrupt Vector register is loaded with LLL data from the fifo when it is popped. The fifo is popped by a hardware interrupt ackowledge or a read to address 8. This register in undefined at POR.

L(2: 0)
This is the interrupt priority determined by the message processor.

D(4: 0)
The DDDDD field is inputted by the CPU. This is used as an offset for the interrupt vector. During a hardware interrupt acknowledge, this register is outputted on the upper and lower bytes of the CPU data bus.

4.2.7 AUXILIARY VECTOR REGISTER Address: 4(Ubyte) R

This register contains additional information related to the interrupt request. The data is popped from the FIFO and latched into the AVR during the interrupt acknowledge cycle or whenever the FIFO is popped by a host read instruction to address 8. Upon POR, this register is undefined.

MODE	15	14	13	12	11	9	10	8
RTU	EMP	BUS	T/R	SADR4 MODE4	SADR3 MODE3	SADR2 MODE2	SADR1 MODE1	SADR0 MODE0

EMP **Bits: 15**
1= Fifo empty. Ignore data.
0= Fifo data valid. Use data.

BUS **Bits: 14**
0= Indicates that the message was on bus A
1= Indicates that the message was on bus B.

T/ R **Bits: 13**

0= Indicates a receive message.
1= Indicates a transmit message.

SADR / MODE **Bits: (12-8)**

This field defines the sub- address or mode code.
Note: the interrupt level distinguishes between regular transmit/ receive commands and mode commands.

4.2.8 REAL- TIME CLOCK

RTC HIGH WORD **Address: 5** **R**
RTC LOW WORD **Address: 6** **R**

The RTC is a 32 bit up- counter which can be used for time- tagging. If the time- tagging option is in effect, the RTC is sampled and stored in 2 words in the data table The most significant word is stored first.

When messages are time- tagged, the host should not write data to the first 2 locations following the data table tag word since they will be overwritten with the value of the message time tag.

The RTC can be reset by the mode command "Synchronize Without Data" and the least significant 16 bits can be updated by "Synchronize With Data". The full 32 bits can be updated using the first two data words in a receive command. See RTC CONTROL REGISTER for details.

The RTC can be read and reset by the host at any time. Since the RTC consists of 32 bits, at least 2 memory cycles are required to read all of its value. As a result, a carry- out from the lower word can occur between the read cycles. A mechanism is therefore provided to solve this potential difficulty.

If the host reads the RTC as two 16 bit words, *LOCK should be initialized to 1 in the RTC CONTROL register. In this case, when the host reads the upper word, all 32 bits are latched into the host output register. The value in the output register remains unchanged until the host finishes reading the lower word of the RTC.

If the host reads the RTC in bytes, *LOCK should be initialized to 0. In this case, when the host reads any of the bytes of the RTC, all 32 bits are latched into the host output register and its value remains unchanged until updating is re- enabled by reading the RTC CONTROL register. The RTC resolution can be programmed equal to 1, 2, 4, 8, 16, 32, or 64 microseconds.

4.2.9 RTC CONTROL REGISTER Address: 7 R/ W

The RTC CONTROL register controls the RTC as well as having other functions.

15	14	13	12	11	10	9	8
RTC RESET	RESET LAST	RES2	SYNUPD	*LOCK	SYNRST	RES1	RES0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M1760	BUSY OPT	RESET BUSY	PRESET 4	PRESET 3	PRESET 2	PRESET 1	PRESET 0

RTC RESET **Bits: 15**

When a "1" is written to RTC RESET, a reset pulse is issued to the RTC. The contents of the register are not affected by this operation and RTC RESET is always read by the host as "0".

RESET LAST **Bits: 14**

When a "1" is written to RESET LAST, all the bits in the LAST STATUS REGISTER except the ADDRESS field and the BUSY bit are set to a "0". The contents of the register are not affected by this operation and RESET LAST is always read by the host as "0".

SYNUPD **Bits: 12**

1= Specifies that the lower 16 bits of the RTC will be updated whenever a valid mode command "Synchronize With Data" is received by the RT.

***LOCK** **Bits: 11**

0 = Enables updating of the host output register after the RTC CONTROL register is read (this feature is needed to support byte wide read cycles).

1 = Enables updating of the host output register after the lower RTC word is read.

SYNRST **Bits: 10**

1= Specifies that the RTC shall be reset whenever a valid mode command "Synchronize Without Data" is received by the RT.

RES **Bits: 13, 9, 8**

This field defines the resolution of the RTC in microseconds as follows:

RESOLUTION(us)	13	9	8
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
OFF/EXT	1	1	1

Note: Some NHi- RT device types have an external TIME TAG CLOCK input.

M1760 **Bits: 7**

1= Specifies that the RT shall comply with MIL- STD- 1760A. This mode of operation has two consequences: first, the mode command "Synchronize With Data" updates the lower 16 bits of the RTC only if the least significant data bit is "0" and second, the IPO_ DSC pin serves as a store disconnect signal rather than an interrupt priority output.

0= Specifies that the RT shall comply with MIL-STD-1553B.

BUSY _OPT **Bits: 6**

0= MRST, Software Reset and MODE CODE_ 08 RESET will set the BUSY bit in the LAST STATUS REGISTER and the BASIC STATUS REGISTER to a "1".

1= Only MRST will set the BUSY bit in the LAST STATUS REGISTER and the BASIC STATUS REGISTER to a "1".

RESET BUSY **Bits: 5**

When a "1" is written to RESET BUSY, the BUSY bit in the LAST STATUS REGISTER is set to a "0". The contents of the register are not affected by this operation and RESET BUSY is always read by the host as "0".

PRESET **Bits: (4: 0)**

These bits provide a method to perform a double word(32 bit) preset to the RTC. When this bit field is set to any number from 1 to 30(bit 0 = LSB), the first two words of a receive message whose subaddress is equal to this value will be used to preset the internal RTC. The most significant word is received first. If this field is equal to a "0" or "31", the RTC will not be preset. All bits in this register are cleared during initialization of the RT.

4.2.10 FIFO READ Address: 8 R

This address is used to read the contents of the interrupt FIFO. Reading this address pops the FIFO, updates the IVR and the AVR; then outputs the AVR(upper byte) and IVR(lower byte).

4.2.11 FIFO RESET Address: 8 W

Writing any value to this address empties the FIFO.

4.2.12 LAST COMMAND REGISTER Address: 11 R

This register holds the last command word as defined by MIL-Bus. The contents are not defined after initialization of the RT.

4.2.13 LAST STATUS REGISTER Address: 12 R

This register holds the last status word as defined by MIL- STD- 1553B. After initialization of the BUSY bit= 1, the TADR field contains the hardwire address, and all other bits are set to 0. See RTC CONTROL REGISTER for special options.

4.2.14 RESET REMOTE TERMINAL Address: 15 W

Writing a word to address 15 resets the RT and causes it to perform its initialization (see initialization section).

4.2.15 ENCODER STATUS Address: 18 R

This register contains flags indicating the status of the encoder. These flags are intended to facilitate transmission of messages in loop- back mode during self- test.

15	7	0
TXREQ_L	EOTX_L	FAILSAFE_L

TXREQ_ L **Bits: 15**

0= Indicates that the encoder is ready to accept the next word for transmission. This bit should equal "0" before loading the Encoder Data register with the next word. In order to transmit contiguous words, the next word should be loaded within 18 microseconds after *TXREQ transitions to "0".

EOTX_ L **Bits: 7**

0= Indicates that the encoder has completed transmission and that there are no pending requests.

FAILSAFE_ L **Bits: 0**

0= FAILSAFE TIME OUT has occurred. This bit will be set to a "1" when a new message is received or during a reset.

4.2.16 CONDITION REGISTER Address: 19 R

This register contains information about the command being processed by the NHi- RT. and the operational condition.of the NHi-RT.

15	14	13	12	11	10	9	8
X	X	AXEN	BXEN	TFE	X	MDCD_L	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

AXEN **Bits: 13**

1= Indicates that transmitter A is enabled. This bit is set to a "1": at POWER UP, if the NHi- RT is RESET, after receipt of a "Reset" mode code, or after receipt of an OVERRIDE TRANSMITTER SHUTDOWN mode code on the B bus.

0= Indicates that transmitter A is inhibited. This bit is set to a "0" after receipt of TRANSMITTER SHUTDOWN mode code on the B bus.

BXEN **Bits: 12**

1= Indicates that transmitter B is enabled. This bit is set to a "1": at POWER UP, if the NHi- RT is RESET, after receipt of a "Reset" mode code, or after receipt of an OVERRIDE TRANSMITTER SHUTDOWN mode code on the A bus.

0= Indicates that transmitter B is inhibited. This bit is set to a "0" after receipt of a TRANSMITTER SHUTDOWN mode code on the A bus.

TFE **Bits: 11**

1= Indicates that the TERMINAL FLAG bit in the status word can be set to a "1" . This can be done in the BASIC STATUS REGISTER or by the TERMINAL FLAG pin on the NHi-RT. This bit is set to a "1" at POWER UP, if the NHi- RT is RESET, after receipt of a RESET MODE CODE, or after receipt of an OVERRIDE INHIBIT TERMINAL FLAG mode code.

0= Indicates that the TERMINAL FLAG bit in the status word CANNOT be set to a "1". This bit is set to a "0" after receipt of an INHIBIT TERMINAL FLAG mode code.

MDCD_ L **Bits: 9**

1= Indicates that the last command received was NOT a mode code.

0= This bit is set to a "0" when a mode code is received.

4.2.17 ENCODER DATA REGISTER Address: 23 R/W

This register contains data to be transmitted when performing a loop back test.

4.2.18 ENCODER DATA TRANSMIT RQST Address: 24 W

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a data word. This instruction together with the ENCODER COMMAND TRANSMIT REQUEST can be used to loop- back entire messages for self- test purposes. The received data can be read from the data table associated with the command.

4.2.19 ENCODER COMMAND TRANSMIT REQUEST Address: 25 W

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a command word. This instruction is useful for sending commands to the decoder while in loop- back mode. The command can then be read from the LAST COMMAND register.

4.2.20 EXTERNAL TERMINAL ADDRESS REGISTER Address: 30 R

This register contains information about the hardwire terminal address.

7	6	5	4	3	2	1	0
INVALP	DISCON	TADRP	TADR4	TADR3	TADR2	TADR1	TADR0

The terminal address may be hardwired using I/ O DAT(5: 0). External pull- down resistors of 4.7K are used to set a low, 64K internal pull- ups set a high. I/ O DAT5 is wired for odd parity in the address. The hardwire terminal address and its parity can be obtained by reading I/ O address 30. This address is unique since a read operation activates both the I/ O bus command strobe and the I/ O bus read signal (i. e., CMDS= 1 and *I/ O RD= 0). As a result, a buffer containing the terminal address can be selected without decoding address lines.
If an external buffer is not desired, pull- up/ down resistors on the I/ O data bus can be used instead (see BASIC STATUS register for details). The protocol chip also calculates the terminal address's parity and compares it to the value obtained from the I/ O bus.

INVALP Bits: 7

1= Specifies that the terminal address which was read automatically by the protocol chip following reset (from I/ O address 30) had invalid parity.

DISCON Bits: 6

0= Specifies that the store is disconnected because a terminal address of 31 was detected on the I/ O bus for at least 800 nanoseconds.
1= Specifies that the store is connected.

This bit indicates the "disconnected store" condition defined by MIL- STD- 1760A, provided that the store contains the pull- down resistors used for defining the terminal address (see BASIC STATUS register for details). After the store is disconnected, the standby state of all I/ O lines will be high and will therefore define an illegal terminal address of 31.

TADRP Bits: 5

TADRP equals the value of the terminal address parity read from I/ O address 30.

TADR Bits: (4:0)

TADR equals the value of the terminal address read from I/ O address 30.

4.2.21 COMMAND OUTPUT PINS Address: 30 W

Writing a word to the COMMAND OUTPUT PINS (address 30 in the I/ O space) can be used to simulate the option which outputs 5 bits onto the I/ O bus following valid command reception (see CMDO bit in the CONTROL register for details). This address is unique since a write operation activates both the I/ O bus, COMMAND STROBE and the I/ O bus write signal (i. e., CMDS= 1 and *I/ O WR= 0). As a result, the bits can be latched without decoding address lines.

4.2.22 I/ O TAG WORD REGISTER Address: 31 R/ W

When a data table is mapped to address 32 in the I/ O space, its tag word is contained in this register. This tag word can be used, for example, to specify an output pulse whenever the data table is accessed. All other I/ O space data tables are without internal tag words and have no pulses associated with them.

4.2.23 CONFIGURATION REGISTER 1 Address: 9 R/ W

This register is used to configure the functionality of the part.

15	14	13	12	11	10	9	8
RSVD	RSVD	RSVD	RSVD	RSVD	3818 MODE	RSVD	RSVD
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	INHIBIT DBCA	RSVD	RSVD	INHIBIT SOFTADR	CONVERT BUSY BIT	SEP BCST TABLES

Note: Reserved Bits must be set to "0".

3818_ STATUS Bits: 10

0 = Status response and protocol operation as defined in Mil- Std- 1553B.
1 = Status response and protocol operation as defined in MDC A3818 and Mil- Std- 1553A.

INHIBIT DBCA Bits: 5

0 = DBCA bit in Status Word is set upon receipt of a valid DBCA Mode Code.
1 = Prevents DBCA Bit in Status Word from being set upon receipt of a valid DBCA Mode Code.

INHIBIT SOFT_ ADR Bits: 2

0 = Bits (15: 11) of Basic Status Register set the RT Address when a Write Operation to that register is performed. The Hard Wired Address sets the RT Address at RESET.
1 = Prevents software change of RT Address when writing to the Basic Status Register. Bits (15: 11) of Basic Status Register are “Don’t Care”. Only the Hard Wired Address sets the RT Address at RESET.

CONVERT BUSY BIT Bits: 1

0 = BUSY Bit is compliant with Mil- Std- 1553B.
1 = Converts BUSY Bit to Non- 1553B operation. BUSY Bit becomes a standard bit with no special functionality. BUSY Bit is not set during software reset or MODE CODE_ 08 RESET.

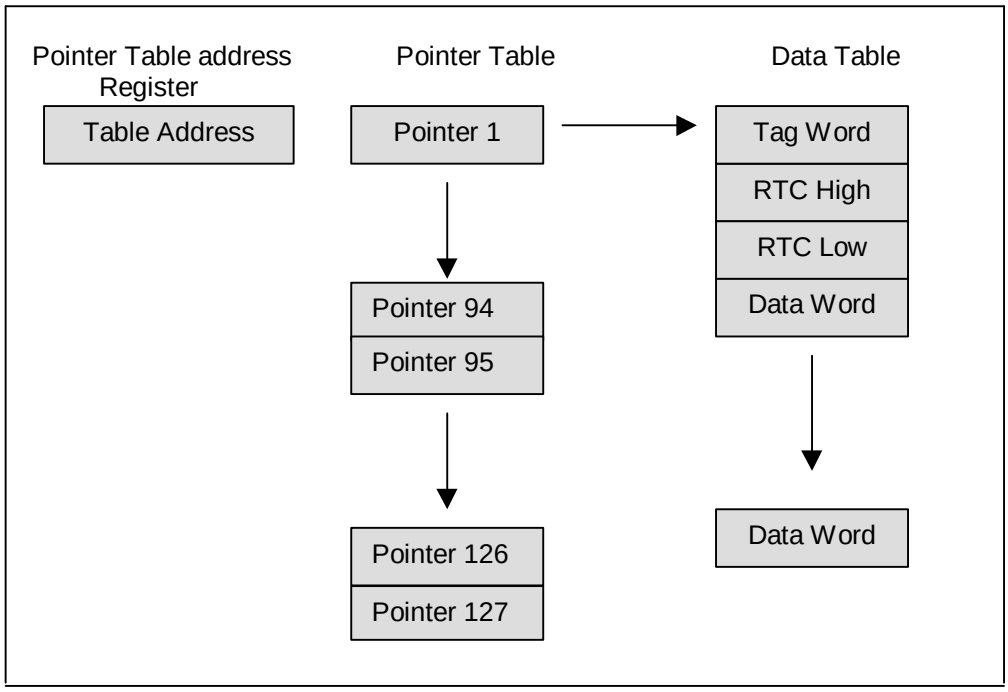
SEP_ BCST_ TABLES Bits: 0

0 = Broadcast messages use the same pointers as receive message:. therefore, receive and broadcast messages are stored in the same data tables. The BCST bit in the tag word is used to differentiate between the two message types.
1 = An additional 30 pointers are activated which puts receive and broadcast messages in separate data tables.

4.3.0 RT DATA TABLES

The data words associated with transmit/ receive/ broadcast messages and mode commands are stored in data tables. The data table addresses are stored in a POINTER TABLE located in the RAM. The data tables themselves can be individually allocated to either the RAM or the I/ O space. Data tables mapped to the I/ O space can be used for discrete I/ O without requiring host intervention. The mapping scheme is illustrated in the following diagram:

REMOTE TERMINAL MEMORY ORGANIZATION



The T/R bit subaddress and word count fields in the Command word are used to index into the Pointer table as defined below:

INDEX	T/R	SUBADDRESS	MODE CODE	COMMAND TYPE
0		NOT USED		
1 - 30	0	1 – 30		RECEIVE/BROADCAST
31	0	31 (Note 2)		
32		NOT USED		
33 - 62	1	1 – 30		TRANSMIT
63	1	31 (Note 2)		TRANSMIT
64 - 95	X	0, 31(Note 2)	0 - 31	MODE CODE
96		NOT USED		
97 - 126	0	1 – 30		BROADCAST
127	0	31 (Note 2)		BROADCAST

Note 1: Separate Broadcast Pointers are activated when BIT "0" of CONFIGURATION REGISTER 1 is a "1" (See this register for details).

Note 2: When 3818A/ 1553A protocol option is enabled, subaddress 31 is an extend subaddress, **Not a Mode Code Flag.**

4.3.1 MESSAGE ILLEGALITY

Commands are illegalized by setting the address field of the corresponding data table pointer to 0. When the protocol chip receives an illegal command, it responds with ME= 1 in the status; in addition, data transmission and storage are suppressed. All undefined mode commands are ignored.

4.3.2 REMOTE TERMINAL DATA TABLE TAG WORD

The data table's first word can be defined to be either a data word or a TAG WORD (see the NTAG field in the CONTROL register) which defines the table's status and associated options. The TAG WORD has the following format:

15	14	13	12	11	10	9	8
UPDATE	SSFENA	BCST	X	PULSE3	PULSE2	PULSE1	PULSE0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOCK	INVALID	OVRWRT	WCNT4	WCNT3	WCNT2	WCNT1	WCNT0

UPDATE **Bits: 15**

1= Indicates that the table was updated with data by the CPU or a 1553 message. The CPU should set this bit after writing to the table and reset the bit after reading the table.

SSFENA **Bits: 14**

1= Enables setting the subsystem flag in the status word whenever the RT transmits stale data or overwrites received data (i. e., whenever data is transmitted from a table with UPD= 0, or is stored into a table with UPD= 1).

BCST **Bits: 13**

1= Indicates that the table contains data from a valid broadcast message.
0= Indicates that the table contains data from a non- broadcast message.

PULSE(3: 0) **Bits: 11:8**

This field defines which pin should be pulsed at the end of a valid message which accesses the data table (see CMDO in the CONTROL register for details). The field is defined as follows:

PULSE FIELD VALUE	PULSED OUTPUT PIN
0	NO PULSE
1 – 8	I/O DATA(7..0)
14	PLSCMD PIN

LOCK **Bits: 7**

1= Indicates that the protocol chip is currently using the table for a message, either writing receive data or reading transmit data.

INVALID **Bits: 6**

1= Indicates that the table contains invalid data.

OVW **Bits: 5**

1= Indicates that data received from the 1553 bus caused the data to be overwritten before its previous contents were read by the host or that the host did not update the data since the last transmission (i. e., whenever data is transmitted from a table with UPD= 0, or is stored into a table with UPD= 1). This bit is similar to the subsystem flag returned to the Bus Controller when SSFENA= 1.

WCNT(4: 0) **Bits: 4-0**

This field contains the word count/ mode code in the command which referenced the data table.

4.3.3 DATA TABLE POINTER WORD

The Data Table Pointer Word has the following format:

15	14	13	12	11	10	9	8
INTREQ	RTCENA 1	ADDR 13	ADDR 12	ADDR 11	ADDR 10	ADDR 09	ADDR 08
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR 07	ADDR 06	ADDR 05	ADDR 04	ADDR 03	ADDR 02	ADDR 01	RTCENA 0

INTREQ **Bits: 15**

1= Specifies that an interrupt shall be issued after the completion of a message which accesses the data table and a header pushed on to the Fifo,.

0= No interrupt issued; nothing pushed on to Fifo.

ADDR(13: 1) **Bits: 13:1**

Defines the location of the RTU data table which MUST be in the lower 8K word address space. The RTU data tables always begin on word boundaries. The least significant bit of the word address is bit 1 in the Pointer word. If the data table address field is set to 0, the command associated with the pointer is illegalized.
with the pointer is illegalized.

RTCENA **Bits: 14,0**

Real Time Clock Time Tag Message Oprions. The Time_ Tag_ Transmit option will cause the first two transmitted words of the associated Transmit Command to contain the time tag, MSW first.

TIME TAG MODE	14	0
NO TIME TAG ON MESSAGES	0	0
NO TIME TAG ON MESSAGES	0	1
TIME TAG MESSAGES; DON'T TRANSMIT TIME TAG WITH TRANSMIT COMMAND	1	0
TIME TAG MESSAGES; TRANSMIT TIME TAG WITH TRANSMIT COMMAND	1	1

Note: If the No Time Tag option is used, data words occupy the time tag positions.

4.3.4 RT DATA TABLE BUFFERING SCHEME

Since the host and the NHi RT can access data tables asynchronously, data integrity must be ensured by a suitable buffering scheme. The method employed by the RT assumes that there are two pointer tables; one specifies data tables accessed by the RT and the other tables accessed by the host. The host's pointer table can reside anywhere in its memory space since it is never accessed by the RT. Data buffers are switched by the host exchanging pointers as explained below.

4.3.4.1 RT RAM ACCESS

When the RT wants to read or write to a data table, it fetches the corresponding data table pointer from its pointer table. It then sets the LOCK bit in the data table's TAG WORD to 1 and proceeds with the update. At the completion of the update, the RT sets the LOCK bit to 0 and also sets the UPDATE bit in the TAG WORD to 1 if it wrote to the data table or 0 if it read the data table. If the condition of the UPDATE bit at the start of the RT access indicates that the host has not read from or written to the data table since the last RT access to that table, the RT sets the OVRWRT bit in the TAG WORD to 1 to tell the host stale data has been transmitted by the RT or data has been overwritten by the RT.

Since the RT may fetch a data table pointer while the host is in the process of exchanging the corresponding pointers, there is a possibility that the RT's pointer will point to the table used by the host. In order to avoid this potential conflict, the host should check the LOCK bit in its data table tag word AFTER exchanging the pointers but BEFORE reading the data. If LOCK= 1, the host should wait until the protocol chip sets LOCK= 0.

NOTE: The LOCK bit is ALWAYS set in the TAG WORD of the data table accessed by the RT, irrespective of when the pointers are exchanged by the host. This is guaranteed because the RT reads the data table's pointer and sets the LOCK bit in the TAG WORD using a read - read - modify - write sequence which cannot be interrupted by the host (i. e., read POINTER - read TAG WORD - modify LOCK bit - write back TAG WORD with LOCK bit modified).

4.3.4.2 HOST RAM ACCESS

RECEIVE DATA TABLE
When the host wants to read the data in a RECEIVE data table, it **FIRST EXCHANGES** the pointer in its pointer table with the corresponding pointer in the RT's table. Then, the host reads the LOCK bit in the TAG WORD. If the LOCK bit is 0, the host proceeds with its access. If, however, the LOCK bit is 1, this informs the host that the RT is accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the RT. When the host finishes accessing the RECEIVE data table, it should clear the UPD bit in the data table's TAG WORD to 0. This will tell the RT the host has taken the data.

TRANSMIT DATA TABLE
When the host wants to write data to a TRANSMIT data table, the apparent method would be to load the table with data then exchange corresponding pointers. There is a subtle problem with this approach. If the host had, within a short period of time prior to this exchange previously loaded and exchanged these same pointers while the RT had been transmitting data from that data table , the LOCK bit could still be set in the table the the host was loading during the second sequence. This is possible because it can take up to 640us to transmit a message, the LOCK bit being set for the entire time. This could cause new data to be mixed with old data and transmitted. Avoiding this potential problem is quite simple.

When the host wants to access a TRANSMIT data table, it first reads the LOCK bit in the TAG WORD of the table belonging to the host. If the LOCK bit is 0, the host proceeds with its access and loads the data table . If, however, the LOCK bit is 1, this informs the host that the RT is still accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the RT. When the host finishes updating its TRANSMIT data table, it should set the UPD bit in the data table's TAG WORD to 1 and then exchange corresponding pointers. This will ensure that updated data for transmission is made available to the RT as soon as possible and inform the RT that it will be transmitting fresh data.

Since the host can change its table of pointers at any time, the above mapping scheme can be used to achieve any desired depth of buffering by simply employing a "round- robin" of pointers.

4.3.4.3 READ- MODIFY- WRITE
The host Read- Modify- Write cycle is used to support CPUs similar to the Motorola 680X0 where certain instructions (eg:, test and set) require two contiguous accesses to memory. Such accesses are unique in that the address remains active for both cycles.

5.0.0 REMOTE TERMINAL MODE CODE OPERATION

5.1.0 GENERAL

This section defines the operation of the NHi- RT when operating as an RT during reception of all the mode commands. The following terms are used in this section:

VALID COMMAND
A command meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

INVALID COMMAND
A command NOT meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

UNIMPLEMENTED COMMAND
A command not implemented by the NHi- ET.

The following general response characteristics apply to the NHi- RT when operating on the bus:

RECEIPT OF AN INVALID COMMAND
There is no response and the command is ignored.
RECEIPT OF AN UNIMPLEMENTED COMMAND
There is no response and the command is ignored.
RECEIPT OF AN UNDEFINED MODE COMMAND
There is no response and the command is ignored.

The following abbreviations are used in this discussion:

LSW = LAST STATUS WORD
CDR = CONDITION REGISTER
TW = TAG WORD IN DATA TABLE
ME = MESSAGE ERROR BIT
BCR = BROADCAST BIT

Additional information about each mode code is available in the Interrupt Vector register and the Auxilliary Vector register if it is set to be interrupt driven (see Data Table Pointer word, Interrupt Vector register and Auxiliary Vector register).

5.2.0 TABLE OF RT MODE CODE RESPONSES

5.2.1 DYNAMIC BUS CONTROL (00000; T/ R= 1)

Responds with status except if broadcast
Bits set: *MDCD to "0" in CDR

COMMAND+ DATA WORD
No status response
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW
INV to "1" in TW

T/ R= 0
UNIMPLEMENTED COMMAND

BROADCAST
UNIMPLEMENTED COMMAND

5.2.2 SYNCHRONIZE WITHOUT DATA (00001; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast
Bits set: *MDCD to "0" in CDR
If broadcast- BCR, BCST in LSW & TW to "1"

COMMAND+ DATA WORD
No status response
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW
INV to "1" in TW

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.3 TRANSMIT LAST STATUS WORD (00010; T/ R= 1)

VALID COMMAND
Responds with last status except if broadcast. Status NOT updated.
Bits set: *MDCD to "0" in CDR.

COMMAND+ DATA WORD
Status not cleared. No status response.
Bits set: *MDCD to "0" in CDR. INV to "1" in TW.
ME to "1" in LSW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.4 INITIATE SELF TEST (00011; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.5 TRANSMITTER SHUTDOWN (00100; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast. Transmitter on alternate bus inhibited.
Alternate bus transmitter re- enabled by: Reset mode code, Override Transmitter Shutdown mode code, resetting RT, or power up. Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "0" in CDR.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.6 OVERRIDE TRANSMITTER SHUTDOWN (00101; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast. Transmitter on alternate bus enabled.
Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "1" in CDR.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.7 INHIBIT TERMINAL FLAG (00110; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "0" in CDR. Terminal Flag inhibited in LSW.

If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.8 OVERRIDE INHIBIT TERMINAL FLAG (00111; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "1" in CDR. Terminal Flag enabled in LSW.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.9 RESET REMOTE TERMINAL (01000; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast. Both Transmitters enabled and Terminal
Flag enabled. Pointer base address register set to 2048 dec. External terminal address loaded.
Bits set: BUSY in LSW
If broadcast- BCR, BCST in LSW & TW set to "1".

COMMAND+ DATA WORD
No status response.
Bits set:
INV to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.10 RESERVED MODE CODES (01001- 01111; T/ R= 1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

BROADCAST COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR set to "1" in LSW.
INV and BCST set to "1" in TW.

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.11 TRANSMIT VECTOR WORD (10000; T/ R= 1)

VALID COMMAND
Responds with status followed by vector word except if broadcast.
Bits set: *MDCD to "0" in CDR.

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+ DATA WORD
UNIMPLEMENTED COMMAND

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.12 SYNCHRONIZE WITH DATA WORD (10001; T/ R= 0)

VALID COMMAND
Responds with status except if broadcast. Data word stored into RAM. Data word will update lower 16 bits of real time clock depending on the configuration of the RTC CONTROL REGISTER.

Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in LSW & TW to "1".

COMMAND NO DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.

COMMAND + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV set to "1" in TW.

BROADCAST + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR to "1" in LSW.
INV and BCST to "1" in TW.

T/ R= 1
UNIMPLEMENTED COMMAND

T/ R= 1 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.13 TRANSMIT LAST COMMAND (10010; T/ R= 1)

VALID COMMAND
Responds with status followed by LAST VALID COMMAND word except if broadcast.
Status and command registers NOT updated.
Bits set: *MDCD to "0" in CDR.

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR.
INV to "1" in TW.
ME to "1" in LSW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+ DATA WORD
UNIMPLEMENTED COMMAND

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.14 TRANSMIT BIT WORD (10011; T/ R= 1)

VALID COMMAND
Responds with status followed by BIT word.
Bits set: *MDCD to "0" in CDR.

COMMAND+ DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" inLSW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+ DATA WORD
UNIMPLEMENTED COMMAND

T/ R= 0
UNIMPLEMENTED COMMAND

T/ R= 0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.15 SELECTED TRANSMITTER SHUTDOWN (10100; T/ R= 0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & LSW.

COMMAND + EXTRA DATA WORD
No response
Bits set:

INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:

BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

5.2.16 OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101; T/ R= 0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & LSW.

COMMAND + EXTRA DATA WORD
No response
Bits set:
INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:

BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

5.2.17 RESERVED MODE CODES (10110- 11111; T/ R= 1)

VALID COMMAND
Responds with status and data word.
Bits set: *MDCD to "0" in CDR.

COMMAND + DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME to "1" in LSW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+ DATA WORD
UNIMPLEMENTED COMMAND

5.2.18 RESERVED MODE CODES (10110- 11111; T/ R= 0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & LSW.

COMMAND + EXTRA DATA WORD
No response
Bits set:
INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:
BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

6.0.0 INITIALIZATION

There are several types of initialization that can set up the NHi- RT parameters.

6.1.0 INTERNAL INITIALIZATION

There are two methods of initializing the NHi RT. Each will produce the same results. They are: Hardware(MRST) and Software (writing to address 15, data not used). After these resets have been performed, all internal state machines are reset.

The hardwire terminal address is loaded when a hardware or software reset occurs. The hardwire address is connected to I/ O DAT(5: 0) pins. I/ O DAT(4: 0) are used for the address and I/ O DAT5 is used to set odd parity in the address. The address is wired using external 4.7K pull-down resistors to set a low and internal 64K pull- up resistors to set a high.

The following table summarizes the condition of internal registers after a reset has been performed.
Note: All register bit set to 0 at reset except as noted.

REGISTER RESET TABLE

ADDR	REGISTER	BITS=1	COMMENTS
0	CONTROL	HWD	
1	POINTER TABLE ADDRESS		LOADED WITH 4096 DEC WORD
2	BASIC STATUS*		HARDWIRE ADDRESS LOADED
3	INTERRUPT MASK	ALL	ALL INTERRUPTS ARE MASKED
4	INTERRUPT VECTOR		
3	INTERRUPT REQUEST		
4	AUXILLIARY VECTOR		UNDEFINED
5,6	RTC; HIGH.LOW		NOT AFFECTED BY RESET
7	RTC CONTROL		
8	FIFO		RESET ONLY BY MRST
11	LAST COMMAND		UNDEFINED
12	LAST STATUS*		HARDWARE ADDRESS LOADED
18	ENCODER STATUS		
19	CONDITION	9,11-13	

* See RESET BUSY TABLE

RESET FUNCTION TABLE

RESET TYPE	REGISTERS	STATE MACHINES
MODE CODE	RESET	RESET
MRST(HARDWARE)	RESET	RESET
SOFTWARE	NO CHANGE	RESET

RESET BUSY TABLE

This table defines the state of the Busy bit in the Basic Status and Last Status registers.

RESET TYPE	RTCC REG BIT 6	CONFIG REG1 BIT1	BUSY BIT
MRST(HARDWARE)	X	X	SET TO “1”
SOFTWARE	0	0	SET TO “1”
SOFTWARE	X	1	NO CHANGE
SOFTWARE	1	X	NOCHANGE
MODE CODE	X	X	SET TO “1”
MODE CODE	X	X	SET TO “1”
MODE CODE	X	X	SET TO “1”

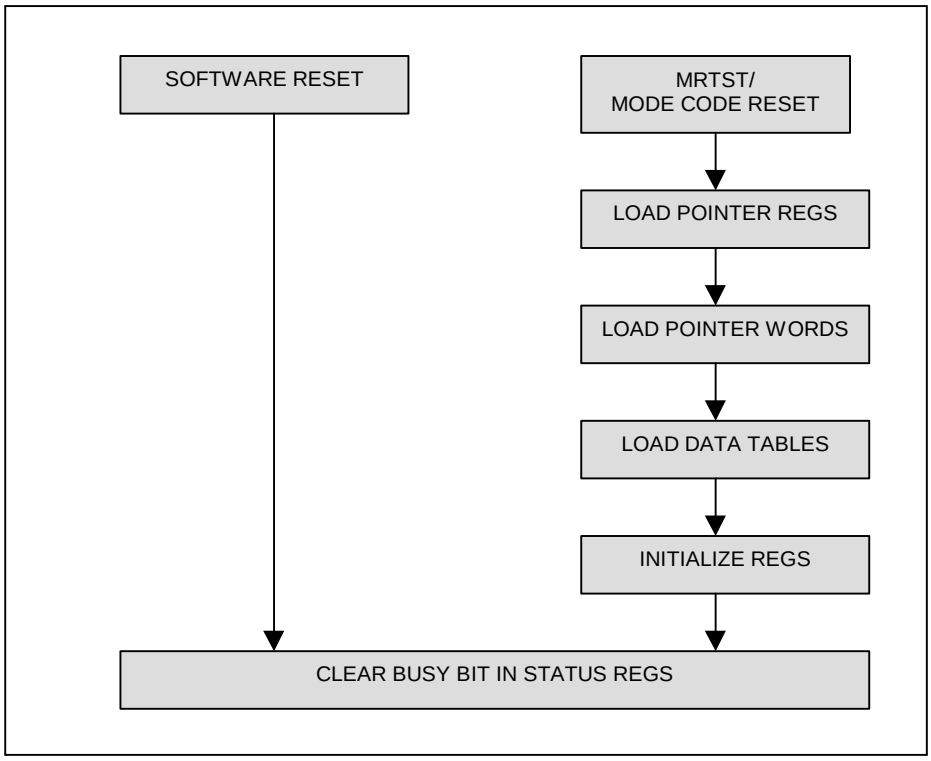
6.2.0 HOST INITIALIZATION OF NHi-RT

The host will usually want to initialize the RT at power up or at any other time it feels the procedure is necessary. At power up the host must initialize the registers discussed in the preceding section if the default settings of the internal initialization are not suitable. In addition the host must initialize the RAM, the pointer tables, and the data table tag words for each command type and subaddress.

The host initialization of the registers is also required only after a hardware reset. Since the RAM is not affected by any resets, it does not have to be re- initialized unless data has been lost or corrupted, therefore the pointer tables will remain intact.

The following flow diagram is a suggested method of host initialization of the NHi- RT.as a function of the type of reset which has occurred.

TYPICAL NHi-RT INITIALIZATION PROCEDURE BY CPU



Note: If bit 6 in the RTCC or bit 1 in Configuration reg 1 is set to "1", the Software reset wil NOT set the busy bit in the Status regs.

7.0.0 INTERRUPT HANDLING

When an interrupt request is received by the NHi-RT, the *IRQ line goes low and header information about the message that caused the interrupt is pushed on an internal FIFO. If another interrupt request is received before the CPU performs an acknowledge, it's header information is also pushed onto the FIFO. I n this manner, there is no danger of losing interrupt vectors or header information due to receiving multiple interrupt requests before an acknowledge by the CPU takes place. The FIFO can hold header information for six interrupt messages. If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the header information for the message which caused the overflow is pushed onto the FIFO. As a result, the header information from the two oldest messages is lost.

If the FIFO is in the revolving mode, the FIFO will store seven interrupts. When another interrupt is issued and the FIFO contains seven previous headers, the new header is pushed onto the FIFO and the oldest header is lost.

7.1.0 HARDWARE INTERRUPT ACKNOWLEDGE

To acknowledge an interrupt in hardware, the *INTACK line is taken low, the *HCS line held high and the *INTPI line is held low. This pops the interrupt header information off the FIFO and into the IVR and AVR. The *IRQ line will go high if the FIFO is empty, but remain low if there are

additional interrupt headers on the FIFO. The IVR will be outputted on the upper and lower byte of the CPU data bus. If the *INTPI line is high, then *INTACK is ignored.

The IVR and AVR can be read from address 4 after performing the hardware interrupt.

If there are more interrupt headers on the FIFO, indicated by the *IRQ remaining low after the interrupt acknowledge, the procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line returning high after an interrupt acknowledge and bit 8 in the AVR will be a "1".

7.2.0 SOFTWARE INTERRUPT ACKNOWLEDGE

If the host CPU does not support a hardware interrupt acknowledge, a software acknowledge can be performed by reading address 8. This read pops the interrupt header information off the FIFO and into the IVR and AVR and places their contents on the CPU data bus. The *IRQ line will go high if the FIFO is empty and remain low if there are additional interrupt headers on the FIFO.

If there are more interrupt headers on the FIFO, indicated by the *IRQ remaining low after the interrupt acknowledge, the procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line returning high after an interrupt acknowledge and the MSB in the AVR will be a "1".

8.0.0 PC BOARD CONSIDERATIONS AND GUIDE LINES

There are a few guide lines which should be observed when mounting the RT and its coupling transformer on a PC board. The following considerations will prevent layout problems on the board:

The width of the two land traces for each Bus from the RT to the transformer must be as wide as possible(0.1in min width).

The length of the two land traces for each Bus from the RT to the transformer must be as short as possible(0.5in max length).

The two land traces for each Bus from the RT to the transformer must be balanced in length and width.

There should be no ground plane or power plane under the transformer or the land traces connecting the transformer to the RT.

The center tap of the transformer primary must be connected to ground with a heavy short land trace.

The center tap of the transformer secondary should be left floating.

All the power and ground pins on the RT must be connected.

A 0.1uf capacitor should be connected from each power pin on the RT to ground.

9.0.0 PIN FUNCTIONAL DESCRIPTION

The NHi-RT I/ O pins are divided into 5 families:

General purpose signals
Host interface signals
I/ O bus interface signals
Mil-Bus interface signals
Power

9.1.0 GENERAL PURPOSE SIGNALS

MRST_ L Master Reset (active low, input).
Initializes all registers and state machines. RT reads hardwire terminal address. Reset pulse width is 300ns min. The reset recovery time is 12us max after the rising edge of the reset pulse.

CLK_ H Terminal Clock from 10 Mhz oscillator (input).

9.2.0 HOST INTERFACE SIGNALS

H_ DAT (15: 0) Host Data bus (bi- directional).

H_ ADR (14: 1) Host Address bus (input).

HCS_ L Chip Select (active low, input).
Selects the NHi-RT. The falling edge of HCS_ L is used to latch the host address and indicates the start of a host memory cycle. The rising edge terminates the current cycle. During a host read- modify- write cycle. This signal must remain active from the beginning to the end of an access cycle.
NOTE: The host should not hold *HCS active for more than 5 microseconds, otherwise timing errors on the 1553 bus may occur.

HWRL_ L Host Write Lower Byte (active low, input).

HWRH_ L Host Write Upper Byte (active low, input).

HRD_ L Host Read (active low, input).

DACK_ L Host Data Transfer Acknowledge (active low, open drain output, 5K internal pull up).
Indicates to the host that a data transfer has been completed. When the host reads data, it takes HCS_L low and the HRD_ L low. The RT will indicate that stable data is on the bus by outputting a low on DTACK_ L. When the Host writes data, it takes HCS_ L low and HWRL_ L and/ or HWRH_ L low. The RT then indicates that it has completed the write cycle by outputting a low on DTACK_ L.

IRQ_ L Host Interrupt Request (active low, open drain output, 5K internal pullup).
The IRQ_L will remain low until the Fifo is empty

INTACK_ L Host Interrupt Acknowledge (active low, input).
When HRD_ L= 0, INTACK_ L= 0, and HCS_ L= 1, an interrupt vector is popped from the FIFO, the IVR and AVR registers are updated, and the IVR is outputted onto both the lower and upper bytes of the host data bus, provided the INTPI_ L is low.

INTPI_ L Interrupt Priority Input (active low, input).
This signal is used to daisy chain interrupt requests on the host bus. This signal must be active for the RT to output an interrupt vector.

INTPO_L_DSC Interrupt Priority Output, Disconnect Signal (output).
This pin has 2 possible functions, depending on the M1760 bit in the RTC CONTROL register.
If M1760= 0, then the signal is used to daisy chain interrupt requests on the host bus. When the RT requests an interrupt, this signal is output high; otherwise, this signal is equal to INTPI_ L.
If M1760= 1, then the pin is set to "1" when the store is disconnected (see EXTERNAL TERMINAL ADDRESS BUFFER for details).

9.3.0 DISCRETE I/O BUS INTERFACE SIGNALS

I/O_ RD_ L I/O Read (active low, output).
I/O_ WR_ L I/O Write (active low, output).

I/O_ ADR (2: 1) I/O Address (outputs).
These three signals can be used to select 4 byte- wide input devices and 4 byte- wide output devices which reside on the I/ O Data bus.

I/O_ DAT (7: 0) I/O DATA bus (bi- directional).
This bus is used for messages that are mapped to I/O, discreet pulse message identifiers and setting the Hardwire RT address.

CMDS Command Strobe (active high, output; 100ns).
This strobe is used for two special I/ O operations. When the strobe is active during a write cycle (i. e., CMDS= 1, I/ O WR_ L= 0), valid commands or pulses appear on the I/ O bus (see the CMDO bit in CONTROL register for details). When the strobe is active during a read cycle (i. e., CMDS= 1, I/ O RD_ L= 0), the EXTERNAL TERMINAL ADDRESS buffer is accessed.

PLSCMD Pulse Command(active high, output; 100ns).
Depends on the value of the CMDO bit in the CONTROL register. If CMDO= 0, then a pulse is issued whenever a bus message accesses a data table with PULSE (3: 0)= 14 (decimal) in its tag word. If CMDO= 1, then a pulse is issued whenever a valid broadcast command is received.
Note: The NTAG bit in the CONTROL register must be 0 to get a pulse output.

MDCDRST Mode Command Reset Pulse (active high, 400 nS pulse, output).
Pulsed high whenever the mode command "Reset" is received by the RT.

SSF_ TF Subsystem Flag, Terminal Flag (active high, input).
Sets either the Subsystem Flag bit or the Terminal Flag bit in the STATUS register. The SSF_ TF bit in the CONTROL register determines which status bit will be set by this input (see CONTROL register for details).

9.4 MIL-BUS INTERFACE SIGNALS

BUS_ A, BUS_ A_ L BUS A signals (bi- directional).
Connected to a bus coupling transformer.

BUS_ B, BUS_ B_ L BUS B signals (bi- directional).
Connected to a bus coupling transformer.

TXINH_ A BUS A INHIBIT (input).
A logic high Inhibits the bus A transmitter.

TXINH_ B BUS B INHIBIT (input).
A logic high Inhibits the bus B transmitter.

10.0.0 ELECTRICAL CHARACTERISTICS

10.1.0 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
SUPPLY VOLTAGE	Vcc	-0.3	+7.0	Volts	
INPUT VOLTAGE	Vin	-0.3	+6.7	Volts	1
INPUT CURRENT	Iin	-10		Microamps	2
INPUT ZAPPING	Vzap	2000		Volts	3
LATCH-UP TRIGGER	ILatch		200	Milliamps	4
THERMAL RESISTANCE	Tjc		4	DegC/W	
STORAGE TEMP.	Tstorage	-65	+150	Deg C	
LEAD TEMP.	TL		+300	Deg C	

Note 1: VCC referenced to ground
Note 2: Does not include current through internal 64K ohm pull- up/ down resistors.
Note 3: As defined for ESDS in Method 3015 0f MIL- STD- 883.
Note 4: The latch- up triggering current is the maximum current that will not cause latch- up on an I/ O BUFFER.

10.2.0 OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	Vcc	4.7	5.5	Volts
STANDBY CURRENT	Iccstby		90	Milliamps
100% XMT CURRENT	Icc100		675	Milliamps
BUS LEVEL	Vpp	7.1		Volts
STUB LEVEL	Vpp	20	27	Volts
CASE TEMPERATURE	TC	-55	+125	Deg C

10.3.0 I/O TYPES & DESCRIPTIONS

I/O TYPES	DESCRIPTION
1	BI-DIRECTIONAL 3 STATE BUFFER 64K PULL UP
2	BI-DIRECTIONAL STATE BUFFER 64K PULL UP
3	TOTEM POLE OUTPUT BUFFER
4	TOTEM POLE OUTPUT BUFFER
5	OPEN DRAIN OUTPUT BUFFER
6	3 STATE OUTPUT BUFFER
7	INPUT BUFFER 64K PULL UP
8	INPUT BUFFER 64K PULL DOWN
9	INPUT BUFFER

I/O TYPE	SIGNAL NAME	I/O TYPE	SIGNAL NAME
1	H_DAT(15:0)	7	HWRH_L
2	I/O_DAT(7:0)	7	HWRL_L
3	DSC_INTPO_L	7	MRST_L
3	CMDS	7	INTPI_L
4	MDCDRST	7	INTACK_L
4	PLSCMD	7	SSF_TF
4	I/O_RD_L	7	H_ADR(14:1)
4	I/O_WR_L	7	HCS_L
5	DTACK_L	8	CLK10
5	IRQ_L	9	TXINH_A
6	I/O_ADR(2:1)	9	TXINH_B
7	HRD_L		

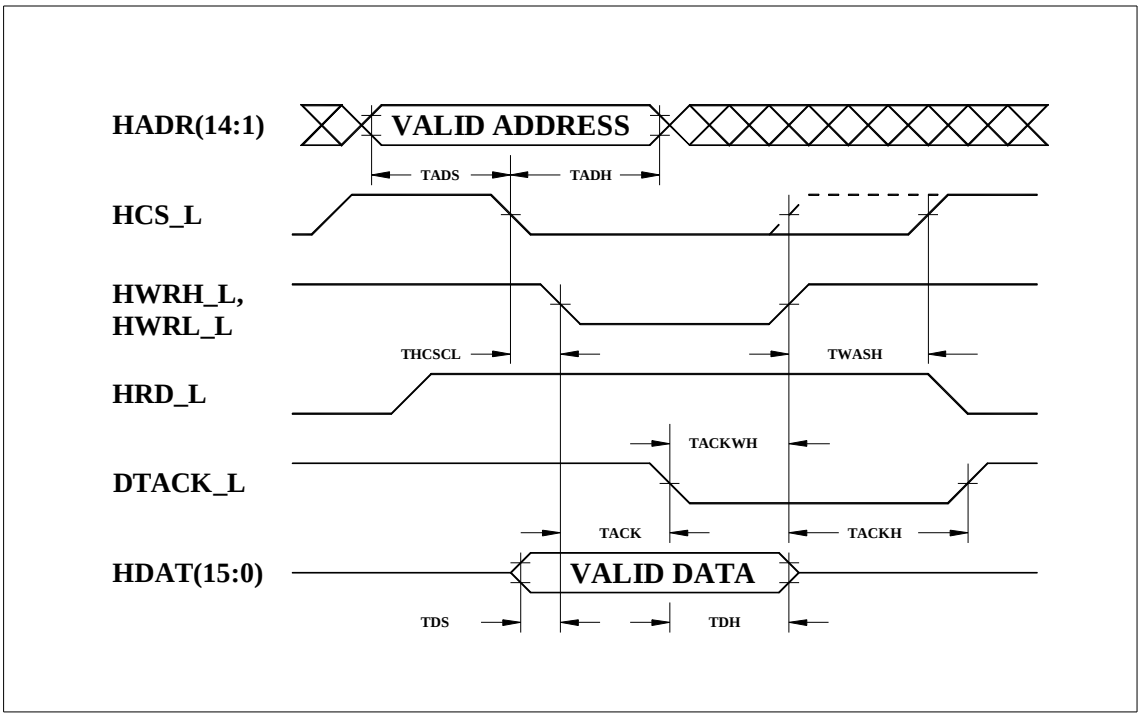
10.4.0 I/O ELECTRICAL CHARACTERISTICS

PARAMETER	I/O TYPE	CONDITION	MIN	MAX	UNITS
INPUT LOW VOLT	1,2,7,8,9			0.8	VOLTS
INPUT HIGH VOLT	1,2,7,8,9		2.0		VOLTS
OUTPUT LOW VOLT	1	IOL < 8.0 ma		0.4	VOLTS
	2	IOL < 4.0 ma		0.4	VOLTS
	3	IOL < 4.0 ma		0.4	VOLTS
	4	IOL < 6.0 ma		0.4	VOLTS
	5	IOL < 16.0 ma		0.4	VOLTS
	6	IOL < 8.0 ma		0.4	VOLTS
OUTPUT HIGH VOLT	1	IOH > -8.0 ma	2.4		VOLTS
	2	IOH > -4.0 ma	2.4		VOLTS
	3	IOH > -4.0 ma	2.4		VOLTS
	4	IOH > -6.0 ma	2.4		VOLTS
	6	IOH > - 8.0 ma	2.4		VOLTS
INPUT CAPACITANCE				10	PF

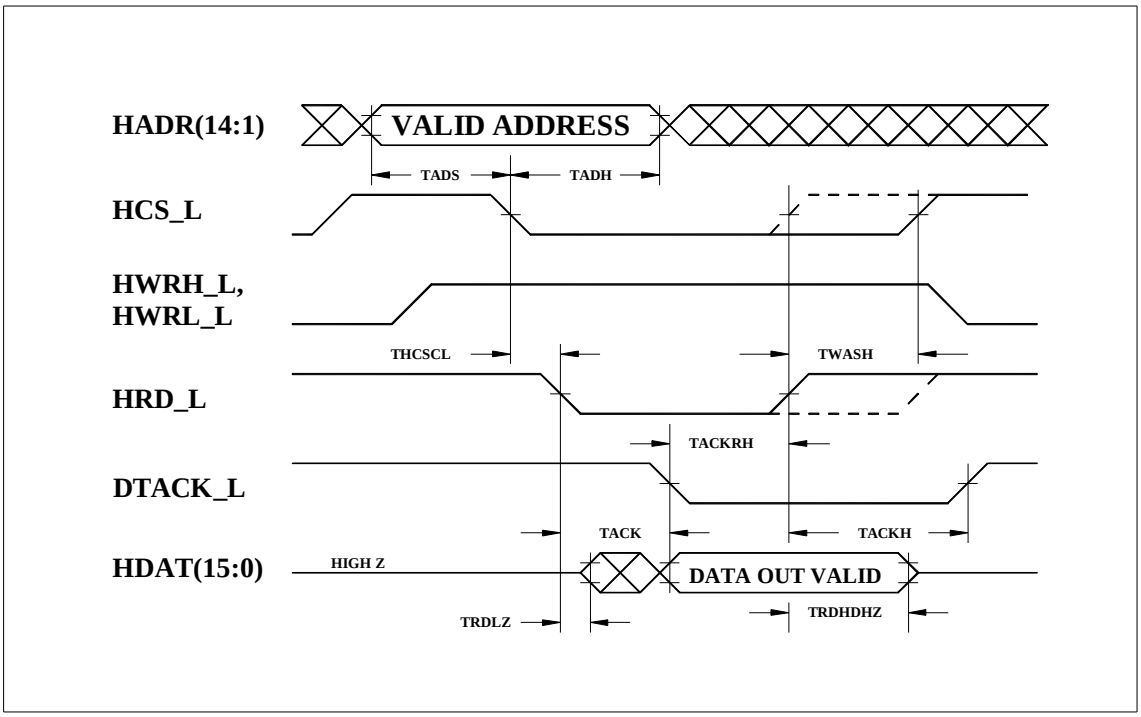
11.0.0 TIMING DIAGRAMS

The following diagrams and notes describe the timing of the address, data, and control lines.

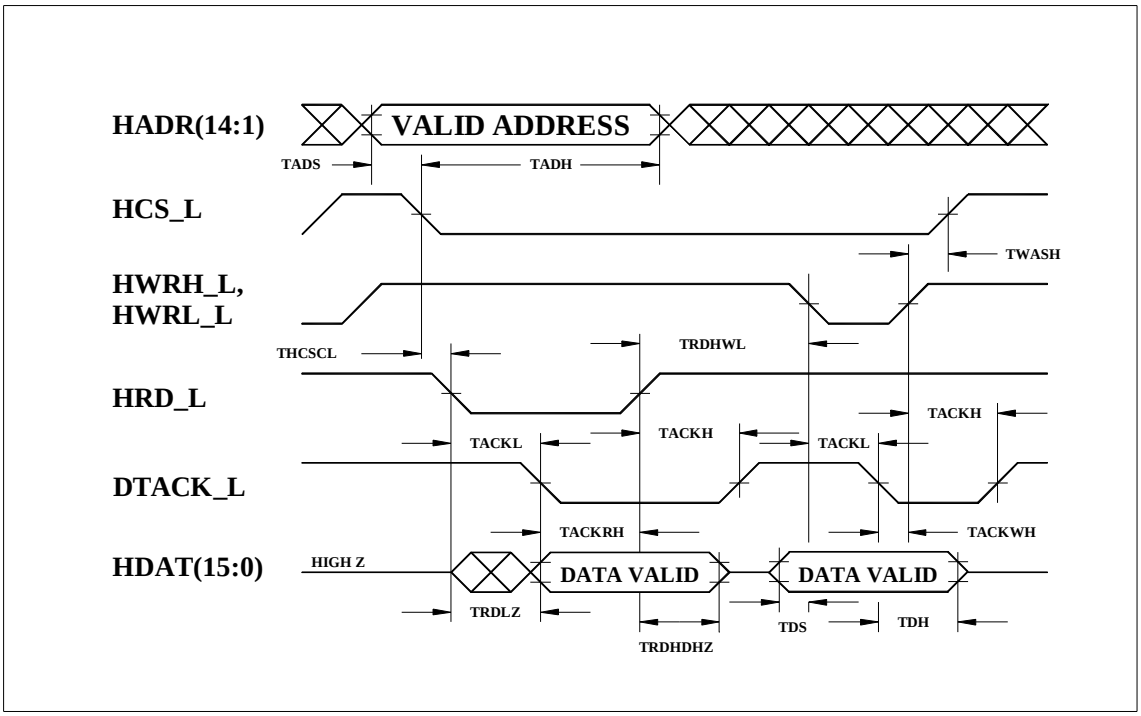
11.0.1 HOST WRITE CYCLE



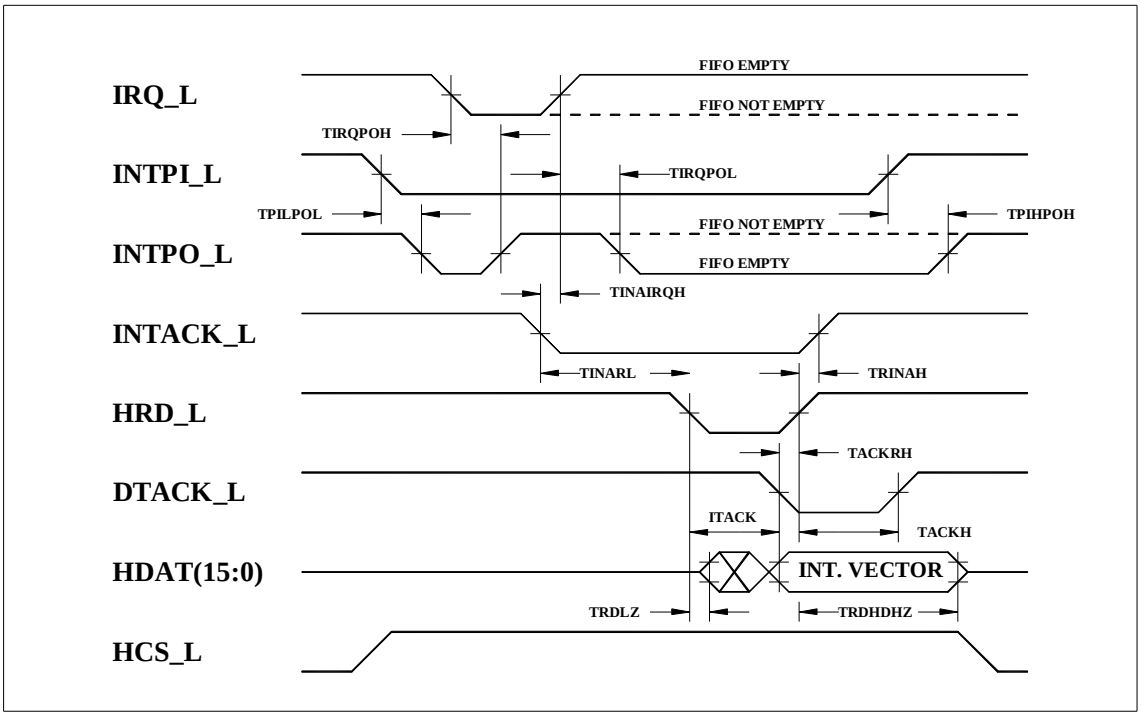
11.0.2 HOST READ CYCLE



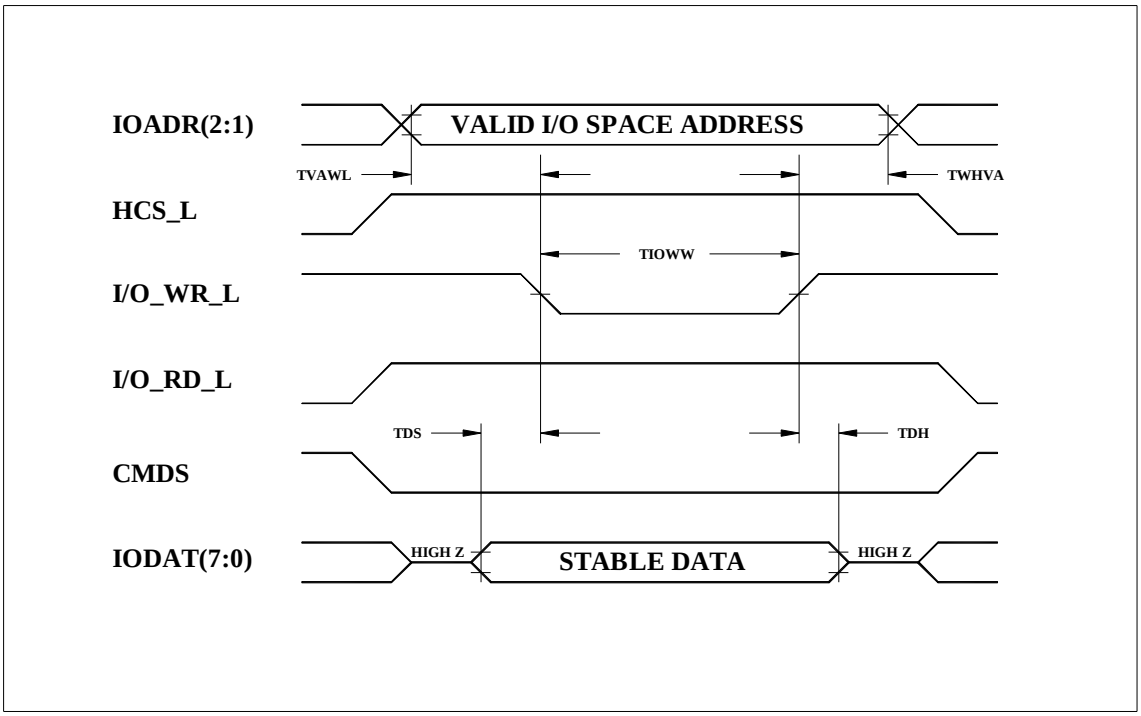
11.0.3 HOST READ- MODIFY- WRITE CYCLE



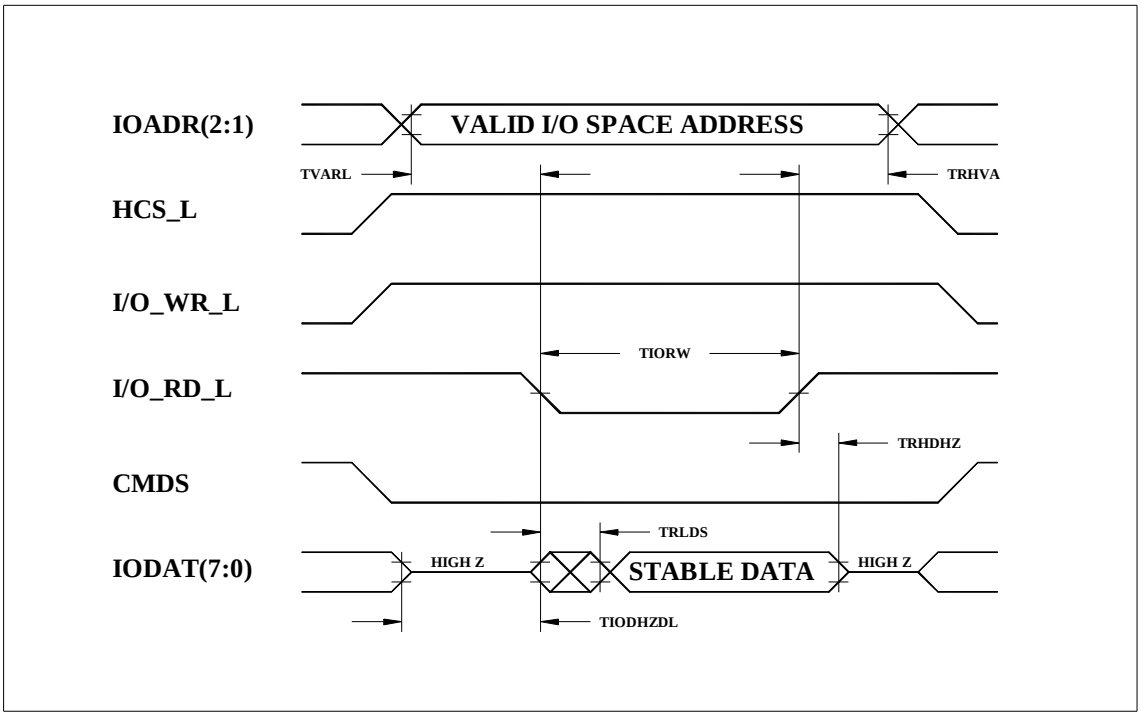
11.0.4 RT HARDWARE INTERRUPT ACKNOWLEDGE CYCLE



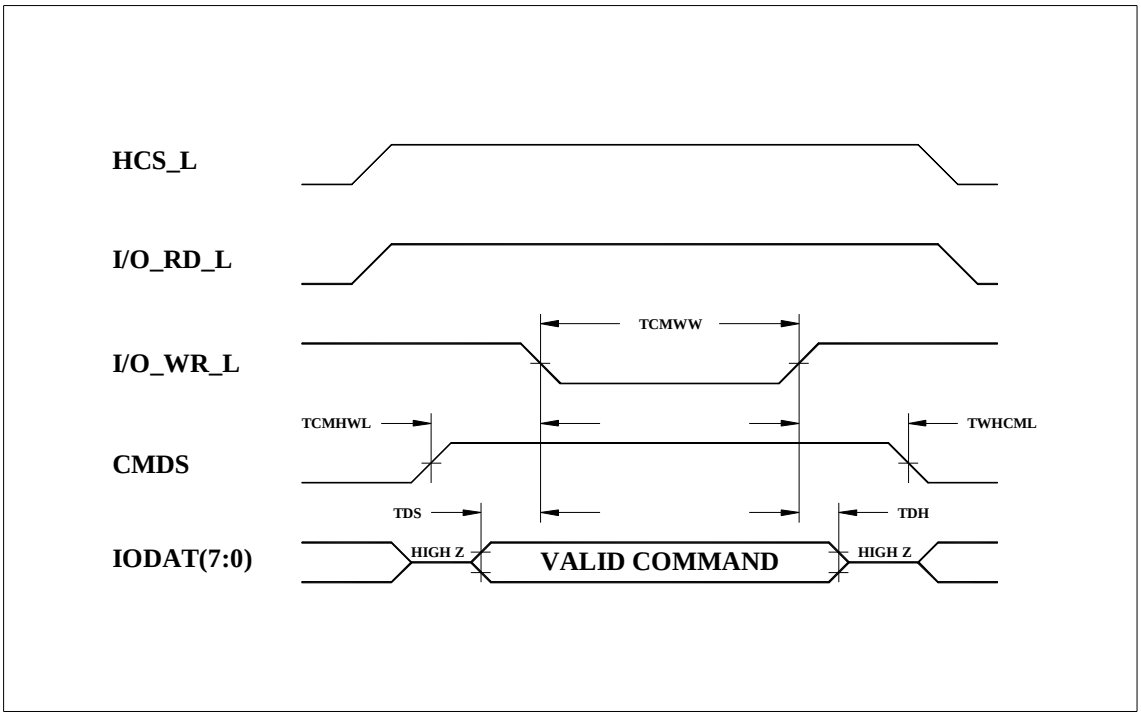
11.0.5 I/O WRITE CYCLE



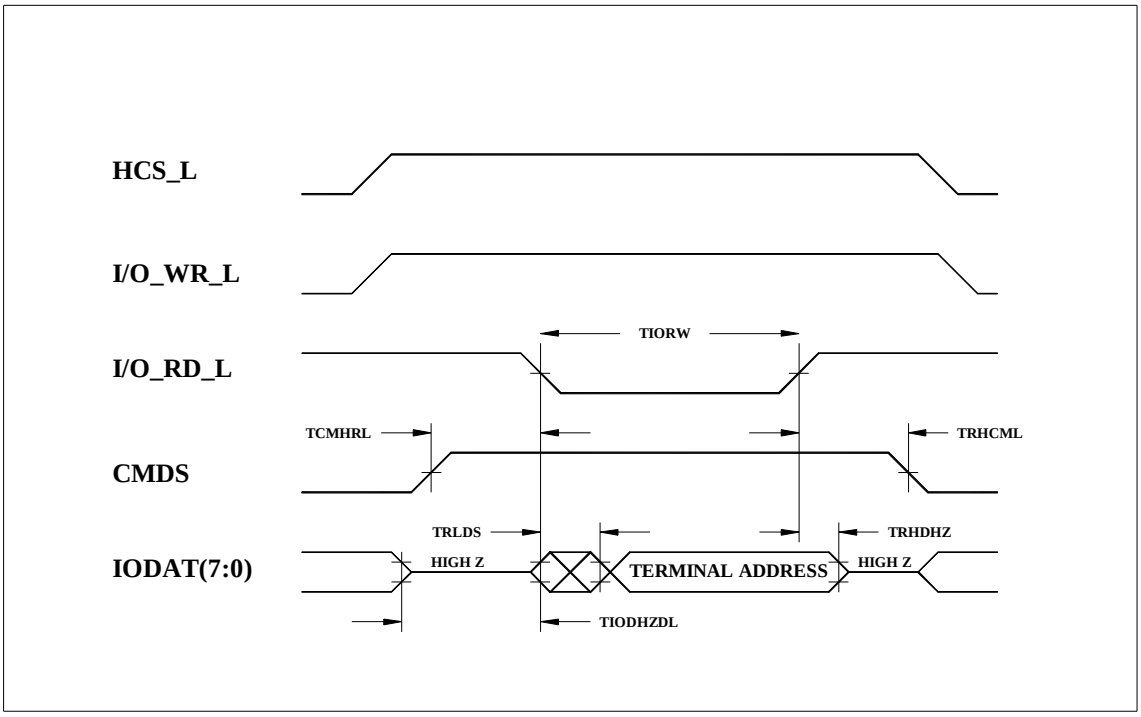
11.0.6 I/O READ CYCLE



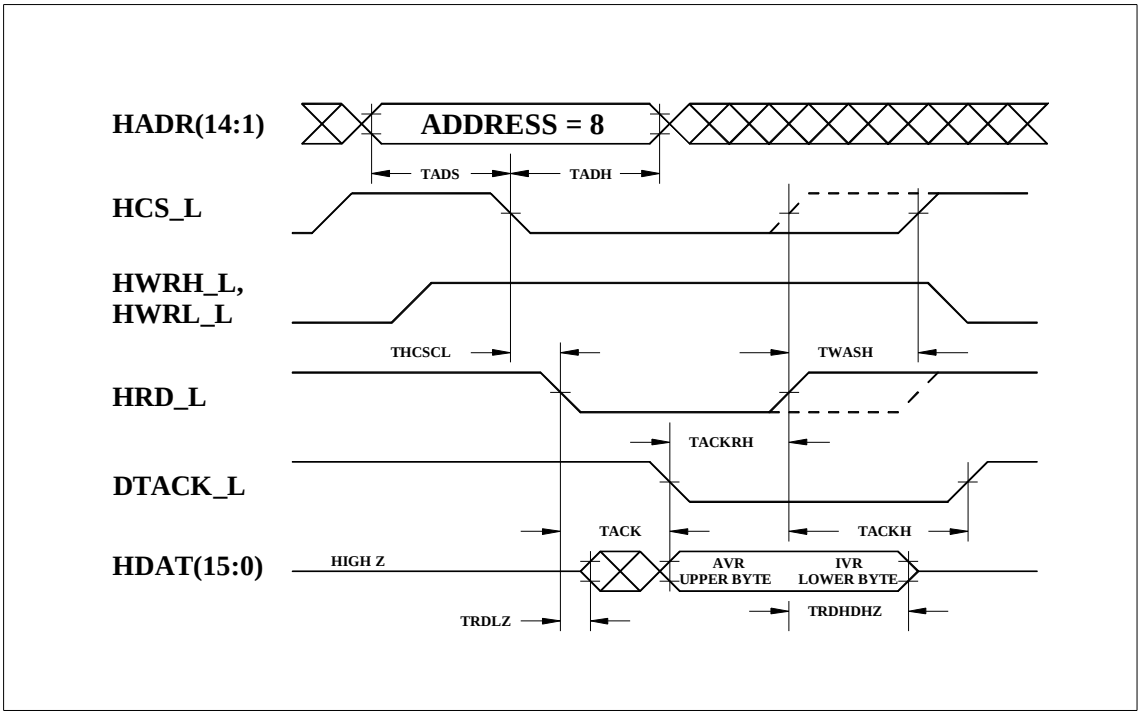
11.0.7 COMMAND WRITE CYCLE



11.0.8 TERMINAL ADDRESS READ CYCLE



11.0.9 SOFTWARE INTERRUPT ACKNOWLEDGE CYCLE



11.0.10 TIMING NOTES

The address is latched by the NH- RT on the high- to- low transition of the *HCS line. TADS, TADH, and TASLC are referenced to the high- to- low transition of *HCS.

TACK is a function of the contending access performed by the NHi-RT (see host access table).

The low- to- high transition of HRD_L or I/ O RD_L or HCS_L terminates the read cycle.

The low- to- high transition of HWRH_L or HWRL_L or I/ O WR_L or HCS_L terminates the write cycle.

The DTACK_l line is tri- stated after delay TACKH. Its rise time is a function of the internal 5K ohm pull- up resistor and the external load.

While INTACK_L is low, INTPO_L will be affected by changes in IRQ_L.

ITACK starts after the falling edge of HRD_L and INTACK_L..

11.1.0 TIMING PARAMETER TABLES

11.1.1 HOST READ, WRITE, READ- MODIFY- WRITE TABLE and SOFTWARE INTERRUPT ACKNOWLEDGE

SYMBOL	PARAMETER	MIN(ns)	Max(ns)
TADS	ADDRESS SETUP TIME	0	-
TADH	ADDRESS HOLD TIME	200	-
THCSCL	HCS_L LOW TO COMMAND LOW	0	-
TACKWH	DATA ACKNOWLEDGE LOW TO WRITE HIGH	0	-
TWASH	HWRH,L_L HIGH TO HCS_L HIGH	0	-
TACKH	END OF CYCLE TO DATA ACKNOWLEDGE HIGH	0	30
TACKL(1)	NO CONTENTION	0	650
TACKL(2)	WITH CONTENTION	0	1500
TACKL(3)	WORST CASE ; ONCE AT START OF MESSAGE	0	3200
TDS	DATA SETUP TIME	0	75
TDH	DATA HOLD TIME	0	-
TACHRH	DATA ACKNOWLEDGE LOW TO READ HIGH	0	-
TRDLZ	HRD_L LOW TO DATA LOW Z	0	20
TRDHDHZ	HRD_L HIGH TO DATA HIGH Z	0	30
TRDHWL	HRD_L HIGH TO WRITE LOW	30	-

11.1.2 I/O READ and TERMINAL ADDRESS READ TABLE

SYMBOL	PARAMETER	MIN(ns)	Max(ns)
TVARL	VALID ADDRESS TO I/O_RD_L LOW	50	-
TRHVA	ADDRESS VALID AFTER I/O_RD_L HIGH	50	-
TIORW	I/O_RD_L PULSE WIDTH	190	210
TRHDHZ	I/O_RD_L HIGH TO DATA HIGH Z	0	200
TRHCML	I/O_RD_L HIGH TO CMDS LOW	100	-
TCMHRL	CMDS HIGH TO I/O_RD_L LOW	100	-
TIODHZDL	I/O DATA BUS HIGH Z TO DATA ON BUS	100	-
TRLDS	I/O_RD_L LOW TO DATA STABLE	-	80

11.1.3 I/O WRITE and COMMAND WRITE TABLE

SYMBOL	PARAMETER	MIN(ns)	Max(ns)
TVAWL	VALID ADDRESS TO I/O_WR_L LOW	50	-
TWHVA	ADDRESS VALID AFTER I/O_WR_L HIGH	50	-
TIOWW	I/O_WR_L PULSE WIDTH	90	110
TDS	DATA SETUP TIME	25	50
TDH	DATA HOLD TIME	40	80
TCMWW	COMMAND WRITE PULSE WIDTH	290	310
TCMHWL	CMDS HIGH TO I/O_WR_L LOW	40	-
TWHCML	I/O_WR_L HIGH TO CMDS LOW	100	-

11.1.4 RT HARDWARE INTERRUPT ACKNOWLEDGE CYCLE TABLE

SYMBOL	PARAMETER	MIN(ns)	Max(ns)
TIRQPOH	IRQ_L LOW TO INTPO_L HIGH	-	20
TPILPOL	INTPI_L LOW TO INTPO_L LOW	-	40
TPIHPOH	INTPI_L HIGH TO INTPO_L HIGH	-	40
TINAIRQH	INTACK_L LOW TO IRQ_L HIGH	0	200
TINAIRQL	INTACK_L HIGH TO NEXT IRQ_L LOW	0	200
TRINAH	HRD_L HUGH TO INTACK_L HIGH	0	-
ITACK	HRD_L LOW TO DTACK_L LOW	300	400
TACKRH	DTACK_L LOW TO HRD_L HIGH	0	-
TRDLZ	HRD_L LOW TO DATA IN LOW Z	0	20
TRDHDHZ	HRD_L HIGH TO DATA IN HIGH Z	0	30
TACKH	END OF CYCLE TO DTACK_L HIGH	0	30
TIRQPOL	IRQ_L HIGH TO INTPO_L LOW	10	20
TINARL	INTACK_L LOW TO HRD_L LOW	0	30

12.0.0 PIN FUNCTION TABLE

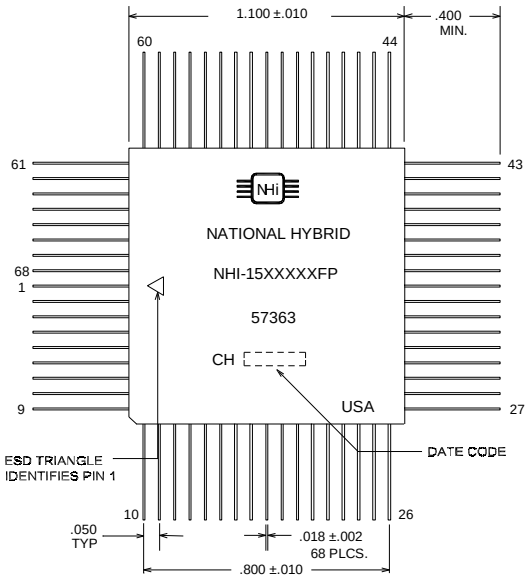
12.0.1 UNIVERSAL PIN FUNCTIONS QUAD FLAT PACK AND PIN GRID ARRAY PINS

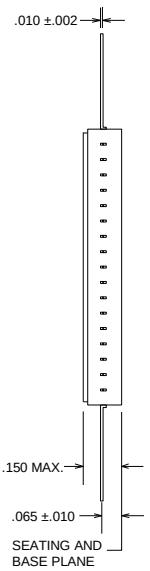
QFP	PGA	FUNCTION	QFP	PGA	FUNCTION
1	L10	I/O_DAT1	35	D2	H_ADR4
2	H10	I/O_DAT2	36	C1	H_ADR5
3	J10	I/O_DAT3	37	B1	H_ADR6
4	K10	I/O_DAT4	38	A2	H_ADR7
5	K9	I/O_DAT 5	39	K5	+5V
6	L9	I/O_DAT6	40	L5	+5V
7	L8	I/O_DAT7	41	J1	GND
8	G11	HCS_L	42	K1	GND
9	H11	SSF_TF	43	B2	GND
10	G10	MRST_L	44	A3	H_ADR8
11	J11	CLK10	45	B4	H_ADR9
12	K8	I/O_ADR1	46	A4	H_ADR10
13	L7	I/O_ADR2	47	B5	H_ADR11
14	K7	INTPO_L_DSC	48	A5	H_ADR12
15	L6	INTPI_L	49	B6	H_DAT0
16	K6	INTACK_L	50	A6	H_DAT1
17	G2	TXINH_A	51	A7	H_DAT2
18	B3	BUS_A	52	B7	H_DAT3
19	C2	BUS_A_L	53	A8	H_DAT4
20	C3	H_ADR13	54	A9	H_DAT5
21	L3	CMDS	55	A10	H_DAT6
22	K4	TXINH_B	56	B8	H_DAT7
23	J2	BUS_B	57	B9	H_DAT8
24	H1	BUS_B_L	58	B10	H_DAT9
25	K3	H_ADR14	59	B11	H_DAT10
26	L4	I/O_RD_L	60	C11	H_DAT11
27	H2	I/O_WR_L	61	C10	H_ADR1
28	K2	MDCDRST	62	D11	HRD_L
29	F2	PLSCMD/B_JAM	63	E11	HWRL_L
30	F1	IRQ_L	64	F11	HWRH_L
31	E1	DTACK_L	65	D10	H_DAT13
32	G1	H_DAT12	66	E10	H_DAT14
33	E2	H_ADR2	67	F10	H_DAT15
34	D1	H_ADR3	68	K11	I/O_DAT0
-	-	-	-	L2	N/C

Note: See individual part listing for special pin functions.

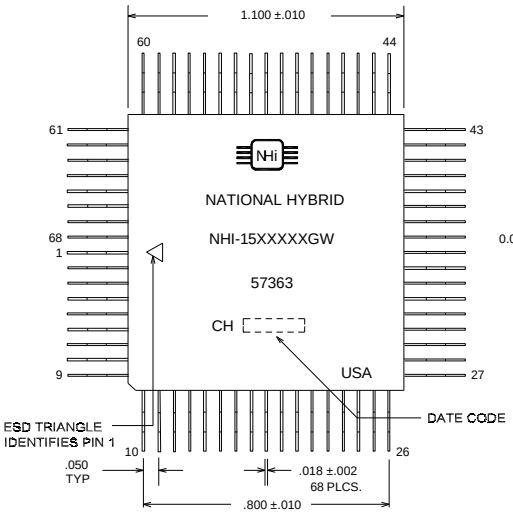
12.1.0 GENERIC PACKAGE OUTLINE DRAWINGS

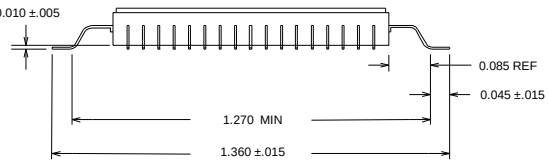
12.1.1 QUAD FLAT PACK UNFORMED LEADS



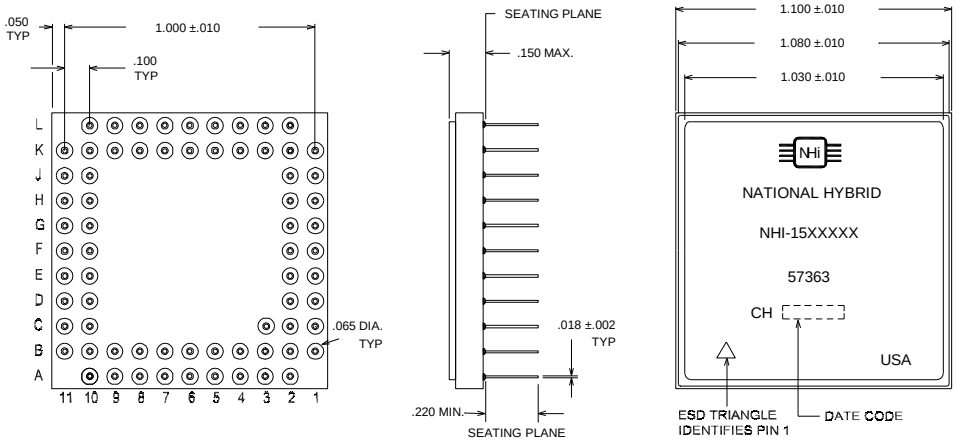


12.1.2 QUAD FLAT PACK GULL WING LEADS

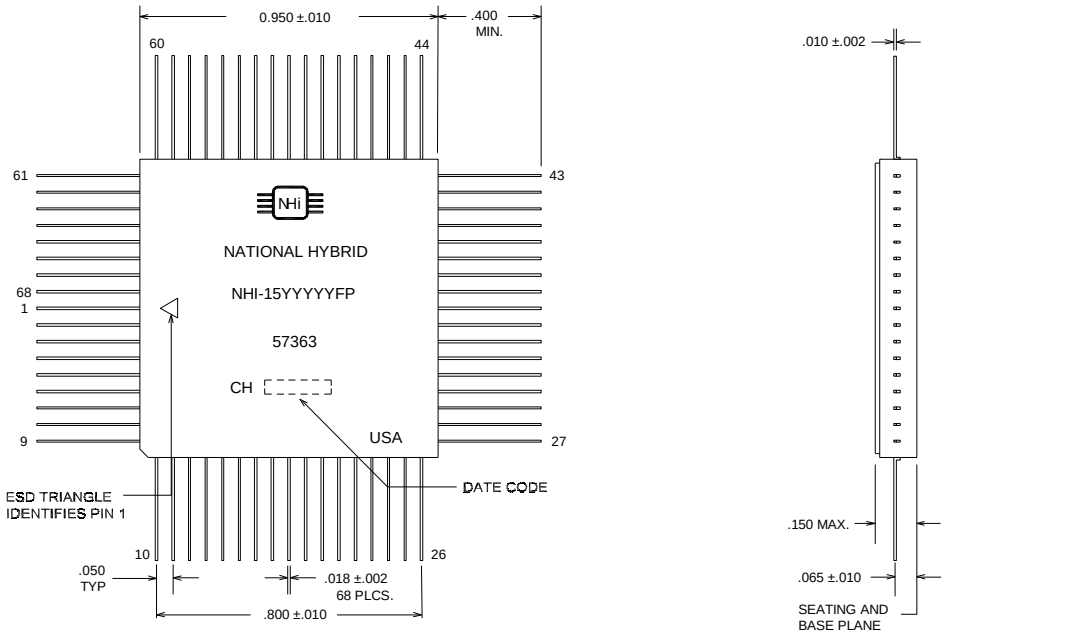




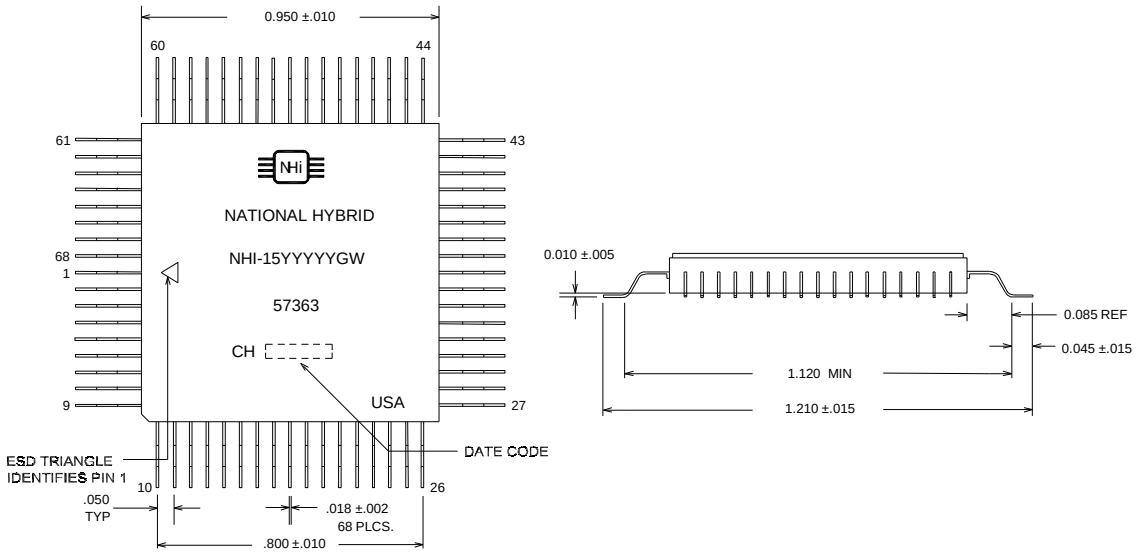
12.1.3 PIN GRID ARRAY



12.1.4 MICRO QUAD FLAT PACK UNFORMED LEADS



12.1.5 MICRO QUAD FLAT PACK GULL WING LEADS

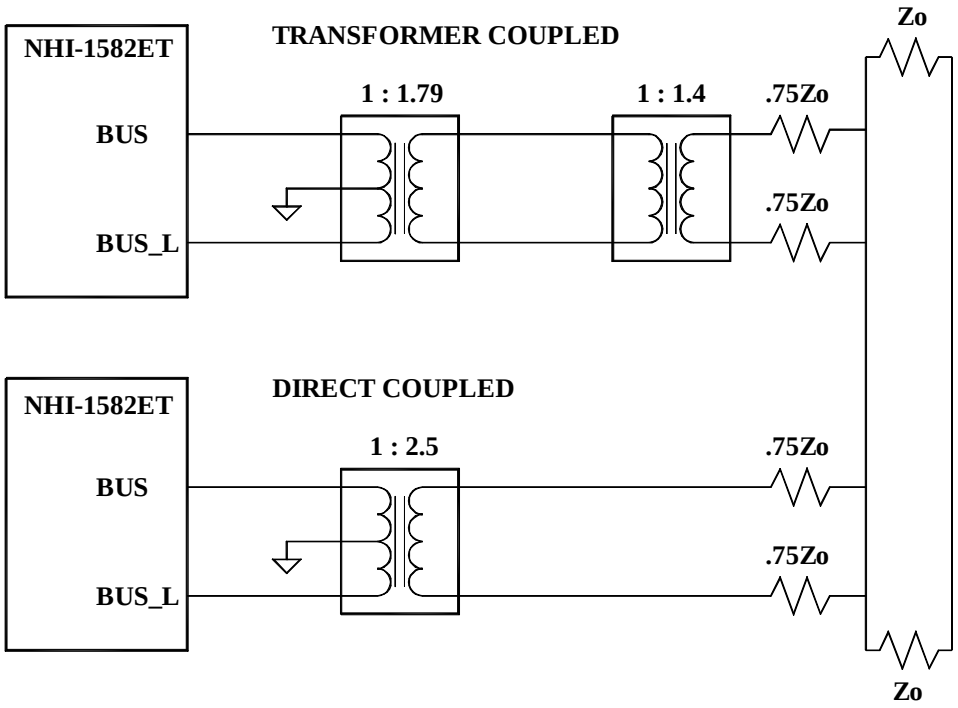


13.0.0 MATING TRANSFORMER REFERENCE

All the NHi-RT requires a coupling transformer with a turns ratio of 1: 2.5 for Direct Coupling, and a turns ratio of 1: 1.79 for Transformer Coupling to the Mil- Std- 1553 Bus. Technitrol part number Q1553- 45 or equivalent is recommended.

The center tap on the NHi-RT side of the coupling transformer must be grounded. The center tap on the bus side of the coupling transformer should be left floating.

The figure shows a typical transformer connection.

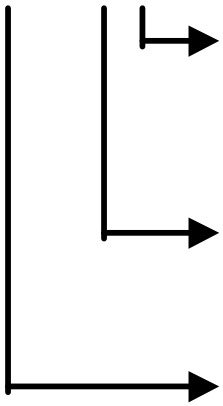


14.0.0 ORDERING INFORMATION

Unless otherwise specified, all terminals contain the following standard features:

- **Dual Redundant +5 Volt Only Operation**
- **Remote Terminal**
- **NHi Monolithic Transceivers**
- **16K Word Internal Ram**
- **Multi Protocol Compliant**
- **Trapezoidal Output Waveform**
- **Package Outline 1.1 x 1.1 inches**
- **Package Pins Defined in Pin Function Table**

NHi-15191RTGW/ 883



Grade

883	Compliant to MIL- PRF- 38534 Class H
M	MIL- PRF- 38534 Table VIII Device Screening.
T	Industrial Grade, MIL Temp: -55 to +125° C
Blank	Industrial, -40 to +85° C

Package

Blank	Plug- In
GW	Gull Wing lead formed surface mount flatpack
FP	FlatPack

Device

191RT	See Standard Features List.
192RT	Sinewave Output Waveform
202RT	Sinewave Output Waveform External Time Tag Input Replaces I/O_ADR2
302RT	Sinewave Output Waveform External Time Tag Input Replaces I/O_ADR2 Package Outline 0.95 x 0.95 inches.
391RT	Package Outline 0.95 x 0.95 inches.
392RT	Sinewave Output Waveform, Package Outline 0.95 x 0.95 inches.
991RT	Radiation Tolerant, Consult Factory for Details.
992RT	Sinewave Output Waveform, Radiation Tolerant, Consult Factory for Details.

**** SMD Listing: DESC Drawing# 5962- 91687**
See QML- 38534 for NHi Qualification under Mil- PRF- 38534