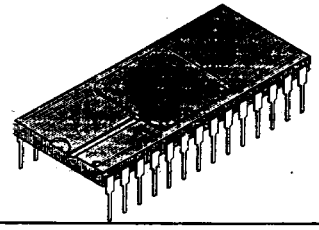
10/9Bit 20MSPS Sub-ranging A/D Converter (ECL I/O)

Description

CX20220A series is a high-speed, 20MSPS A/D converter which comes in two types of resolution, 10-bit and 9-bit, that are distinguished by the number suffixed to the name. Since a series-parallel system is used, an external sample hold circuit is required.

- Resolution: 10 bits (CX20220A-1)
  9 bits (CX20220A-2)
- Maximum conversion rate: 20MSPS
- Digitizing range: 0 to −2V
- Digital input/output: ECL level
- Output code: binary
- Low power consumption: 360 mW

28pin DIP (Ceramic)



Structure

Bipolar silicon monolithic IC

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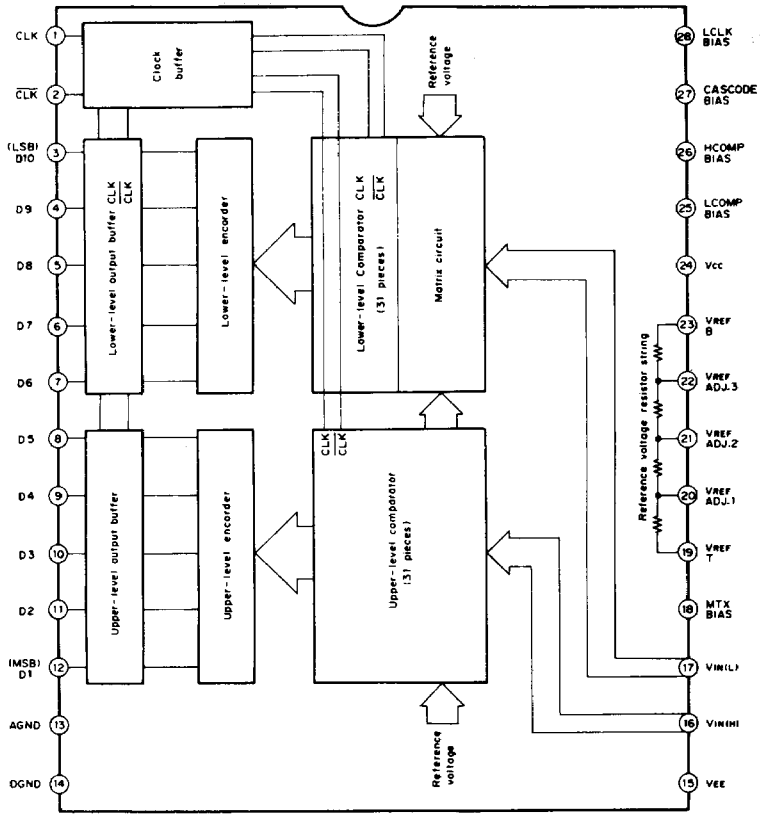
Block Diagram and Pin Configuration (Top View)



E89639-HP

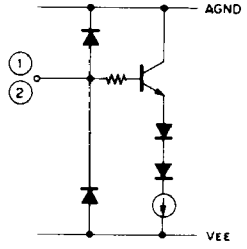
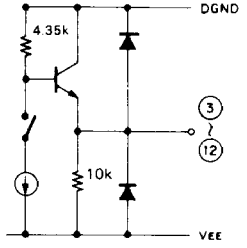
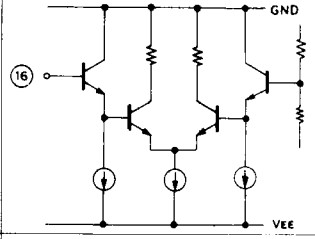
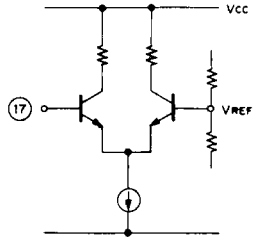
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	2.5	V
	V_{EE}	−7	V
• Analog voltage	V_I	V_{EE} to 0.3	V
• Clock input voltage	V_{CLK}, $V_{\overline{CLK}}$	V_{EE} to 0.3	V
• Reference voltage	V_{REF}	V_{EE} to 0.3	V
• Digital output current	I_{D01} to I_{D10}	0 to −20	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.23	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	1.6 to 2.1	V
	V_{EE}	−5.25 to −4.75	V
	A_{GND}-D_{GND}	−0.05 to +0.05	V
• Reference voltage	$V_{REF.T}$	0	V
	$V_{REF.B}$	−2.0	V
• Analog input voltage	V_I	$V_{REF.B}$ to $V_{REF.T}$	V
• Clock input voltage	V_{IH}	−1.1 min.	V
	V_{IL}	−1.4 max.	V
• Clock pulse width	T_{PW1}	20 min.	ns
	T_{PW0}	22 min.	ns

Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	CLK		Clock input pin, ECL level.
2	$\overline{\text{CLK}}$		Inverse clock input pin, ECL level
3	D10(LSB)		Digital output pin, ECL level, pull-down resistor (10KΩ) built in
4	D9		
5	D8		
6	D7		
7	D6		
8	D5		
9	D4		
10	D3		
11	D2		
12	D1(MSB)		
13	AGND		Analog ground pin
14	DGND		Digital ground pin
15	VEE		Power supply pin. To be grounded with ceramic chip capacitor of 0.1μF or over.
16	VIN(H)		Analog input pin (Upper level)
17	VIN(L)		Analog input pin (Lower level)

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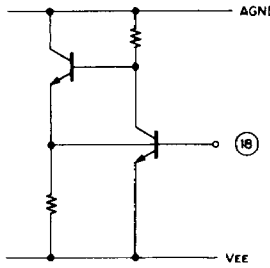
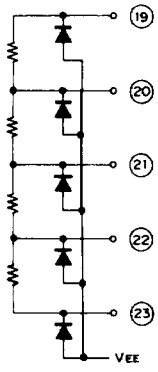
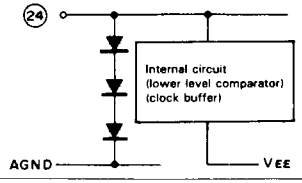
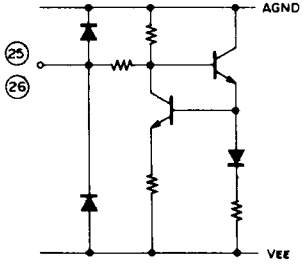
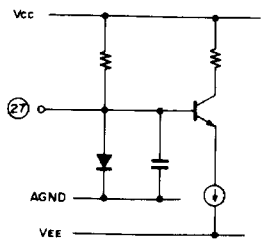
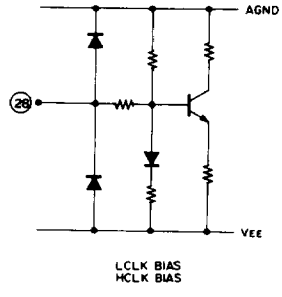
No.	Symbol	Equivalent circuit	Description
18	MTX BIAS		Pin connected internal matrix, which is normally used open.
19	VREF.T		Reference voltage pin (top), 0 V (typ.)
20	VREF ADJ. 1		Reference voltage adjusting pin. To be grounded with ceramic chip capacitor of 0.1μF or over.
21	VREF ADJ. 2		
22	VREF ADJ. 3		
23	VREF.B		Reference voltage pin (bottom), −2 V (typ.) To be grounded with ceramic chip capacifor of 0.1μF or over.
24	VCC		Internal power supply pin. Three diodes are incorporated in series, so that by connecting pull-up resistor to +5 V
25	LCOMP BIAS		Pin connected internal lower level comparator, which is normally used open.
26	HCOMP BIAS		Pin connected internal upper level comparator which is normally used open.

No.	Symbol	Equivalent circuit	Description
27	CASCODE BIAS		Cascode bias pin. To be bypassed to GND with ceramic capacitor of 0.1μF or over.
28	LCLK BIAS		Pin connected internal lower level buffer, which is normally used open.

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Electrical Characteristics (1) (See the Electrical Characteristics Test Circuit)

CX20220A-1 (10Bit) (Ta = 25°C, VCC = 1.6V, VEE = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								10		bit
Differential linearity error	Eo	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	EL	A	A	A	D	Differential waveform output				±1	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc=14.32MSPS nonlock		0.7		%
Differential phase error	DP	A	A	A		DA output			0.3		deg

CX20220A-2 (9Bit)

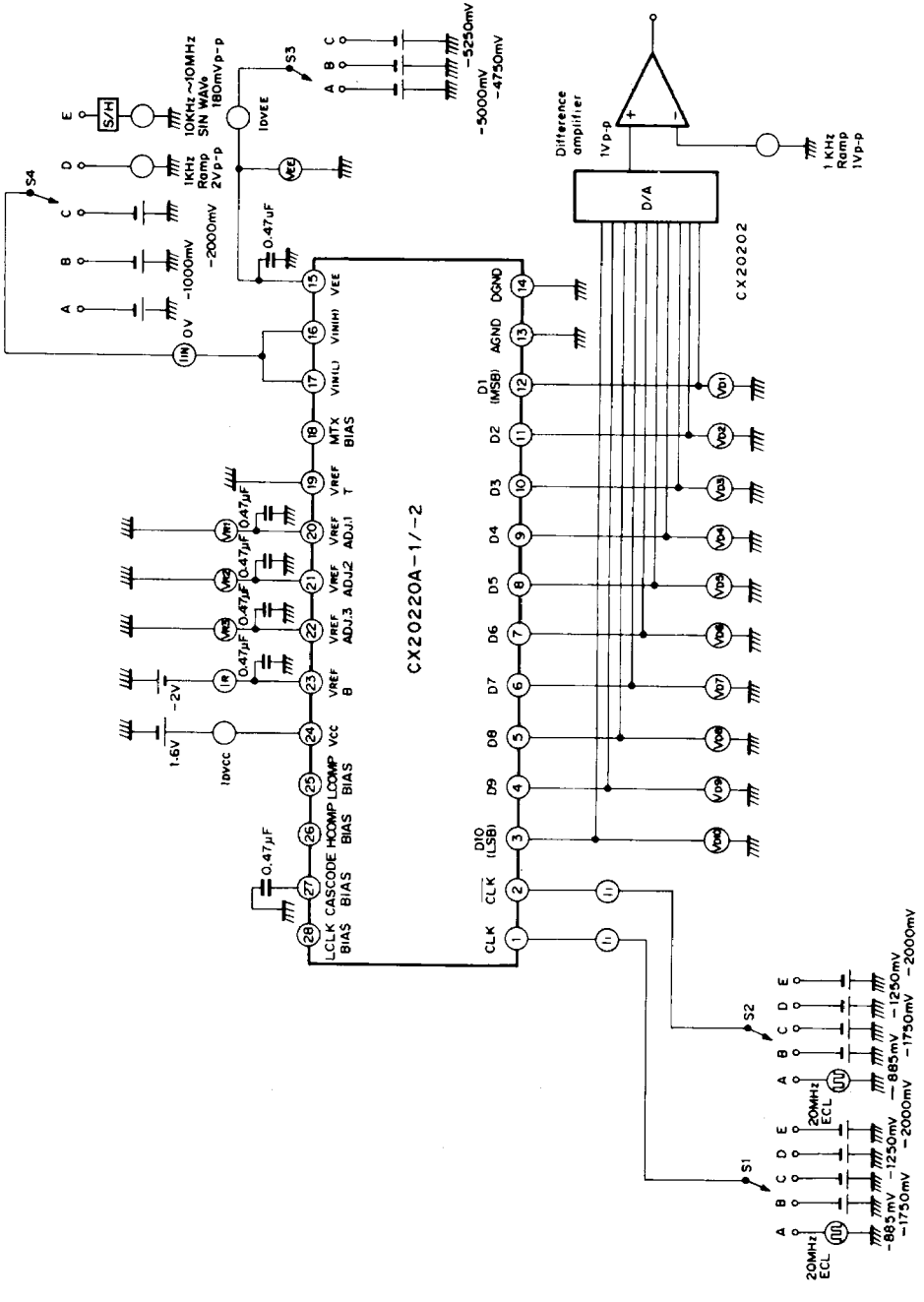
Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								9		bit
Differential linearity error	Eo	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	EL	A	A	A	D	Differential waveform output				±1/2	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc=14.32MSPS nonlock		1.0		%
Differential phase error	DP	A	A	A		DA output			0.5		deg

Electrical Characteristics (2) (See the Electrical Characteristics Test Circuit)

(Ta = 25°C, VCC = 1.6V, VEE = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Conversion rate	f_{max}	A	A	A	D	DA output		20			MSPS
Power consumption(1)	I_{DVCC}	B	D	A	A	I_{DVCC}			17	25	mA
Power consumption(2)	I_{DVEE}	B	D	A	A	I_{DVEE}		−80	−60		mA
Resistor string current	I_{REF}	B	D	A	A	I_R		−14	−12.5		mA
Resistor string pin voltage (1)	V_{R1}	B	D	A	A	V_{R1}		−0.51	−0.5	−0.49	V
Resistor string pin voltage (2)	V_{R2}	B	D	A	A	V_{R2}		−1.01	−1.0	−0.99	V
Resistor string pin voltage (3)	V_{R3}	B	D	A	A	V_{R3}		−1.51	−1.5	−1.49	V
Offset voltage, V_{RT} side	E_{OT}	B	C	A	A				2		mV
Offset voltage, V_{RB} side	E_{OB}	B	C	A	A				4		mV
Analog input current	I_{IN}	B	D	A	A	I_{IN}			40	80	μA
Analog input capacity (1)	C_{IN}	A	A	A			SW4: V_{IN} = 0V + 0.07 Vrms 4 MHz		230		pF
Analog input capacity (2)	C_{IN}	A	A	A			V_{IN} = −2V + 0.07 Vrms 4 MHz		190		pF
Analog input bandwidth	BW	A	A	A	E	DA output	Measurement of output amplitude		10		MHz
Digital input current (1)	I_{IH}	B	C	A	A	I_I			5	8	μA
Digital input current (2)	I_{IL}	E	D	A	A	I_I			5	8	μA
Inverse digital input current (1)	I_{IH}	C	B	A	A	I_I			5	8	μA
Inverse digital input current (2)	I_{IL}	D	E	A	A	I_I			5	8	μA
Digital output voltage, H level (1)	V_{IL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor.	−0.9	−0.8		V
Digital output voltage, H level (2)	V_{OH}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.0		V
Digital output voltage L level (1)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		−1.6	−1.5	V
Digital output voltage, L level (2)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.9		V
Output data delay (1)	Td	A	A	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		10		ns
Output data delay (2)	Td	A	A	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω		5		ns

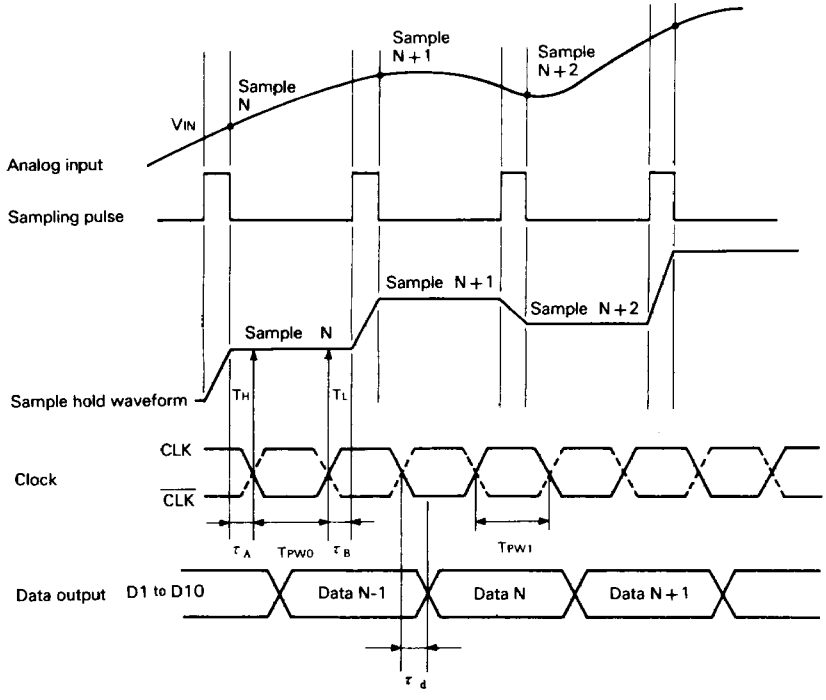
Electrical Characteristic Test Circuit



Reference Data for Standard Circuit Design

Clock Timing

CX20220A-1/-2 is a series-parallel-type A/D converter, and therefore an external sample and hold circuit is required. Careful timing, design should be made according to the timing chart shown below.
The timing design between the S/H output and the A/D clock is important.



Clock Timing

$\tau_A \geqq T_A$ (Aperture time + settling time of sample and hold circuit)

$\tau_B \geqq 2ns$

$T_{PW0} \geqq 22ns$

$T_{PW1} \geqq 20ns$

$\tau_d \leqq ns$

TH is the timing in which the upper level comparator compares VIN and VREF and latches the result. TL is the timing in which the lower level comparator compares VIN and VREF and latches the result. The simple method is for output data to be latched upon rising edge of CLK. Clock duty should be chosen so that the D G and DP per form the best result.

Digital Output (CX20220A-1)

In the output stages (pins 3 through 12), a10kΩ pull-down resistors are built in. A 1kΩ or larger resistance can further be connected to it externally.

D1 = MSB, D10 = LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB LSB 1 2 3 4 5 6 8 8 9 10
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1 1
·	1	1 1 1 1 1 1 1 1 1 0
·	2	1 1 1 1 1 1 1 1 0 1
·	·	·
·	·	·
·	·	·
·	5 1 1	1 0 0 0 0 0 0 0 0 1
·	5 1 2	1 0 0 0 0 0 0 0 0 0
·	5 1 3	0 1 1 1 1 1 1 1 1 1
·	·	·
·	·	·
·	·	·
·	1 0 2 2	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Digital Output (CX20220A-2)

D1=MSB, D9=LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB LSB 1 2 3 4 5 6 8 8 9
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1
·	1	1 1 1 1 1 1 1 1 0
·	2	1 1 1 1 1 1 1 0 1
·	·	·
·	·	·
·	·	·
·	2 5 5	1 0 0 0 0 0 0 0 1
·	2 5 6	1 0 0 0 0 0 0 0 0
·	2 5 7	0 1 1 1 1 1 1 1 1
·	·	·
·	·	·
·	·	·
·	5 1 0	0 0 0 0 0 0 0 0 1
$V_{REF.B}$	5 1 1	0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

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Ground Pin (AGND, DGND)

When mounting the converter on a printed circuit board, take as much space as possible for GND, to reduce impedance and resistance.

Power Supply Pin (VEE)

The VEE pin should be bypassed in the shortest way to AGND with a 0.1 μF or larger ceramic chip capacitor.

Power Supply Pin (VCC)

This is an internal power supply pin. Three diodes are incorporated in it in series, as shown in the equivalent circuit diagram, and its lower end is connected to AGND. Therefore, any desired VCC can be obtained by connecting a pull-up resistor to +5V. Be careful not to connect a capacitor between this pin and GND, because oscillation may result.

Reference Voltage Pin

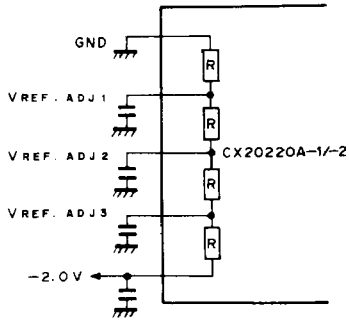
From this pin the reference voltage is supplied to the upper level and lower level comparators. Normally, VREF.T should be connected to GND, and VREF.B to −2.0V, respectively.

The interval between VREF.T and VREF.B constitutes a resistance of approximately 150 Ω, and upon application of −2.0V a current of approximately 13 mA will flow in it.

Any leakage of CLK to the reference voltage, will deteriorate the characteristics of the converter. To avoid this, it should be bypassed to AGND with a tantalum capacitor of 47 μF or over plus a ceramic chip capacitor of 0.1 μF or over.

Linearity Adjusting Pin (VREF.ADJ)

Adjusting pins are extended from reference resistors as shown below. Normally, these pins are connected to AGND with a 0.1 μF or larger ceramic chip capacitor. When adjustments are needed, connect them to AGND or VREF.B via resistance.



Sample & Hold Circuit

As noted in the explanation of the clock timing, it is desirable that the sample and hold circuit has some allowance for TA. A sample and hold circuit based on a diode bridge switch maybe used which performs the best result.

For more information, see Application Circuit (2).

Analog Input

Since CX20220A-1/-2 has an analog input capacitance of approximately 230pF, the buffer amplifier used to drive it must have a sufficient drive capability. Note that, if driven by a low-output-impedance buffer amplifier, a parasitic oscillation may result. This can be prevented by inserting a resistor of about 10 to 30 Ω between the output of the buffer amplifier and the A/D input in series.

Clock Input

The clock input is a complementary configuration.
Normally it should be driven with ECL circuit with complementary output.

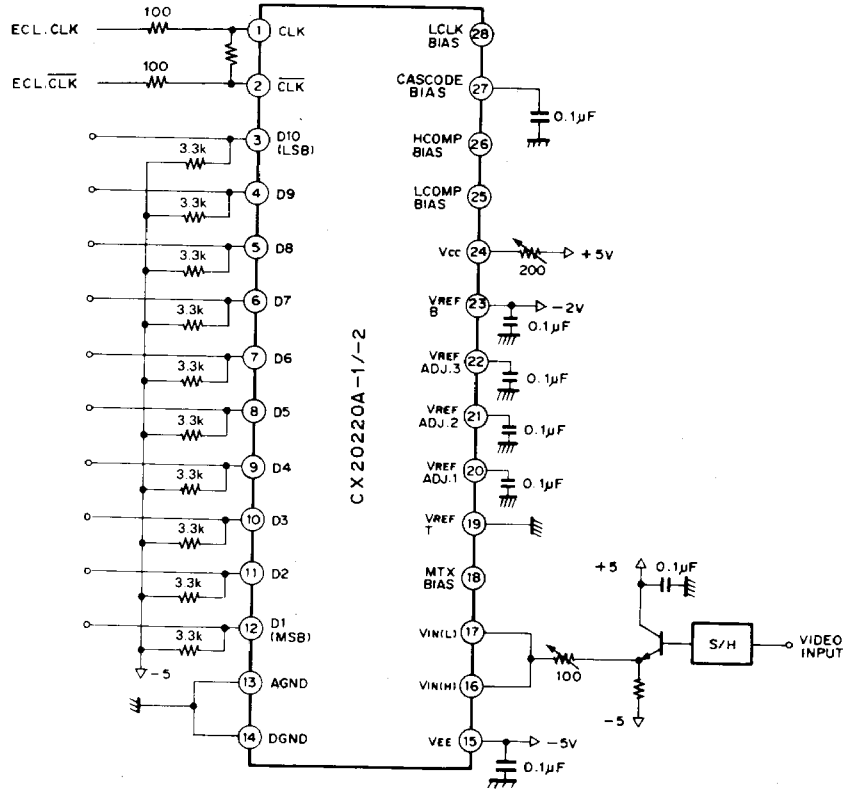
Digital Output (D1 through D10)

Although a 10kΩ pull-down resistor is built into the digital output stage, a 1kΩ or larger resistor can further be connected to it externally. In this case, however, care must be taken about changes in output level.

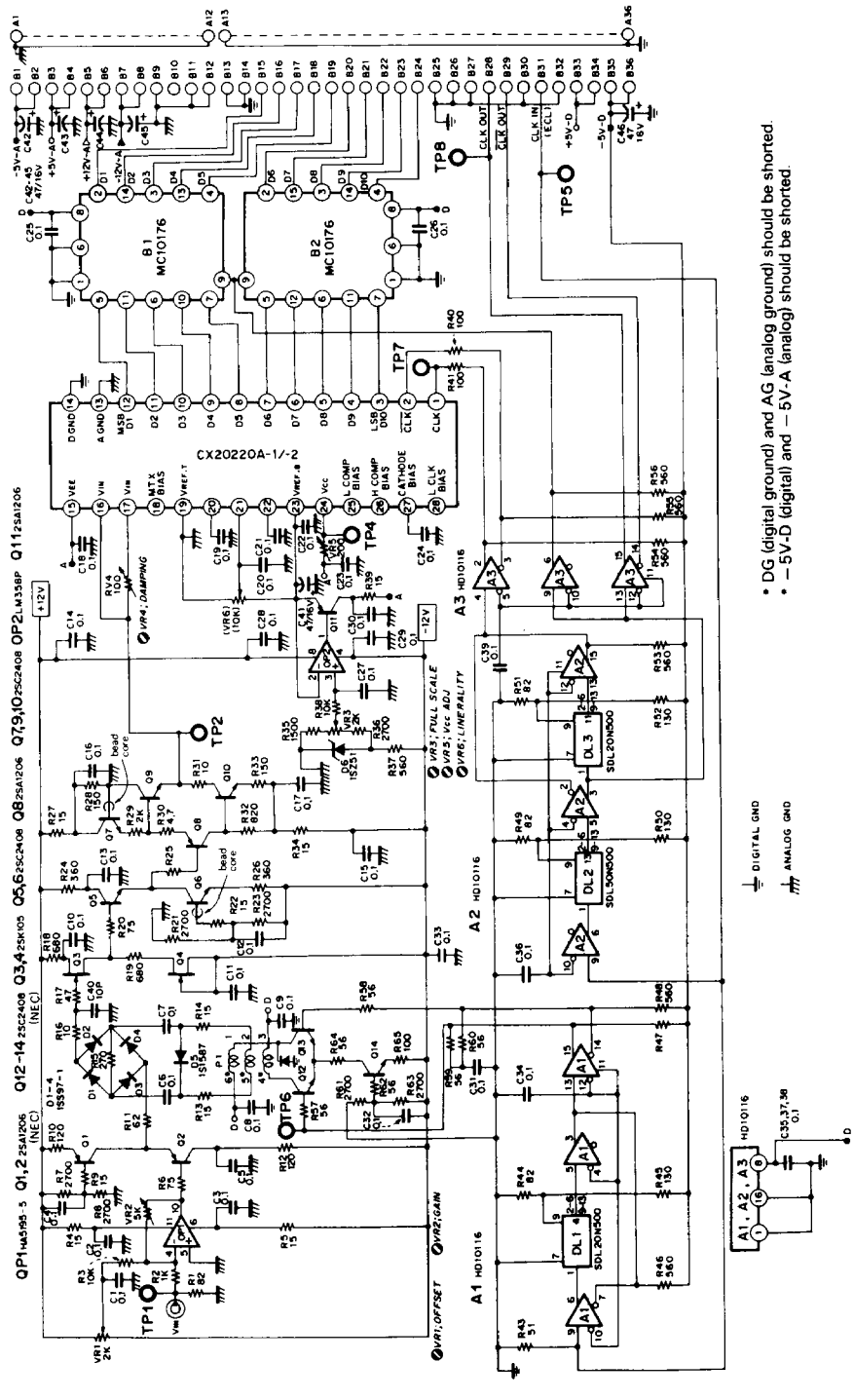
Other

Pin 18 (MTX BIAS), pin 25 (LCOM BIAS), pin 26 (HCOMP BIAS) and pin 28 (LCLK BIAS) are not used. These pins should never be connected to GND, power supply or any other pins.

Application Circuit (1)



Application Circuit (2)



Comparative Description of the System

CX20220A-1/-2 is based on a new series-parallel type. The following is a comparative explanation of the conventional and the new series-parallel types.

Series-Parallel Type (Conventional)

The series-parallel-type A/D converter is designed to accomplish A/D conversion in two steps, as shown in Fig. 1. With a 10-bit device, the level of the analog signal held in the sample hold (S/H) circuit is converted into a first set of parallel 5-bit digital output. This digital output is at the same time converted back into an analog signal, corresponding to the upper 5 bits. The difference between this signal and the level held at input is converted into digital signals in the parallel 5-bit A/D converter at the next stage, resulting in digital output for the lower 5 bits.

The number of comparators required for this system is $(2^5 - 1) \times 2 = 62$ pcs., bringing about a dramatic reduction in circuit size as compared to the 10-bit parallel type. However, since it does A/D conversion twice, once for the upper level and then again for the lower level, it takes longer conversion time, and also requires an S/H circuit to hold the input analog signal so that its level does not change when the lower 5 bits, are being converted, in addition both the 5-bit D/A converter and the subtractor, shown in Fig. 1, are required to possess a 10-bit equivalent accuracy.

New Series-Parallel Type

Essentially the new series-parallel-type A/D converter aims to reduce the number of comparators by doing A/D conversion twice, once for the upper bits and again for the lower bits, as in the case of the conventional series-parallel type. The distinguishing feature of this system, however, is that it does not require the D/A converter and the subtractor as shown in Fig. 2. Simply speaking this system is designed so that the input level held in the S/H circuit is first A/D converted for the upper 5 bits, and upon receipt of control signal from the upper level encoder, the lower level A/D converter is operated.

To simplify the operating principle of this system, Fig. 3 shows an example which consists of an upper 2 bits and lower 2 bits, a total of 4 bits. The upper and lower level circuits each consist of three comparators, switch trains S1 through S4, a single 16-segmented resistor, and an encoder.

Input level V_{IN} held by the S/H circuit is determined by the upper level comparator to be at a level of $V_{REF.T}$ to V_1, V_1 to V_1 to V_2, V_2 to V_3, or V_3 to $V_{REF.B}$. The result of judgement is converted into upper 2-bit digital output through the upper level encoder. At the same time, one of the switch trains S1 to S4 is turned on, according to the level of V_{IN}. As it switches on, reference voltage is supplied to the lower level comparator, and elaborate comparative judgement is made at the interval of $(V_{REF}/4)$, resulting in output of the lower 2 bits from the lower level encoder.

Since this system uses the same resistor strings in common for the upper and lower levels, simplicity is maintained. Furthermore, since this system requires fewer comparators, input bias current for the comparators is reduced accordingly.

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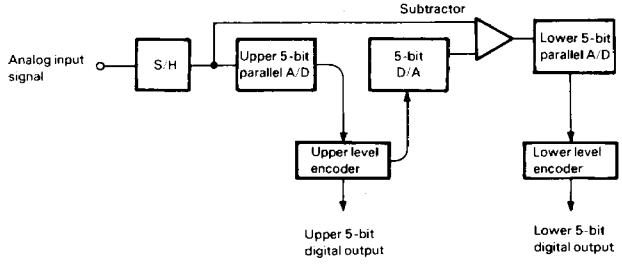


Fig. 1 Configuration of Series-Parallel 10-Bit A/D Converter

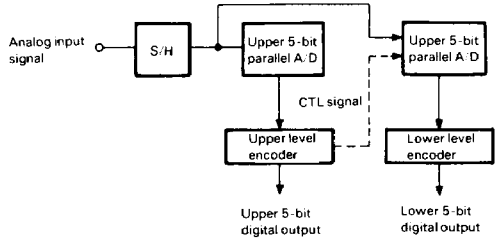


Fig. 2 Configuration of the New Series-Parallel 10-Bit A/D Converter

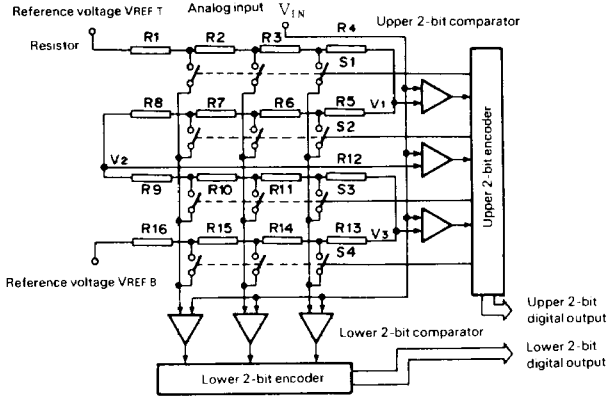
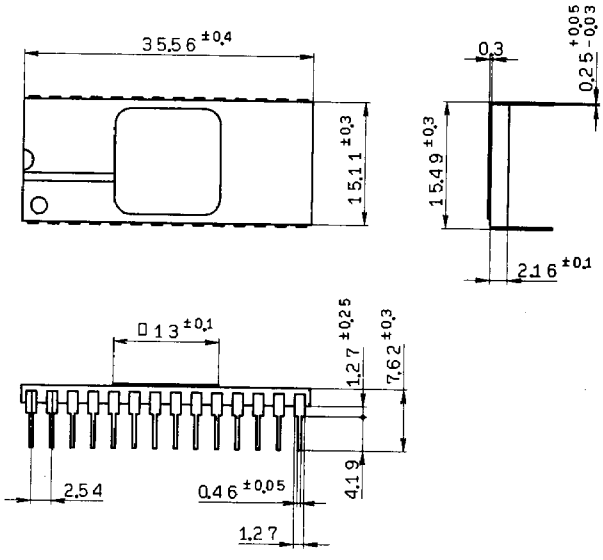


Fig. 3 Operating Principle of the New Series-Parallel Type (Ex.: 4-bit device)

Package Outline Unit : mm

28pin DIP(Ceramic) 600mil 4.8g



DIP-28C-01

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