

DRAM

64K x 16 DRAM

STATIC COLUMN MODE

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V±10% power supply
- Low power, 3mW standby; 225mW active, typical
- All device pins are fully TTL compatible
- 256 cycle refresh in 4ms
- Refresh modes: $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ and HIDDEN
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 only)

OPTIONS

- Timing
 - 70ns access
 - 80ns access
 - 100ns access
- Write Enable
 - Byte or Word
 - Word only
- Mask Enable
 - Not Available
 - Always Available
- Packages
 - Plastic SOJ (400mil)
 - Plastic TSOP (400mil)
 - Plastic ZIP (475mil)

MARKING

7	- 7
8	- 8
10	-10
MT4C1670	MT4C1670
MT4C1671	MT4C1671
MT4C1670	MT4C1670
MT4C1671	MT4C1671
DJ	DJ
TG	TG
Z	Z

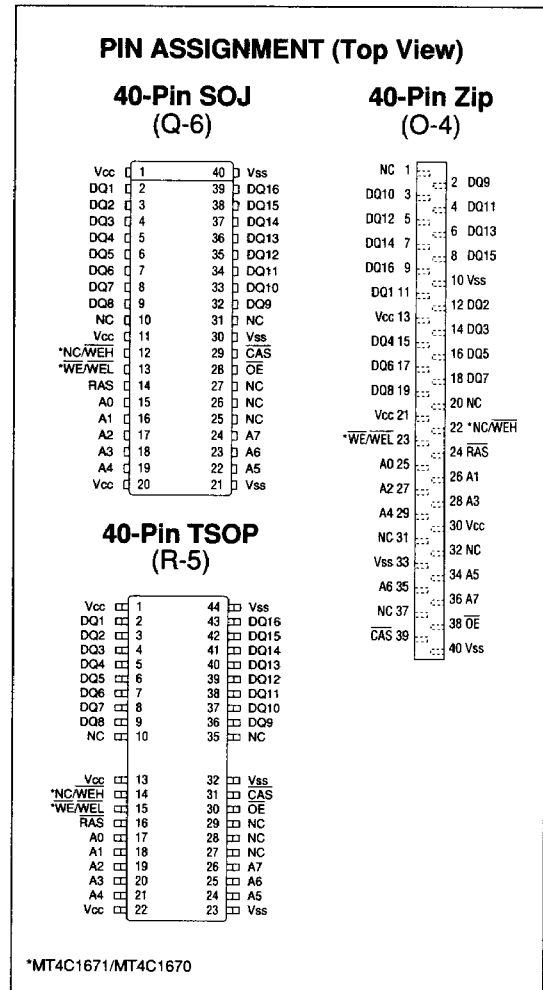
NOTE: Available in die form Please consult factory for die data sheets.

GENERAL DESCRIPTION

The MT4C1670/1 are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 has both BYTE and WORD WRITE access cycles while the MT4C1671 has only WORD WRITE access cycles.

The MT4C1670 functions in a similar manner to the MT4C1671 except that replacing WE with WEL and WEH allows for BYTE WRITE access cycles. WEL and WEH function in an identical manner to WE: either WEL or WEH will generate an internal WE through an AND gate (Inverted NOR gate).

The MT4C1670 "WE" function and timing are determined by the first BYTE WRITE (WEL or WEH) to transition LOW



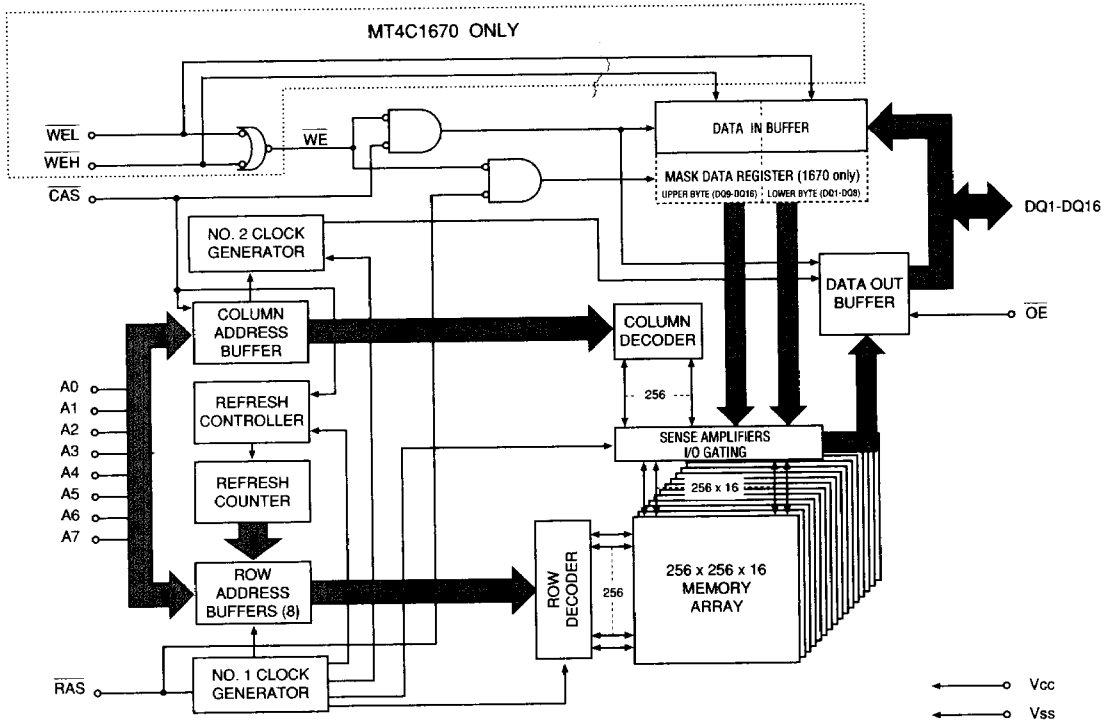
WIDE DRAM

and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: WEL transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or WEH transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 has NONPERSISTENT MASKED WRITE capability.

FUNCTIONAL BLOCK DIAGRAM

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PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{\text{RAS}}$	Input	ROW Address Strobe: $\overline{\text{RAS}}$ is used to clock-in the 8 row address bits and strobe the $\overline{\text{WEL}}$, $\overline{\text{WEH}}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{\text{CAS}}$	Input	Column Address Strobe: $\overline{\text{CAS}}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{\text{OE}}$	Input	Output Enable: $\overline{\text{OE}}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must be LOW and $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ must be HIGH before $\overline{\text{OE}}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{\text{WE/WEL}}^*$	Input	Write Enable Lower Byte: $\overline{\text{WEL}}$ on MT4C1670 is $\overline{\text{WE}}$ control for the DQ1 through DQ8 inputs. $\overline{\text{WE}}$ on MT4C1671 controls DQ1 through DQ16 inputs. If ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$)/ $\overline{\text{WE}}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	$\overline{\text{NC/WEH}}^*$	Input	Write Enable Upper Byte: $\overline{\text{WEH}}$ on MT4C1670 is $\overline{\text{WE}}$ control for the DQ9 through DQ16 inputs. If ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$)/ $\overline{\text{WE}}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITES can be performed by using $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM location. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	10, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V \pm 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671/MT4C1670

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{\text{RAS}}$ is used to latch the first 8 bits and $\overline{\text{CAS}}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1671 are selected with the $\overline{\text{WE}}$ input while either $\overline{\text{WEL}}$ or $\overline{\text{WEH}}$ perform the "WE" on the MT4C1670. The MT4C1670 "WE" function is determined by the first BYTE WRITE ($\overline{\text{WEL}}$ or $\overline{\text{WEH}}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Taking $\overline{\text{WE}}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ remain LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{\text{OE}}$, $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ (MT4C1670) or $\overline{\text{WE}}$ (MT4C1671).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$ followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have $\overline{\text{CAS}}$ or $\overline{\text{WE}}$ toggled strobing-in the different column addresses. Returning $\overline{\text{RAS}}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ -ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, or HIDDEN refresh) so that all 256 combinations of $\overline{\text{RAS}}$ addresses (A0-A7) are executed at least every 4ms, regardless of

sequence. The $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BYTE WRITE ACCESS CYCLE (MT4C1670 ONLY)

The BYTE WRITE mode is determined by the use of $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$. Enabling $\overline{\text{WEL}}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{\text{WEH}}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{\text{WEL}}$ and $\overline{\text{WEH}}$ selects a WORD WRITE cycle.

The MT4C1670 may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the $\overline{\text{WE}}$ input. Figure 1 illustrates the MT4C1670 BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{\text{WE}}$ at $\overline{\text{RAS}}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{\text{WE}}$ is LOW at $\overline{\text{RAS}}$ time. The MT4C1671 is only word selectable when $\overline{\text{WE}}$ is LOW at $\overline{\text{RAS}}$ time (the MT4C1670 does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{\text{RAS}}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{\text{CAS}}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 MASKED WRITE operation (Note: $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ time refers to the time at which $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ transition from HIGH to LOW).

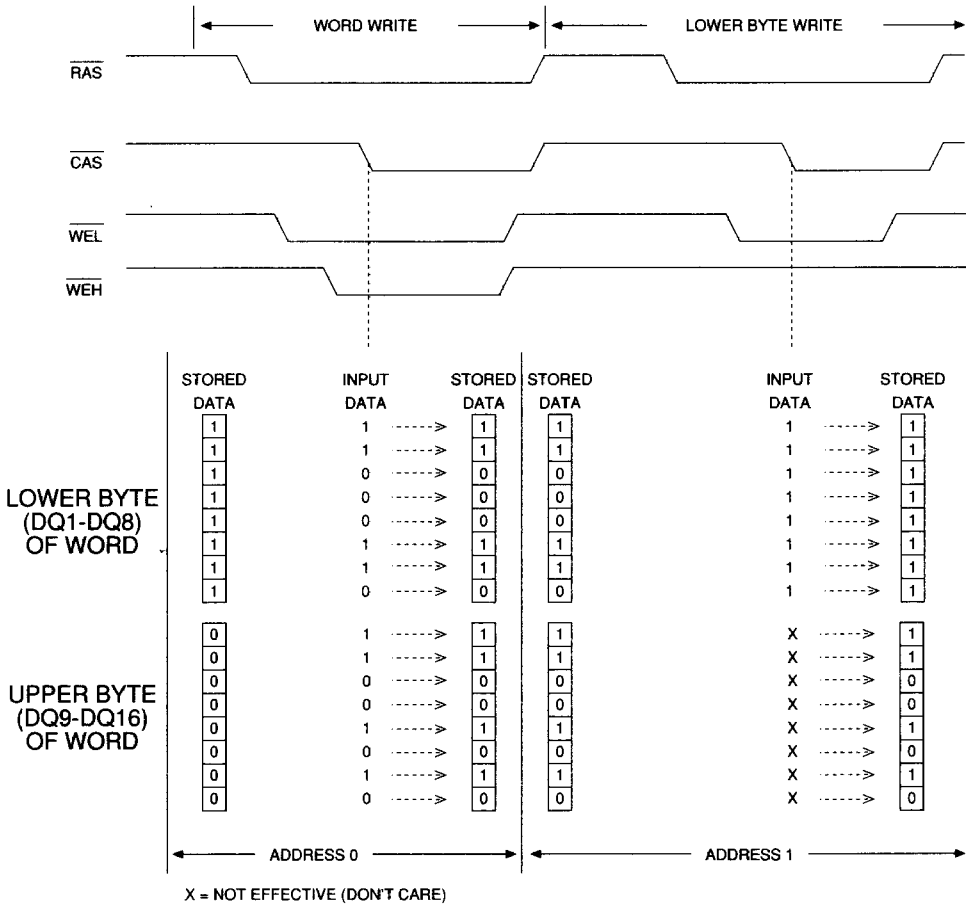


Figure 1
MT4C1670 WORD AND BYTE WRITE EXAMPLE

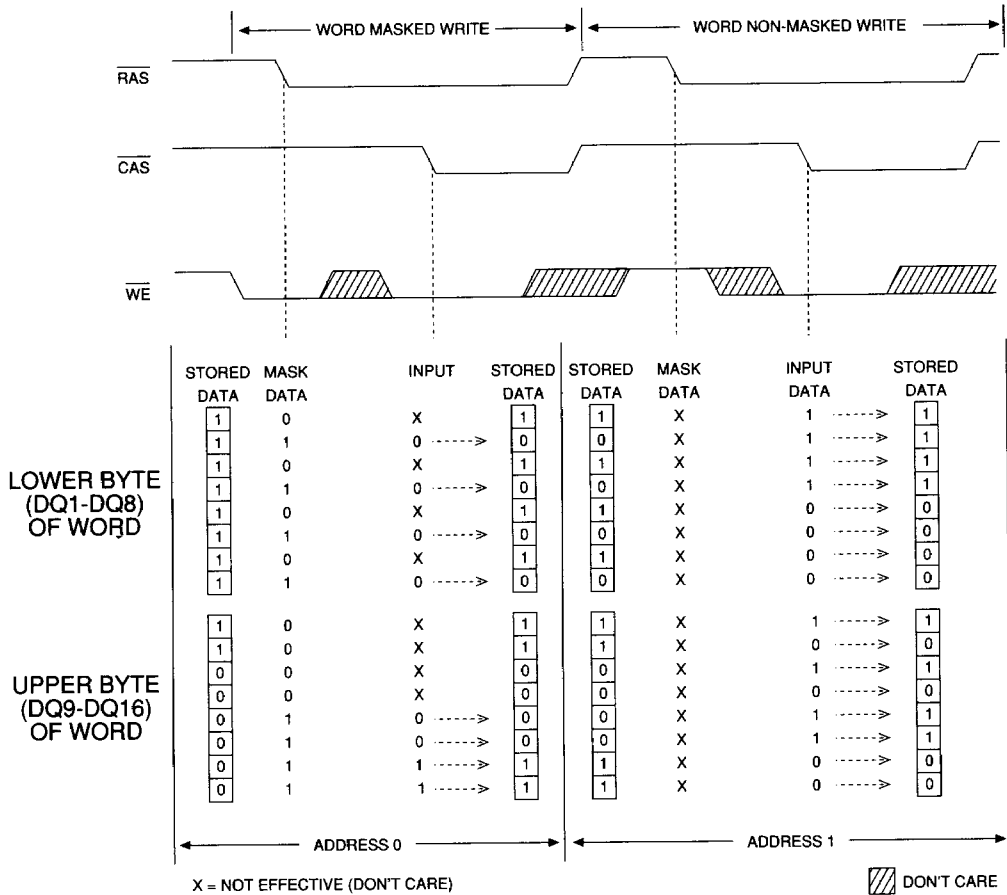


Figure 2
MT4C1671 MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1670

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES		DQs	NOTES
							r	c		
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	

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- NOTE:**
1. These cycles may also be BYTE WRITE cycles (either \overline{WEL} or \overline{WEH} active).
 2. EARLY-WRITE only.
 3. Either CAS or \overline{WEL} / \overline{WEH} must latch in each additional column address and input data.

TRUTH TABLE: MT4C1671

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DQs	NOTES
						r	c		
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN READ	1st Cycle	L	L	H	L	ROW	COL	Data Out	
	2nd Cycle	L	L	H	L	n/a	COL	Data Out	
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	X	ROW	COL	Data In	1
	2nd Cycle	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	

- NOTE:**
1. Data-in will be dependent on the mask provided. Refer to Figure 2.
 2. EARLY-WRITE only.
 3. Either CAS or WEL / WEH must latch in each additional column address and input data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1.0V to +7.0V
 Operating Temperature, T_A (Ambient) 0°C to +70°C
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V _{IN} ≤ V _{CC} (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	
OUTPUT LEVELS	V _{OH}	2.4		V	
Output High Voltage (I _{OUT} = -2.5mA)					
Output Low Voltage (I _{OUT} = 2.1mA)	V _{OL}		0.4	V	

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PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-7	-8	-10		
STANDBY CURRENT: (TTL) (R _{AS} = C _{AS} = V _{IH})	I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) (R _{AS} = C _{AS} = V _{CC} - 0.2V)	I _{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC3}	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current (R _{AS} = V _{IL} ; C _{AS} , Address Cycling: t _{SC} = t _{SC} (MIN))	I _{CC4}	110	95	80	mA	3, 4, 31
REFRESH CURRENT: R _{AS} -ONLY Average power supply current (R _{AS} Cycling, C _{AS} =V _{IH} : t _{RC} = t _{RC} (MIN))	I _{CC5}	120	115	90	mA	3, 31
REFRESH CURRENT: C _{AS} -BEFORE-R _{AS} (CBR) Average power supply current (R _{AS} , C _{AS} , Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC6}	120	115	90	mA	3, 5

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C _{I1}		5	pF	2
Input Capacitance: RAS, CAS, (WEL, WEH)/ WE, OE	C _{I2}		7	pF	2
Input/Output Capacitance: DQ	C _{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	¹ RC	130		150		180		ns	
READ-WRITE cycle time	¹ RWC	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	¹ SC	45		50		55		ns	
STATIC-COLUMN READ-WRITE cycle time	¹ SRWC	95		100		120		ns	
Access time from RAS	¹ RAC		70		80		100	ns	14
Access time from CAS	¹ CAC		25		35		40	ns	15
Output Enable time	¹ OE		25		35		40	ns	
Access time from column address	¹ AA		40		45		55	ns	
Access time from CAS precharge	¹ CPA		45		50		55	ns	
RAS pulse width	¹ RAS	70	100,000	80	100,000	100	100,000	ns	
RAS pulse width (STATIC COLUMN)	¹ RASC	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	¹ RSH	20		35		40		ns	
RAS precharge time	¹ RP	50		60		70		ns	
CAS pulse width	¹ CAS	25	100,000	35	100,000	40	100,000	ns	
CAS hold time	¹ CSH	70		80		100		ns	
CAS precharge time	¹ CPN	10		10		15		ns	16
CAS precharge time (STATIC COLUMN)	¹ CP	10		10		10		ns	
RAS to CAS delay time	¹ RCD	20	45	20	45	25	60	ns	17
CAS to RAS precharge time	¹ CRP	5		10		10		ns	
Row address setup time	¹ ASR	0		0		0		ns	
Row address hold time	¹ RAH	10		12		15		ns	
RAS to column address delay time	¹ RAD	15	35	17	40	20	55	ns	18
Column address setup time	¹ ASC	0		0		0		ns	
Column address hold time	¹ CAH	15		15		20		ns	
Column address hold time (referenced to RAS)	¹ AR	55		60		70		ns	
Column address to RAS lead time	¹ RAL	35		45		55		ns	
Read command setup time	¹ RCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	¹ RCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	¹ RRH	0		10		10		ns	19
CAS to output in Low-Z	¹ CLZ	0		0		0		ns	
Output buffer turn-off delay	¹ OFF	0	20	0	20	0	20	ns	20, 30

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

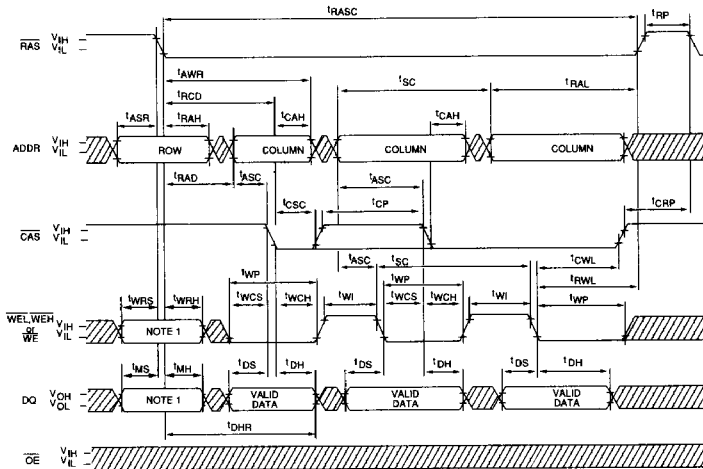
AC CHARACTERISTICS	SYM	-7		-8		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Output disable time	t_{OD}		15		20		20	ns	30
Write command setup time	t_{WCS}	0		0		0		ns	21, 26
Write command hold time	t_{WCH}	15		15		20		ns	26
Write command hold time (referenced to \overline{RAS})	t_{WCR}	50		55		70		ns	26
Write command pulse width	t_{WP}	15		15		20		ns	26
Write command to \overline{RAS} lead time	t_{RWL}	20		35		40		ns	26
Write command to \overline{CAS} lead time	t_{CWL}	20		35		40		ns	26
Data-in setup time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		15		20		ns	22
Data-in hold time (referenced to \overline{RAS})	t_{DHR}	50		60		70		ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	90		100		125		ns	21
Column address to \overline{WE} delay time	t_{AWD}	65		70		80		ns	21
\overline{CAS} to \overline{WE} delay time	t_{CWD}	50		55		70		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	28
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	0		10		10		ns	
\overline{CAS} setup time (\overline{CAS} -BEFORE- \overline{RAS} refresh)	t_{CSR}	10		10		10		ns	5
\overline{CAS} hold time (\overline{CAS} -BEFORE- \overline{RAS} refresh)	t_{CHR}	15		25		30		ns	5
MASKED WRITE command to \overline{RAS} setup time	t_{WRS}	0		0		0		ns	26, 27
MASKED WRITE command to \overline{RAS} hold time	t_{WRH}	15		15		15		ns	26, 27
Mask data to \overline{RAS} setup time	t_{MS}	0		0		0		ns	26
Mask data to \overline{RAS} hold time	t_{MH}	15		15		15		ns	26
\overline{OE} hold time from \overline{WE} during READ-MODIFY-WRITE cycle	t_{OEH}	10		20		20		ns	29
\overline{OE} setup prior to \overline{RAS} during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	
Last WRITE to column address delay	t_{LWAD}	20	30	20	35	25	45	ns	
Access time from last WRITE	t_{ALW}	65		75		95		ns	
Output data enable from WRITE	t_{OW}	t_{AA}		t_{AA}		t_{AA}		ns	
Output data hold time from column address	t_{AOH}	5		5		5		ns	
\overline{RAS} hold time referenced to \overline{OE}	t_{ROH}	10		10		10		ns	
Column address hold time referenced to \overline{RAS} HIGH	t_{AH}	5		5		10		ns	
\overline{CAS} pulse width in STATIC-COLUMN mode	t_{CSC}	t_{CAS}		t_{CAS}		t_{CAS}		ns	
Write command inactive time	t_{WI}	10		10		10		ns	

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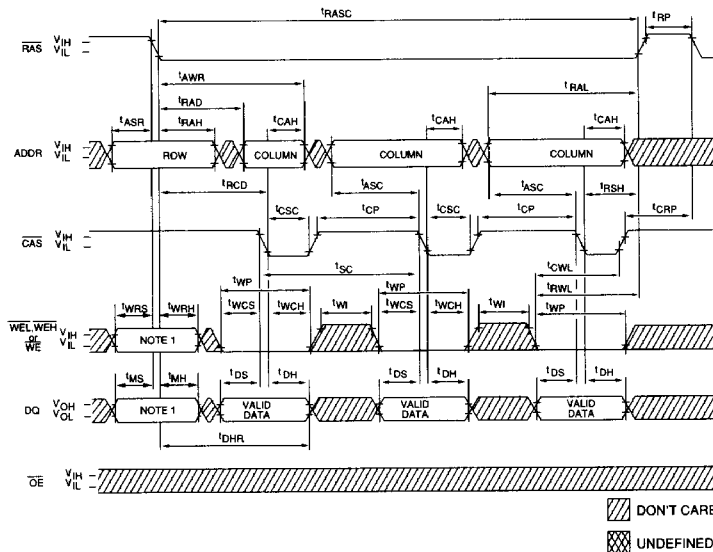
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100μs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume t_T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is High-Z.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that t_{RCD} < t_{RCD} (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that t_{RCD} ≥ t_{RCD} (MAX).
16. If \overline{CAS} is LOW at the falling edge of RAS, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, \overline{CAS} must be pulsed HIGH for t_{CPN}.
17. Operation within the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, then access time is controlled exclusively by t_{CAC}.
18. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, then access time is controlled exclusively by t_{AA}.
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If t_{WCS} ≥ t_{WCS} (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN), t_{AWD} ≥ t_{AWD} (MIN) and t_{CWD} ≥ t_{CWD} (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (\overline{OE} controlled) cycle.
22. These parameters are referenced to \overline{CAS} leading edge in early WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If \overline{OE} is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.
25. All other inputs at V_{CC} -0.2V.
26. WRITE command is defined as either \overline{WEL} or \overline{WEH} or both going LOW on the MT4C1670. WRITE command is defined as \overline{WE} going LOW on the MT4C1671.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. The refresh period may be extended to 8ms without experiencing problems.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met (\overline{OE} HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if \overline{CAS} remains LOW and \overline{OE} is taken back LOW after t_{OEH} is met. If \overline{CAS} goes HIGH prior to \overline{OE} going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If \overline{CAS} goes HIGH first, \overline{OE} becomes a "don't care." If \overline{OE} goes HIGH and \overline{CAS} stays LOW, \overline{OE} is not a "don't care," and the DQs will provide the previously read data if \overline{OE} is taken back LOW (while \overline{CAS} remains LOW).
31. Column address changed once while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

**STATIC-COLUMN EARLY-WRITE CYCLE
(WE CONTROLLED)**



**STATIC-COLUMN EARLY-WRITE CYCLE
(CAS CONTROLLED)**



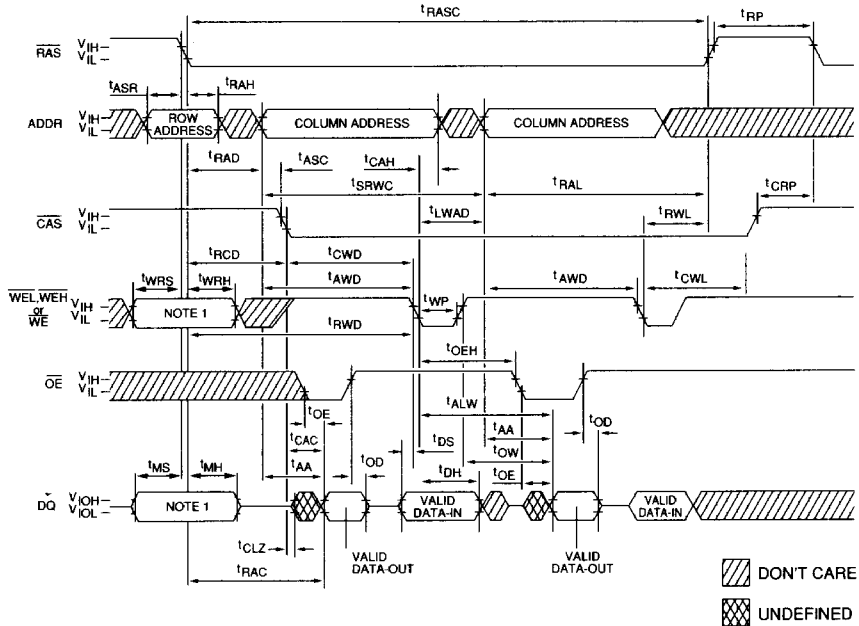
▨ DON'T CARE
▩ UNDEFINED

NOTE: 1. Applies to MT4C1671 only; WEL, WEH and DQ inputs on MT4C1670 are "don't care" at \overline{RAS} time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

WIDE DRAM

**STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**

WIDE DRAM



NOTE: 1. Applies to MT4C1671 only; \overline{WEL} , \overline{WEH} and DQ inputs on MT4C1670 are "don't care" at \overline{RAS} time. \overline{WE} selects between normal WRITE and MASKED WRITE at \overline{RAS} time. The DQ inputs are "don't care" for a normal WRITE, \overline{WE} HIGH at \overline{RAS} time. The DQ inputs provide the mask data at \overline{RAS} time for a MASKED WRITE, \overline{WE} LOW at \overline{RAS} time.

