

Dual J-K Flip-Flop with Preset and Clear

The TC74HC109A is a high speed CMOS DUAL J-K FLIP-FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

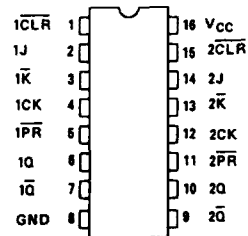
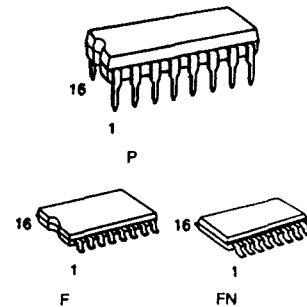
In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

CLEAR and **PRESET** are independent of the clock and are accomplished by a low logic level on the corresponding input.

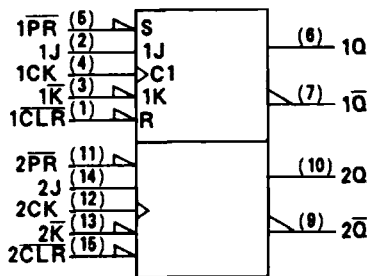
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: $f_{MAX} = 63\text{MHz(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%V_{CC}(\text{Min.})$
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: $V_{CC}(\text{opr}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS109



(TOP VIEW)
Pin Assignment



IEC Logic Symbol

Truth Table

Inputs					Outputs		Function
CLR	PR	J	K	CK	Q	Q̄	
L	H	X	X	X	L	H	Clear
H	L	X	X	X	H	L	Preset
L	L	X	X	X	H	H	-
H	H	L	H	↺	Q _n	Q̄ _n	No Change
H	H	L	L	↺	L	L	-
H	H	H	H	↺	H	L	-
H	H	H	L	↺	Q̄ _n	Q _n	Toggle
H	H	X	X	↺	Q _n	Q̄ _n	No Change

X: Don't Care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 - 7	V
DC Input Voltage	V_{IN}	-0.5 - $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 - $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 - 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 - 6	V
Input Voltage	V_{IN}	0 - V_{CC}	V
Output Voltage	V_{OUT}	0 - V_{CC}	V
Operating Temperature	T_{opr}	-40 - 85	°C
Input Rise and Fall Time	t_r, t_f	0 - 1000($V_{CC} = 2.0\text{V}$) 0 - 500($V_{CC} = 4.5\text{V}$) 0 - 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		Unit		
			V_{CC}	Min	Typ.	Max.	Min.		Max.	
High-Level Input Voltage	V_{IH}	-	2.0 4.5 6.0	1.5 3.15 4.2	- - -	- - -	1.5 3.15 4.2	- - -	V	
Low-Level Input Voltage	V_{IL}	-	2.0 4.5 6.0	- - -	- - -	0.5 1.35 1.8	- - -	0.5 1.35 1.8	- - -	V
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	- - -	1.9 4.4 5.9	- - -	V
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	- - -	0.0 0.0 0.0	0.1 0.1 0.1	- - -	0.1 0.1 0.1	V
			$I_{OL} = 4\text{mA}$ $I_{OL} = 5.2\text{mA}$	4.5 6.0	- -	0.17 0.18	0.26 0.26	- -	0.33 0.33	V
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	± 0.1	-	± 1.0	-	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	2.0	-	20.0	-	μA

Timing Requirements (Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V _{CC}	Typ.	Limit	Limit		
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	-	2.0	-	75	95		ns
			4.5	-	15	19		
			6.0	-	13	16		
Minimum Pulse Width (PR, CLR)	$t_{W(L)}$	-	2.0	-	75	95		
			4.5	-	15	19		
			6.0	-	13	16		
Minimum Set-up Time	t_s	-	2.0	-	75	95		
			4.5	-	15	19		
			6.0	-	13	16		
Minimum Hold Time	t_h	-	2.0	-	0	0		
			4.5	-	0	0		
			6.0	-	0	0		
Minimum Removal Time (PR, CLR)	t_{rem}	-	2.0	-	50	65		
			4.5	-	10	13		
			6.0	-	9	11		
Clock Frequency	f	-	2.0	-	6	5		MHz
			4.5	-	31	25		
			6.0	-	36	29		

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

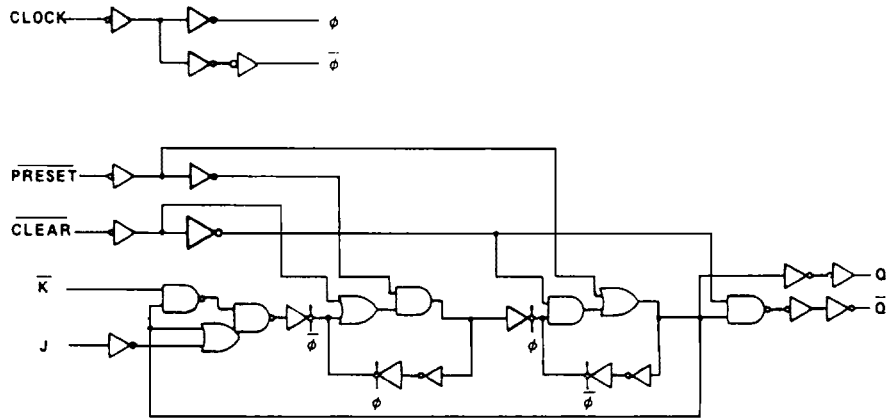
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit						
Output Transition Time	t_{TLH} t_{THL}	-	-	6	12	ns						
							Propagation Delay Time (CLOCK - Q, \bar{Q})	t_{PLH} t_{PHL}	-	-	13	26
Propagation Delay Time (PR, CLR - Q, \bar{Q})	t_{PLH} t_{PHL}	-	-	12	26							

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C				Ta = -40 ~ 85°C		Unit
			V _{CC}	Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	-	2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, \bar{Q})	t_{PLH} t_{PHL}	-	2.0	-	50	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	13	26	-	32	
Propagation Delay Time (PR, CLR - Q, \bar{Q})	t_{PLH} t_{PHL}	-	2.0	-	50	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	13	26	-	32	
Maximum Clock Frequency	f_{MAX}	-	2.0	6	17	-	5	-	MHz
			4.5	31	59	-	25	-	
			6.0	36	67	-	29	-	
Input Capacitance	C _{IN}	-	-	5	10	-	10	pF	
Power Dissipation Capacitance	C _{PD(1)}	-	-	41	-	-	-		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(DD)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2(\text{per F/F})$$



Logic Diagram (1/2 package)