Features

1Mx1 bit CMOS Dynamic
Random Access Memory

- Access Times 70, 80, 100ns
- 8ms Refresh Rate
- Low Operating Power Dissipation
- Low Standby Power
- All Inputs/Outputs TTL Compatible

Package Styles

- 18 Pin DIP, No. 1
- 20(26) Lead Ceramic SOJ, No. 16
- 20 pin Ceramic ZIP, No.18
- 20 Lead Flatpack, No. 78

Single +5V (±10%) Supply Operation

1Megabit x 1 Dynamic RAM
CMOS, Monolithic

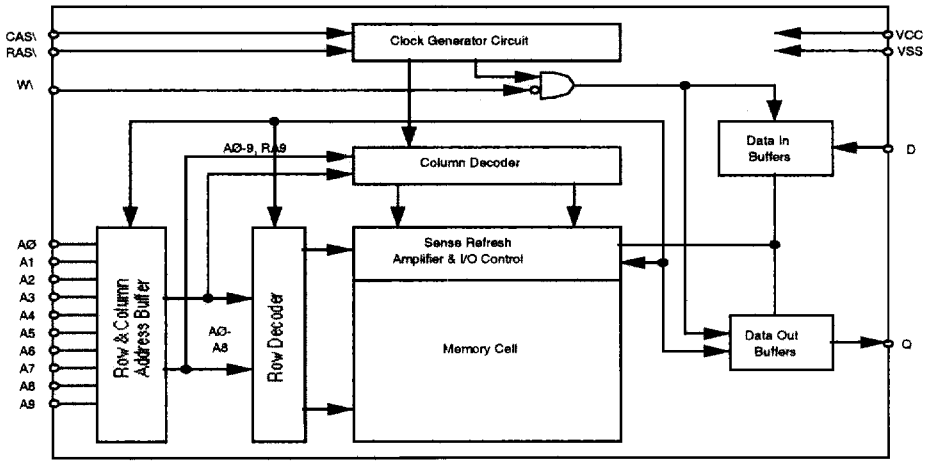
The EDI411204C is a high performance, low power CMOS Dynamic RAM organized as 1Megabit x1.

During Read and Write cycles each bit is addressed through 20 address bits which are entered 10 at a time (AØ - A9). RAS\ is used to latch the first 10 bits and CAS\, the second 10 bits. A READ or WRITE cycle is selected with the W\ input. A logic HIGH on W\ dictates READ mode, while a logic LOW on W\ dictates WRITE mode.

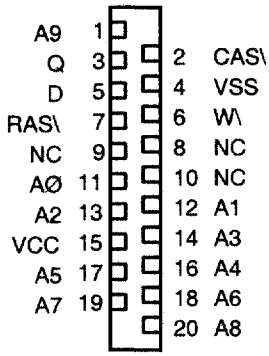
During a WRITE cycle Data-in is latched by the falling edge of W\ or CAS\, which ever occurs last. If W\ goes low prior to CAS\ going LOW, the output pins remain open (HIGH-Z) until the next CAS\ cycle. If W\ goes LOW after data reaches the output pins, Q is activated and retains the selected cell data as CAS\ remains LOW, regardless of W\ or RAS\. This late W\ pulse results in a DELAYED WRITE or READ-WRITE cycle.

The data input and data output use separate pins. FAST PAGE MODE operations allow faster data operations, READ, WRITE or READ-MODIFY-WRITE, within a row address.

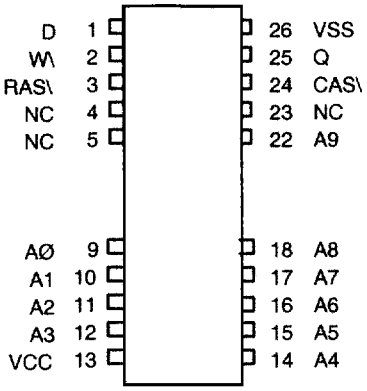
Block Diagram



Pin Configuration



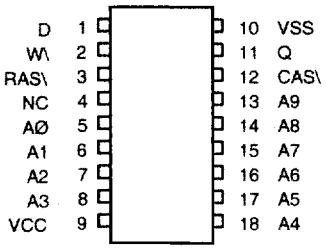
ZIP



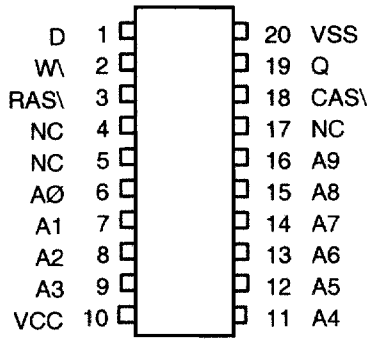
CSOJ

Pin Names

AØ-A9	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



DIP



Flatpack

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-1.0V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0 °C to +70 °C
Industrial	-40 °C to +85 °C
Military	-55 °C to +125 °C
Storage Temperature (Ambient/Ceramic)	-65 °C to +150 °C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	5.5	V
Input Low Voltage	VIL	-1.0	--	0.8	V

Notes: 1. All voltage values are with respect to VSS.

Electrical Characteristics

(VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	Min	Typ	Max	Units
Average Supply Current from VCC	ICC1	RAS\, CAS\ Cycling			80	mA
Operating (Notes 3, 4)		TRC = TWC = Min, Output Open				
Supply Current from VCC	ICC2	RAS\ = CAS\ = VIH, Outputs Open			2	mA
Standby		RAS\ = CAS\ ≥ VCC-0.2, Outputs Open			0.5	mA
Average Supply Current from VCC	ICC3	RAS\ Cycling, CAS\ = VIH			80	mA
Refreshing (Note 3)		TRC = Min, Outputs Open				
Average Supply Current from VCC	ICC4	RAS\ = VIL, CAS\ = Cycling			70	mA
Fast Page Mode (Notes 3, 4)		TPC = Min, Outputs Open				
Average Supply Current from VCC	ICC6	CAS\ before RAS\ Refresh Cycling			80	mA
CAS\ before RAS\ Refresh Mode (Note 3)		TRC = Min Outputs Open				
Input Current	IIL	0V ≤ VIN ≤ VCC	10		10	µA
		VCC = 5.5V, All Other Input Pins = 0V				
Off-State Output Current	IOZ	Q Floating 0V ≤ V OUT ≤ 5.5V	-10		10	µA
Output High Voltage	VOH	IOH = -5mA	2.4	—	VCC	V
Output Low Voltage	VOL	IOL= 4.2mA	0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance	CA	VI = VSS			6	pF
Input Capacitance (D)	CD	f = 1MHz			6	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	Vi = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, Vi = 25mVrms			8	pF

Input Conditions for Each Mode

The EDI411024C provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Fast Page Mode, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown

ACT = Active
NAC= Non-active
DNC= Don't care
VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs RAS\	CAS\	W\	D	Row Address	Column Address	Output Q	Refresh
Read*	ACT	ACT	NAC	DNC	APD	APD	VLD	Yes*
Early Write*	ACT	ACT	ACT	VLD	APD	APD	OPN	Yes*
Read-Modify-Write*	ACT	ACT	ACT	VLD	APD	APD	VLD	Yes*
RAS\-only Refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	Yes
Hidden Refresh	ACT	ACT	DNC	DNC	APD	APD	VLD	Yes
CAS\ before RAS\ Refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	Yes
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	No

*Fast Page Mode Identical

Switching Characteristics

(VCC = 5.0V±10%) Note 5,12,13

Parameter	Sym	70ns Min	70ns Max	80ns Min	80ns Max	100ns Min	100ns Max	Units	Notes
Access Time from CAS\	TCAC		20		20		25	ns	6,7
Access Time from RAS\	TRAC		70		80		100	ns	6,8
Column Address Access Time	TCAA		35		40		50	ns	6,9
Access Time from CAS\ Precharge	TCPA		40		45		55	ns	6,10
Output Low Impedance Time from CAS\ low	TCLZ	0		0		0		ns	6
Output Disable Time after CAS\ High	TOFF	0	20	0	20	0	25	ns	11

Notes: 5. An initial pause of 500µs is required after power-up, followed by any 8 RAS\ or RAS\-CAS\ cycles before proper device operation is achieved. Note that RAS\ may be cycled during the initial pause. Any RAS\ or RAS\-CAS\ cycles are required after prolonged periods of RAS\ inactivity before proper device operation.
6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
7. Assume that TRCD(max) ≤ TRAD and TRAD(max) ≥ TRAD.
8. Assume that TRCD ≤ TRCD(max) and TRAD ≤ TRAD(max).
9. Assume that TRCD – TRAD ≤ TCAA(max) and TRCD ≥ TRCD(max).
10. Assume that TCP ≤ TCP(max) and TASC ≥ TASC(max).
11. TOFF(max) defines the time at which the output achieves the high impedance state (IOUT ≤ |±10µA|) and is not reference to VOH(min) or VOL(max).

Timing Requirements
Read, Write, Read-Modify-Write, Refresh and Fast Page Mode Cycle

(VCC = 5.0V±10%) Note 5,12,13

		70ns		80ns		100ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
Refresh Cycle	TREF		8		8		8	ms	
RAS\ Precharge Time	TRP	60		70		80		ns	
RAS\ to CAS\ Delay Time	TRCD	20	50	25	60	25	75	ns	14
Delay CAS\ High to RAS\ Low	TCRP	10		10		10		ns	15
CAS\ Precharge Time (Non Page Mode)	TCPN	30		35		35		ns	16
Column Address Delay from RAS\ Low	TRAD	15	35	20	40	20	50	ns	17
Row Address Set Up Time	TASR	0		0		0		ns	
Column Address Set Up Time	TASC	0	10	0	15	0	20	ns	18
Row Address Hold Time	TRAH	10		15		15		ns	
Column Address Hold Time	TCAH	15		20		20		ns	
Transition Time	TT	3	50	3	50	3	50	ns	19

Notes: 12. The timing requirements are assumed TT = 5ns.
13. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
14. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in notes 6,8.
15. TCRP requirement is applicable for all RAS\-CAS\ cycles.
16. TCPN(min) is specified as TCPN(min) =TRCD(min) +TCRP(min) except for TCP of fast page mode cycle.
17. TRAD(max) is specified as a reference point only. If TRAD ≥TRAD(max), access time is assumed byTCAA for read cycle.
18. TASC(max) is specified as a reference point only of address access time.
19. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(VCC = 5.0V±10%) Note 5,12,13

		70ns		80ns		100ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Time	TRC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		0		ns	20
Read Hold Time after RAS\ High	TRRH	10		10		10		ns	20
Column Address to RAS\ Setup	TRAL	35		40		50		ns	
Precharge to CAS\ Active	TRPC	0		0		0		ns	

Notes: 20. Either TRCH or TRRH must be satisfied for a read cycle.

Write Cycle

(VCC = 5.0V±10%) Notes 5, 12, 13

		70ns		80ns		100ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	TWC	140		160		190		ns	
RAS\ Low Pulse Width	TRAS	70	10,000	80	10,000	100	10,000	ns	
CAS\ Low Pulse Width	TCAS	20	10,000	20	10,000	25	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		0		ns	23
Write Hold Time after CAS\ Low	TWCH	15		15		20		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after CAS\ Low	TDH	15		15		20		ns	

Read-Write & Read-Modify-Write Cycles

(VCC = 5.0V±10%) Notes 5, 12, 13

		70ns		80ns		100ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-Write Cycle Time	TRWC	165		185		220		ns	21
Read-Modify-Write Cycle Time	TRMWC	165		185		220		ns	22
RAS\ Low Pulse Width	TRASRW	95	10,000	105	10,000	130	10,000	ns	
CAS\ Low Pulse Width	TCASRW	45	10,000	45	10,000	55	10,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	95		105		130		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	45		45		55		ns	
Read Setup time before CAS\ Low	TRCS	0		0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	20		20		25		ns	23
RAS\ Low to W\ Low Delay	TRWD	70		80		100		ns	23
CAS\ Hold after W\ Low	TCWL	20		20		25		ns	
RAS\ Hold after W\ Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after W\ Low	TDH	15		15		20		ns	
Address to W\ Low Delay	TAWD	35		40		50		ns	23

Notes: 21. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +4TT.

22. TRMWC is specified as TRMWC(min)=TRAC(max)+TRWL(min)+TRP(min)+4TT.

23. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only. When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD ≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Fast Page Mode Cycle
Read, Early Write, Read-Write, Read-Modify-Write Cycle

(VCC = 5.0V±10%) Notes 5,12,13

		70ns		80ns		100ns		
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Fast Page Mode Cycle Time	TPC	45		50		60		ns
Fast Page Mode for R/W, R/M/W Cycle Time	TRWPC	70		75		90		ns
RAS\ Low Pulse Width for Read, Write Cycle	TRAS	115	100,000	130	100,000	160	100,000	ns
CAS\ Low Pulse Width for Read Cycle	TCAS	20	100,000	20	100,000	25	100,000	ns
CAS\ Pulse Width (Page Mode)	TCP	10		10		10		ns
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns

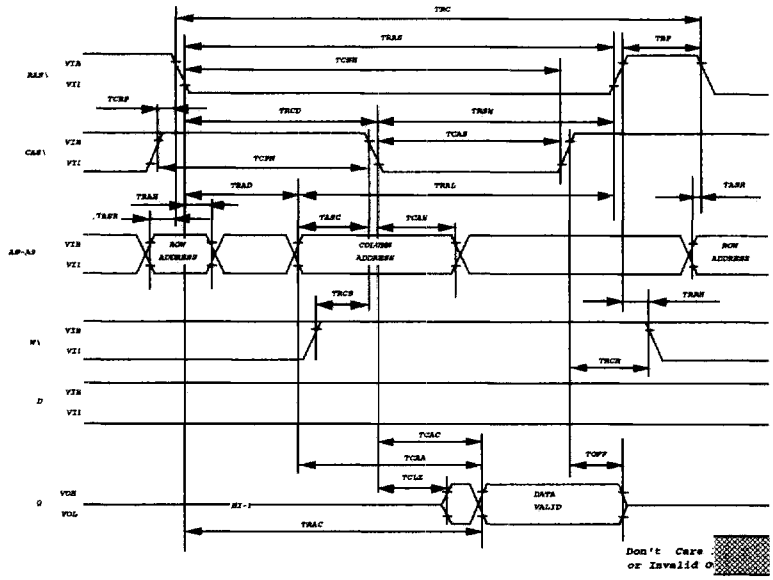
CAS\ before RAS\ Refresh Cycle

(VCC = 5.0V±10%) Notes 5,12,13

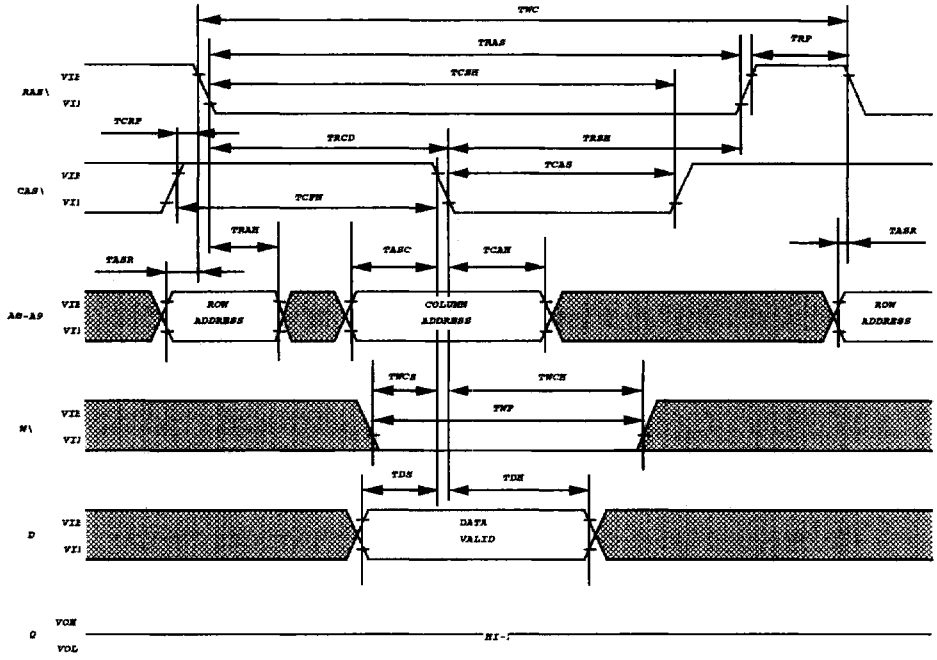
		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	10		10		10		ns	24
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	15		15		20		ns	24
Precharge to CAS\ Active	TRPC	0		0		0		ns	24

Note: 24. Eight or more CAS\ before RAS\ cycles are necessary for proper operation of CAS\ before RAS\ refresh mode.

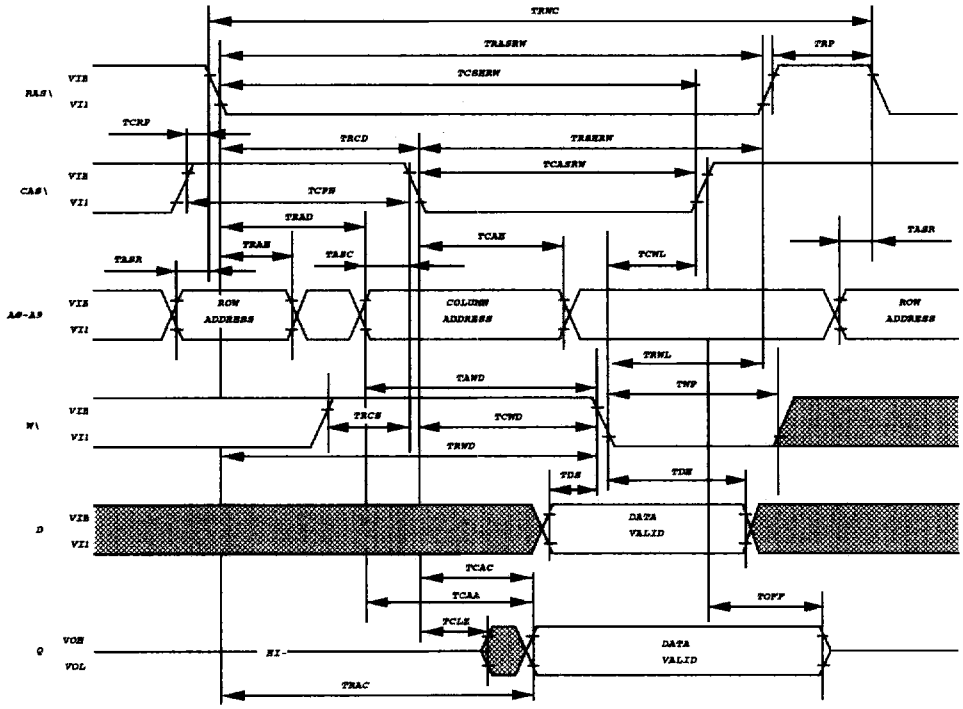
Read Cycle



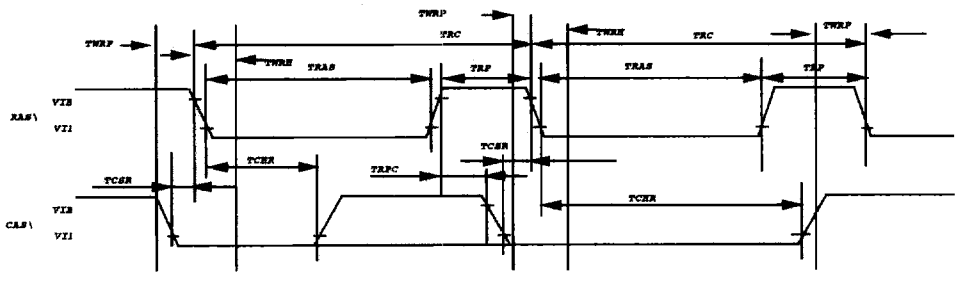
Write Cycle, Early Write



Read-Write, Read-Modify-Write Cycle

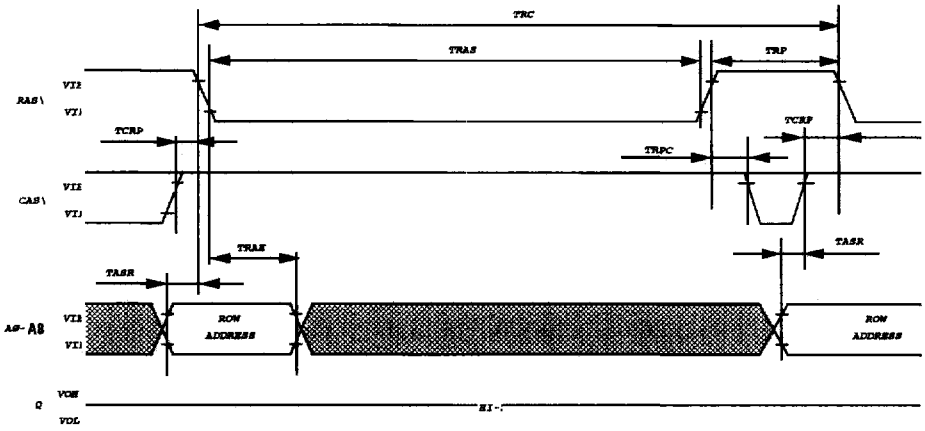


CAS\ before RAS\ Refresh Cycle (Note 25)



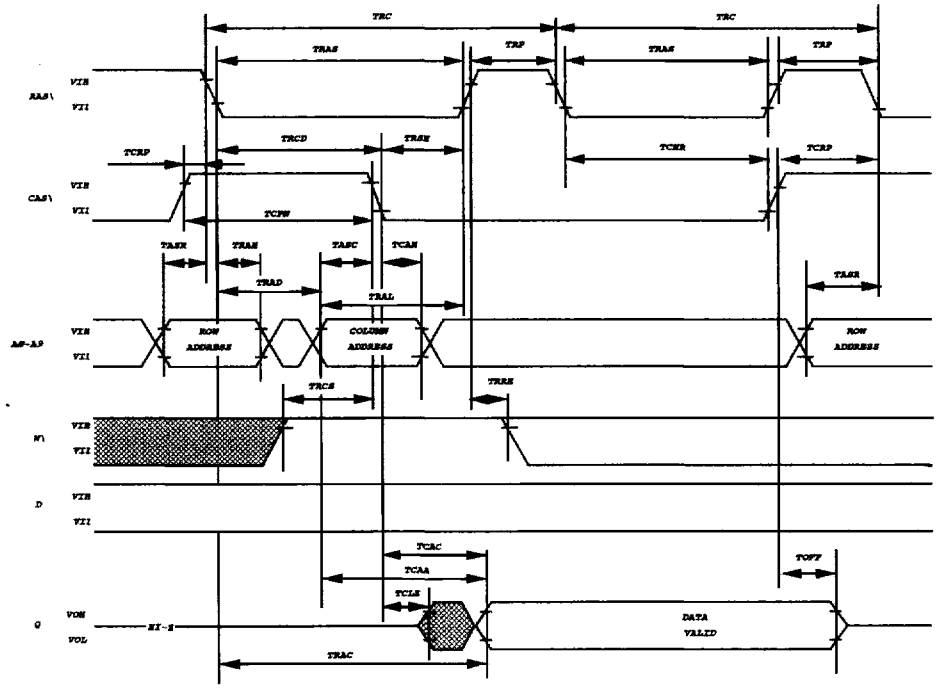
Note: 25. W\ Don't Care.

RAS-only Refresh Cycle (Note 26)

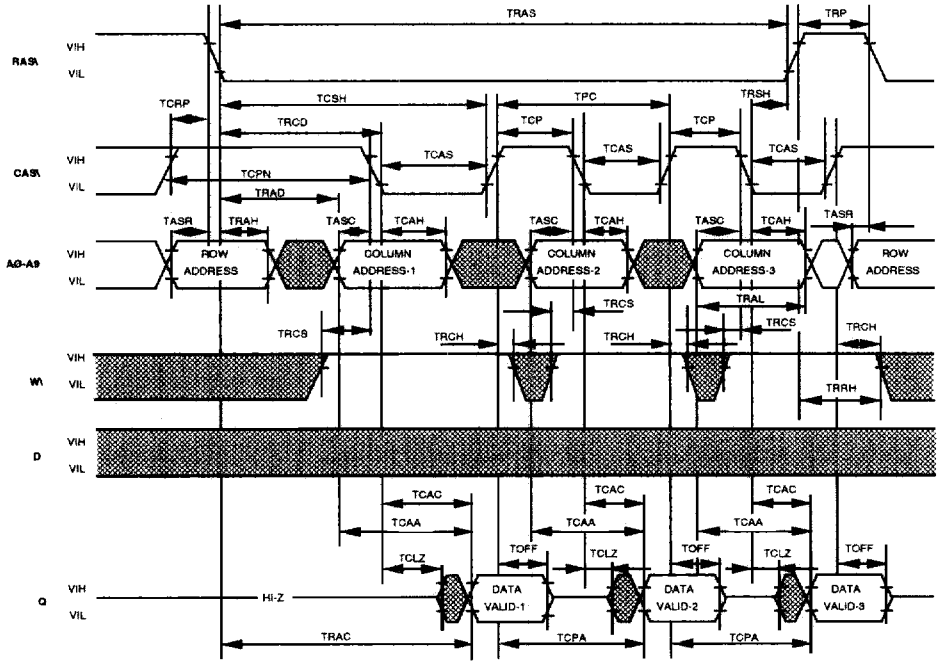


Note: 26 W\, D=Don't Care; A9=VIH or VIL

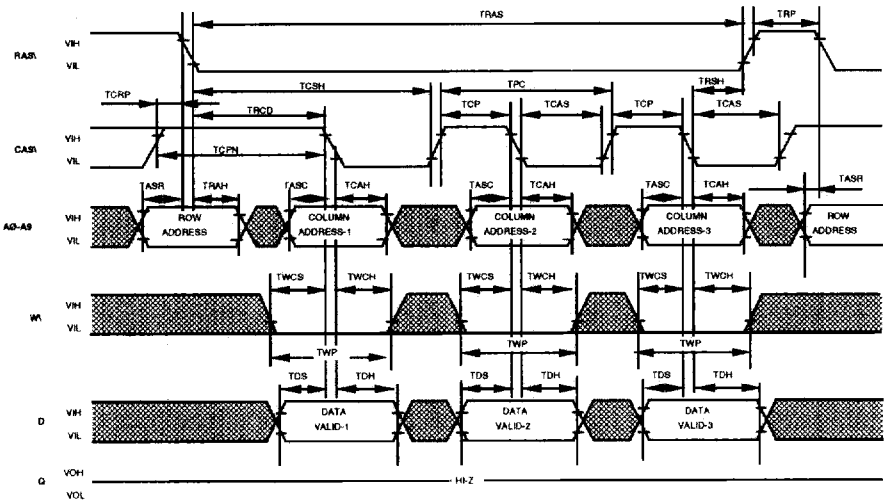
Hidden Refresh Cycle



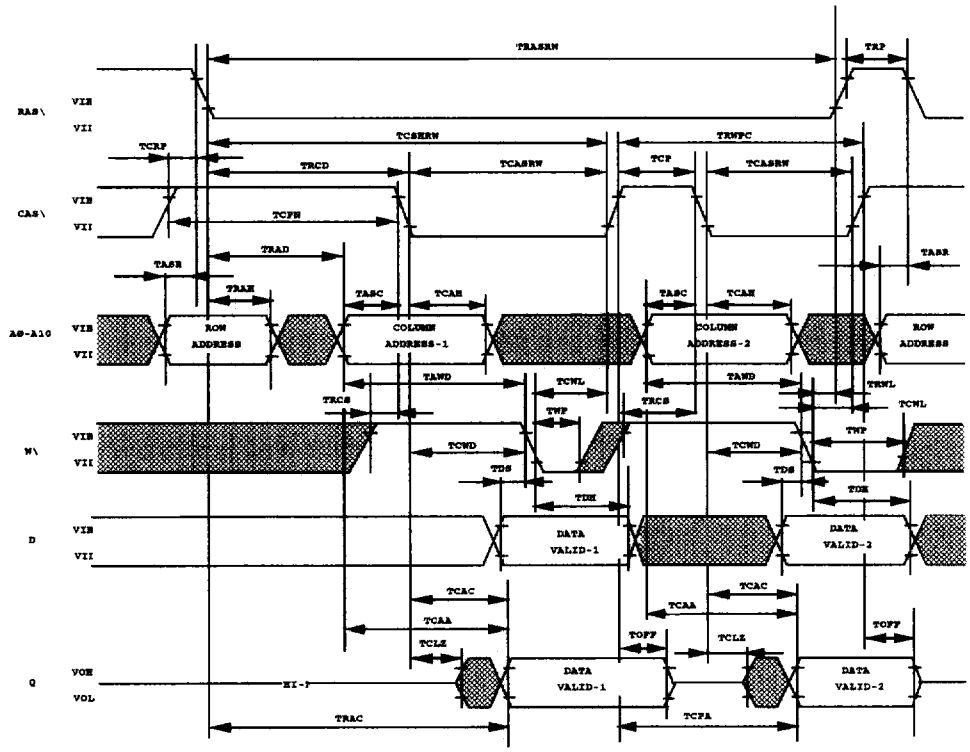
Fast-Page-Mode, Read Cycle



Fast-Page-Mode, Early Write Cycle



Fast-Page-Mode, Read-Write, Read-Modify-Write Cycle



Ordering Information

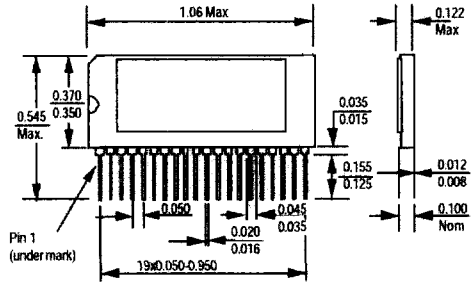
Part No.	Speed ns	Package No.
EDI411024C70ZB	70	18
EDI411024C80ZB	80	18
EDI411024C100ZB	100	18
EDI411024C70QB	70	1
EDI411024C80QB	80	1
EDI411024C100QB	100	1

Part No.	Speed ns	Package No.
EDI411024C70NB	70	16
EDI411024C80NB	80	16
EDI411024C100NB	100	16
EDI411024C70FB	70	78
EDI411024C80FB	80	78
EDI411024C100FB	100	78

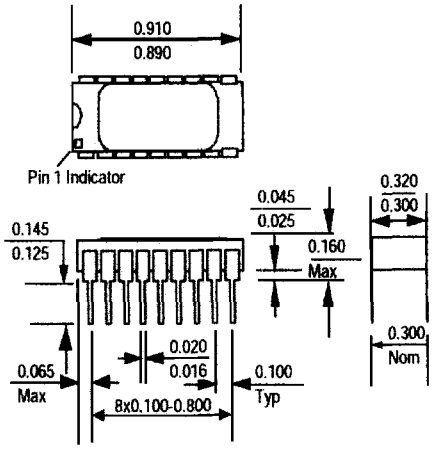
Notes: For Commercial, Industrial or Mil-Temp-Only grade products use C,I or M respectively to replace B in the suffix of the part number, eg. EDI411024C70ZB (Military) becomes EDI411024C70ZI (Industrial Temp Range).

Package Description

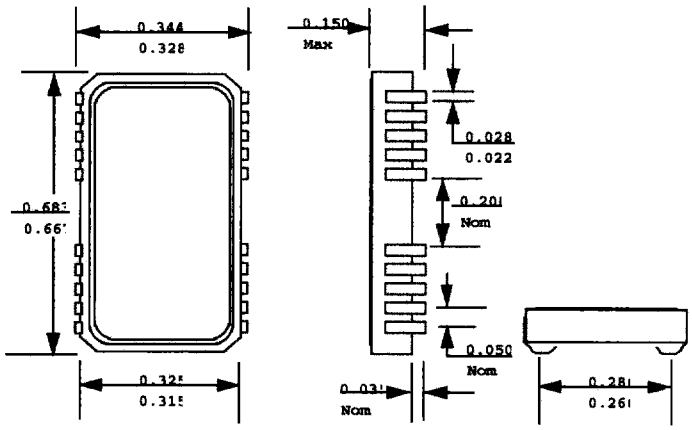
Package No. 18
20 Pin Ceramic Zip



Package No. 1
18 Pin DIP



Package No. 16
20 Lead CSOJ



Package No. 78
20 Lead Flatpack