OKI Semiconductor

MSM5416256/MSM54V16256

(Standard-version) (Low voltage version or V-version)

262,144 Words x 16 Bits GRAPHICS BURST ACCESS MEMORY

GENERAL DESCRIPTION

The MSM5416256 is a high speed 256KX16 configuration burst access memory for high performance graphics applications. In addition to the burst mode, the MSM54(V)16256 has conventional DRAM mode which is selectable by a timing setting when RAS falls. The MSM5416256 has conventional two CAS type 256KX16 DRAM compatible pinout .

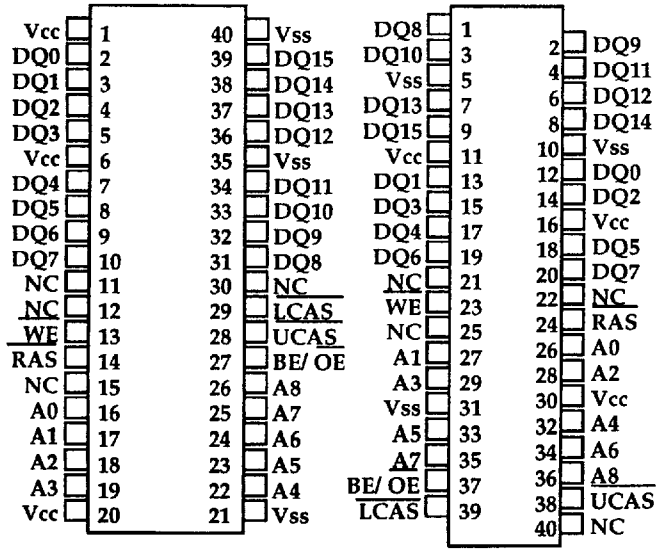
FEATURES

- Selectable function mode; Burst mode and DRAM mode
- Hyper page mode
- Byte wide control: 2 CAS control
- Write-per-bit (not persistent write-per-bit)
- 262,144 words by 16 bits organization
- Pin compatible with 2 CAS type 256KX16 DRAM
- Single +5V Supply, ±10% tolerance (Standard- version)
  Single +3.3V Supply, ±10% tolerance (V- version)
- Output : CMOS compatible, Non-TTL, 50pF load
- CAS before RAS, Hidden, RAS only refresh capability (Standard- version)
  CAS before RAS self-refresh (V- version)
- Refresh: 512 cycles/8ms (Standard- version)

FAMILY ORGANIZATION (TARGET SPEC)

Family	Access Time (Max.)			Cycle Time (Min.)			Power Dissipation
	t_{RAC}	t_{AA}	t_{BAC}	t_{RC}	t_{HPC}	t_{BPC}	
MSM5416256-10	45ns	20ns	10ns	90ns	22ns	10ns	1000mW
MSM5416256-12	47ns	22ns	12ns	100ns	24ns	12ns	900mW
MSM5416256-15	50ns	25ns	15ns	110ns	27ns	15ns	800mW
MSM5416256-20	60ns	30ns	20ns	120ns	32ns	20ns	700mW

PIN CONFIGURATION (TOP VIEW)

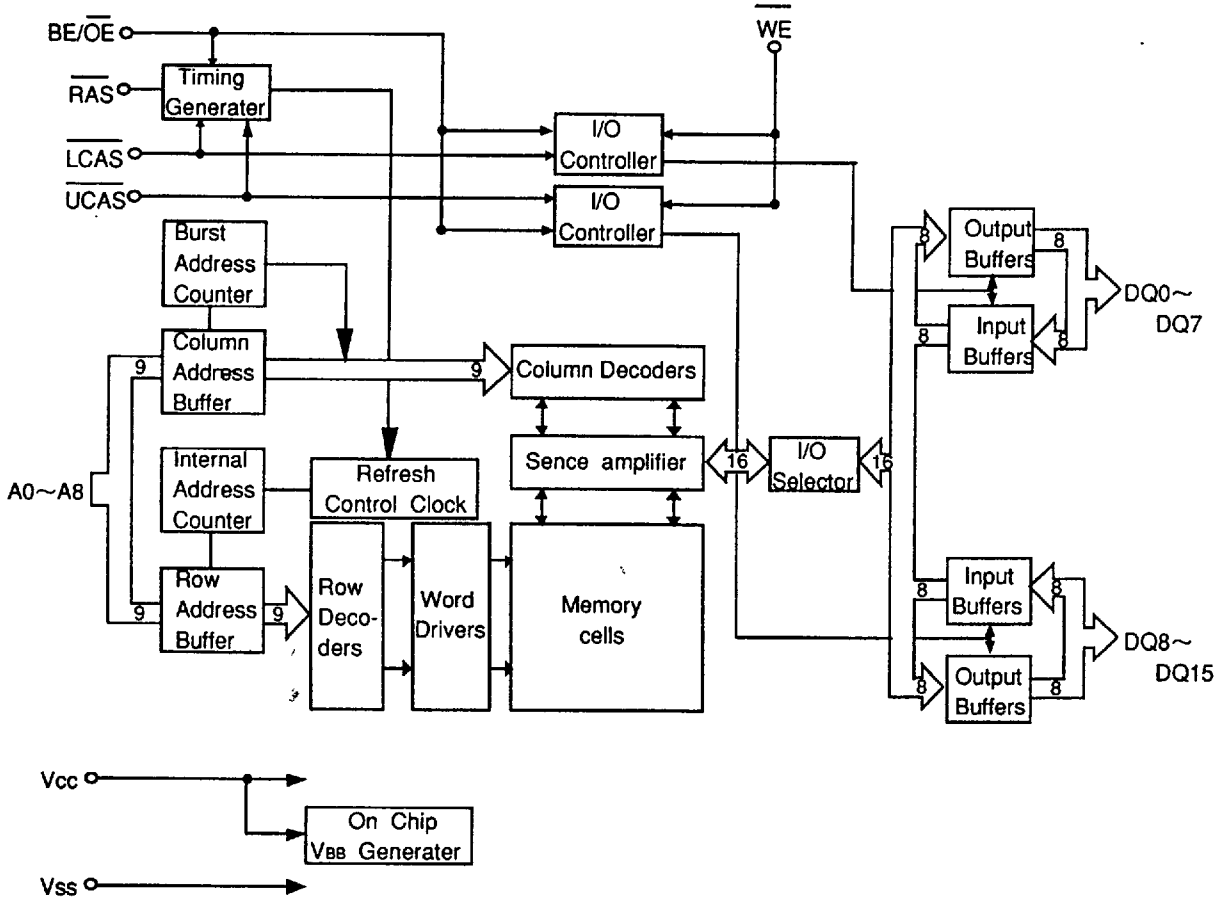


40Pin 400mil SOJ

40Pin 475mil ZIP

Pin Names	Function
A0-A8	Address Input
RAS	Row Address Strobe
LCAS,UCAS	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
WE	Write Enable
BE/ OE	Burst Enable/ Output Enable
VCC	(Standard-version) Power Supply (+5V)
VCC	(V-version) Power Supply (+3.3V)
VSS	Ground (0V)
NC	No Connection

FUNCTION BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functinal Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{UWE}$	BE/$\overline{OE}$	DQ0~DQ7	DQ8~DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	DOUT	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	DOUT	Upper Byte Read
L	L	L	H	L	DOUT	DOUT	Word Read
L	L	H	L	H	DIN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DIN	Upper Byte Write
L	L	L	L	H	DIN	DIN	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25℃	-1.0～+7.0	V
Short circuit output current	Ios	Ta=25℃	50	mA
Power dissipation	Po	Ta=25℃	1	W
Operrating temperrature	Topr	—	0～+70	℃
Storage temperature	Tstg	—	-55～+150	℃

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	4.5	5.0	5.5	V
	Vss	—	0	0	0	V
Input high voltage	V_{IH}	—	2.4	—	6.5	V
Input low voltage	V_{IL}	—	-1.0	—	0.8	V

Capacitance

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0～A8)	C_{IN1}	—	—	7	pf
Input capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{LWE}$,$\overline{UWE}$,$\overline{OE}$)	C_{IN2}	—	—	7	pf
Input capacitance (DQ0～DQ15)	$C_{I/O}$	—	—	10	pf

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0 to 70°C)

Parameter	Symbol	Condition	MSM5416256 -10		MSM5416256 -12		MSM5416256 -15		MSM5416256 -20		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL}= 2.0mA	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V≦V_I≦6.5V; All other pins not under test=0V	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQi Disable 0V≦V_o≦5.5V	-10	10	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling t_{RC}=Min.	—	200	—	200	—	180	—	180	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	—	3	—	3	—	3	—	3	mA	1
		$\overline{RAS}$,$\overline{CAS}$ ≧ V_{CC} − 0.2V	—	1	—	1	—	1	—	1		
Average Power Supply Current ($\overline{RAS}$ only Refresh)	I_{CC3}	$\overline{RAS}$=Cycling $\overline{CAS}$=V_{IH} t_{RC}=Min.	—	200	—	200	—	180	—	180	mA	1,2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IL} Dout=Enable	—	5	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$=Cycling $\overline{CAS}$ Befor $\overline{RAS}$	—	200	—	200	—	180	—	180	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$=V_{IL} $\overline{CAS}$ Cycling t_{PC}=Min.	—	170	—	170	—	150	—	150	mA	1,3
Average Power Supply Current ($\overline{CAS}$ Befor $\overline{RAS}$ Self-Refresh)	I_{CC8}	$\overline{RAS}$≦0.2V $\overline{CAS}$≦0.2V	—	500	—	500	—	500	—	500	μA	1

Notes: 1. Specified valuues are obtained with output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

AC CHARACTERISTICS (1/2)

(Vcc = 5V ± 10%, Ta = 0~70°C)

Parameter	Symbol	MSM5416256 -10		MSM5416256 -12		MSM5416256 -15		MSM5416256 -20		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	90	—	100	—	110	—	120	—	ns	
Read/Write cycle time	t_{RMW}	140	—	140	—	150	—	160	—	ns	
Hyper page mode cycle time	t_{HPC}	22	—	24	—	27	—	32	—	ns	
Fast page mode read/write cycle time	t_{PRWC}	71	—	73	—	75	—	80	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	45	—	47	—	50	—	60	ns	
Access time from $\overline{CAS}$	t_{CAC}	—	13	—	14	—	15	—	15	ns	
Access time from column address	t_{AA}	—	20	—	22	—	25	—	30	ns	
Access time from $\overline{OE}$	t_{OEA}	—	13	—	14	—	15	—	15	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	27	—	28	—	30	—	34	ns	
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Data hold after $\overline{CAS}$ low	t_{COH}	5	—	5	—	5	—	5	—	ns	
Output buffer turn-off delay time	t_{OFF}	0	10	0	10	0	10	0	10	ns	
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	0	10	0	10	0	10	0	10	ns	
Transition time	t_T	1	50	1	50	1	50	1	50	ns	
Refresh preiod	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{RAS}$ precharge time	t_{RP}	35	—	40	—	50	—	50	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	45	10,000	50	10,000	50	10,000	60	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	45	100,000	50	100,000	50	100,000	60	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13	—	13	—	14	—	15	—	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10,000	14	10,000	15	10,000	15	10,000	ns	
$\overline{CAS}$ pulse width (BURST READ)	t_{CAS}	30	10,000	30	10,000	30	10,000	30	10,000		
$\overline{CAS}$ hold time	t_{CSH}	45	—	48	—	50	—	60	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	31	17	31	18	36	20	45	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	12	21	12	21	13	24	15	30	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	7	—	8	—	10	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	12	—	12	—	13	—	15	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	35	—	35	—	40	—	50	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	24	—	24	—	26	—	30	—	ns	
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	

AC CHARACTERISTICS (2/2)

(Vcc = 5V ± 10%, Ta = 0~70°C)

Parameter	Symbol	MSM5416256 -10		MSM5416256 -12		MSM5416256 -15		MSM5416256 -20		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	10	—	11	—	12	—	15	—	ns	
Write command pulse width	t_{WP}	8	—	8	—	10	—	10	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	35	—	35	—	40	—	50	—	ns	
$\overline{OE}$ command hold time	t_{OEH}	12	—	12	—	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	14	—	14	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	14	—	14	—	15	—	ns	
Data to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Data to BE/$\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	9	—	9	—	10	—	10	—	ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	35	—	35	—	40	—	50	—	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	12	—	12	—	13	—	15	—	ns	
Write-per-bit mask data hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
Write-per-bit mask data set-up time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Write-per-bit set-up time	t_{WSR}	0	—	0	—	0	—	0	—	ns	
Write-per-bit hold time	t_{RWH}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	—	35	—	35	—	35	—	ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	48	—	50	—	52	—	56	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	—	73	—	75	—	80	—	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	0	—	0	—	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ befor $\overline{RAS}$ self-refresh)	t_{RASS}	100	—	100	—	100	—	100	—	ns	
$\overline{RAS}$ precharge time ($\overline{CAS}$ befor $\overline{RAS}$ self-refresh)	t_{RPS}	100	—	100	—	100	—	100	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ befor $\overline{RAS}$ self-refresh)	t_{CHS}	-50	—	-50	—	-50	—	-50	—	ns	
Burst access time from $\overline{CAS}$	t_{BAC}	—	10	—	12	—	15	—	20	ns	
$\overline{CAS}$ pulse width (Burst mode)	t_{BCAS}	4	—	5	—	6	—	8	—	ns	
$\overline{CAS}$ precharge time (Burst mode)	t_{BCP}	4	—	5	—	6	—	8	—	ns	
Output buffer turn-off delay (Burst mode)	t_{BOFF}	0	10	0	10	0	10	0	10	ns	
BE/$\overline{OE}$ high set-up time	t_{BES}	0	—	0	—	0	—	0	—	ns	
BE/$\overline{OE}$ high hold time	t_{BEH}	10	—	10	—	10	—	10	—	ns	
Burst mode cycle time	t_{BPC}	10	—	12	—	15	—	20	—	ns	
Data set-up time (Burst mode)	t_{BDS}	0	—	0	—	0	—	0	—	ns	
Data hold time (Burst mode)	t_{BDH}	5	—	6	—	7	—	8	—	ns	

Notes:

1. An initial psuse of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example; $\overline{RAS}$ only refresh) before proper device operation is achieved.

2. Same V_{CC}-voltage level must be applied to all V_{CC}-pins. And same V_{SS}-voltage level must be applied to all V_{SS}-pins too.

3. The AC chracteristics assume at t_T=2ns.

4. Transition times (t_T) are measured between V_{IH} and V_{IL}.

5. Measured with a load circuit equivalent to 1 TTL loads and 50pF.

6. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only; if t_{RAD} is greater then the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.

7. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only; if t_{RAD} is greater then the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.

8. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

9. Either t_{RRH} and t_{RCH} must be satisfied for a read cycle.

10. t_{WCS},t_{CWD},t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and tee data out will remain open circit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min.) , $t_{RWD} \geqq t_{RWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is read/write cycle and data out will contains is satisfied, the condition of the data out (at access time) is indeterminate.

11. These parameters are refereced to $\overline{CAS}$ leadding edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read-modify cycle.

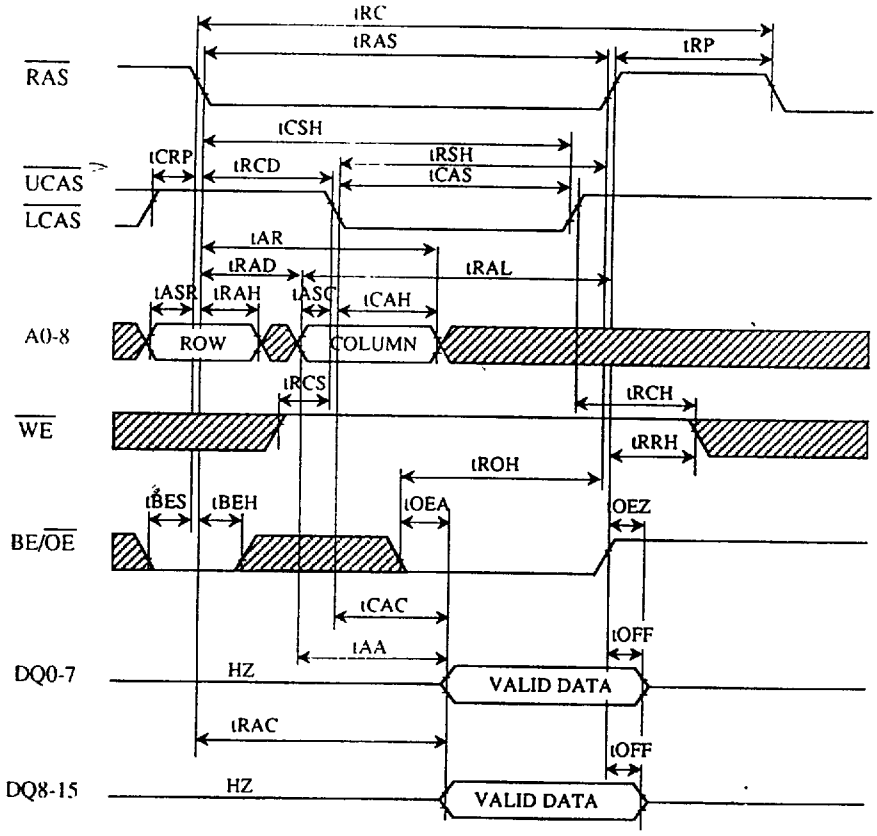
12. t_{ASC}, t_{CHR}, t_{RCS}, t_{RCH}, t_{WCS}, t_{DS}, t_{DH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.

13. t_{CRP}, t_{CHR} and t_{CPA} determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.

14. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.

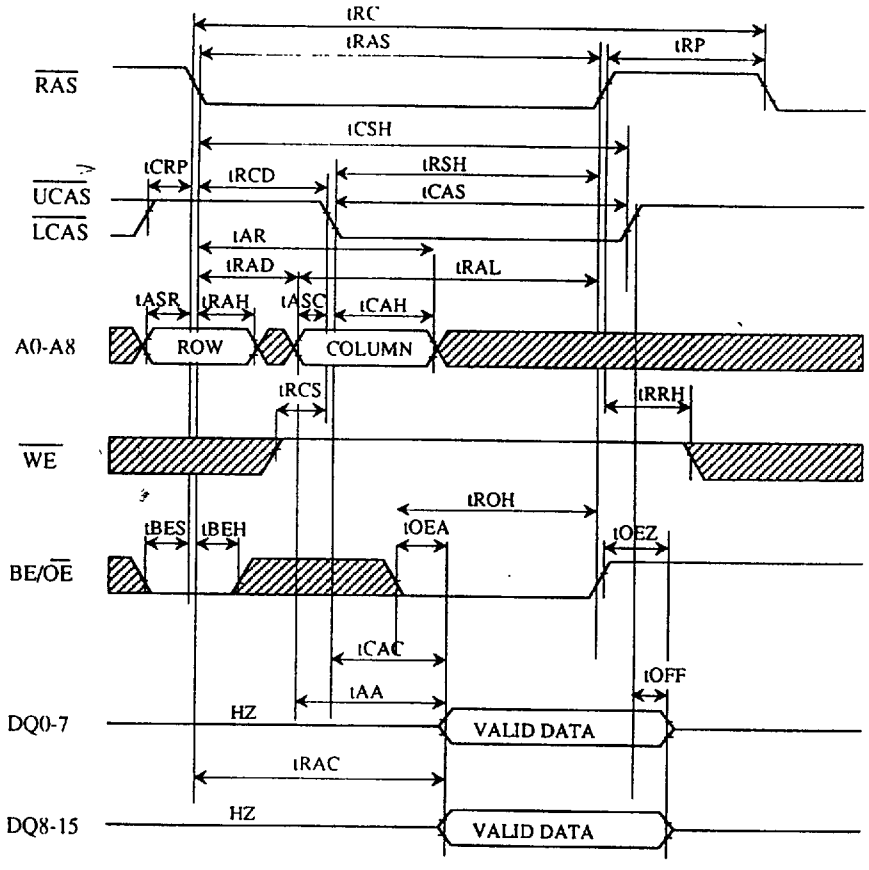
15. t_{CPN}, t_{CP} and t_{CPT} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.

READ CYCLE ($\overline{RAS}$ output control)



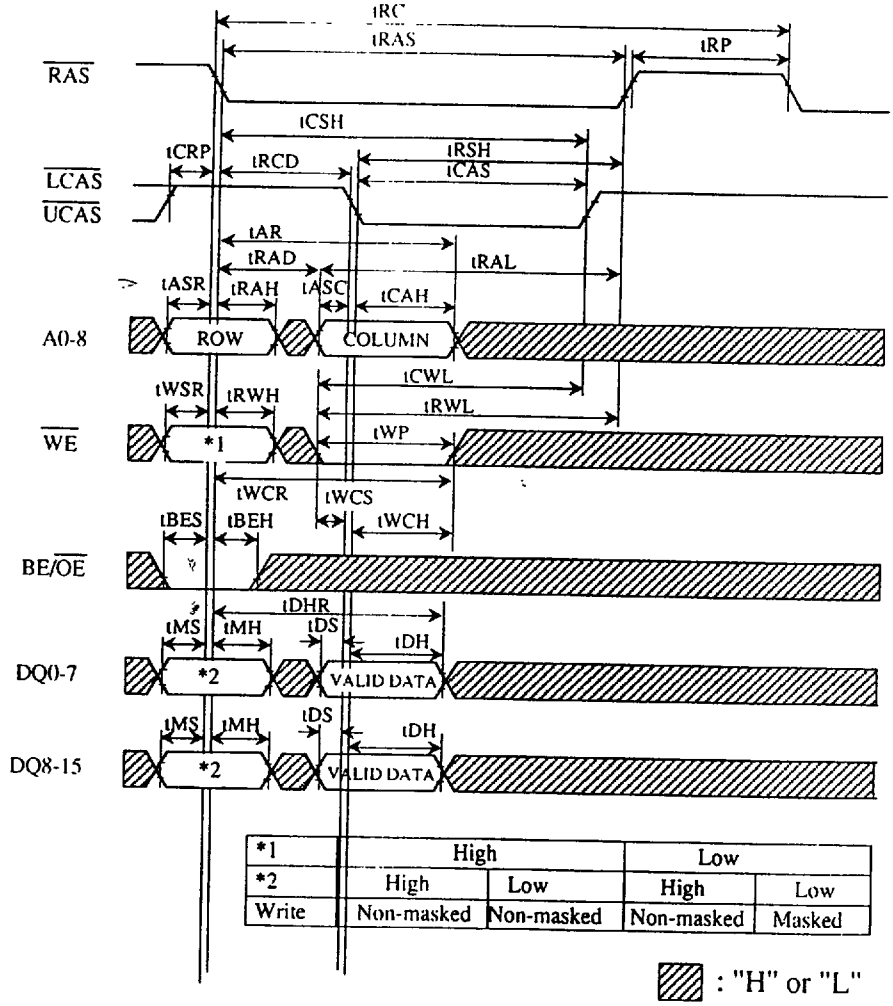
▨ : "H" or "L"

READ CYCLE ($\overline{CAS}$ output control)



▨ : "H" or "L"

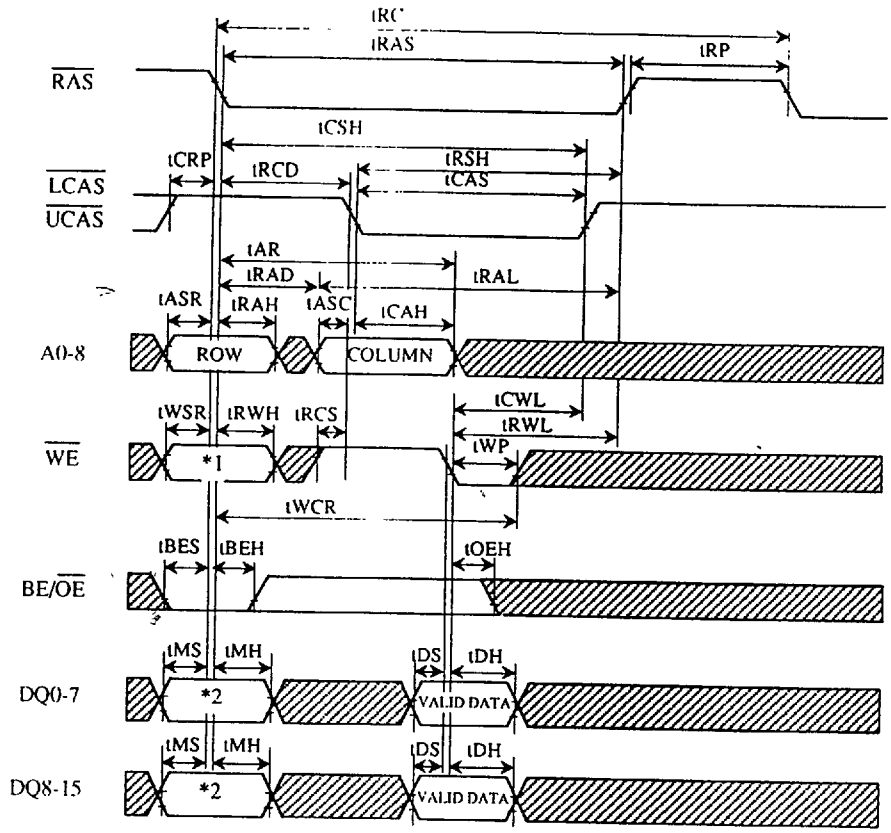
EARLY WRITE CYCLE - $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active -



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

▨ : "H" or "L"

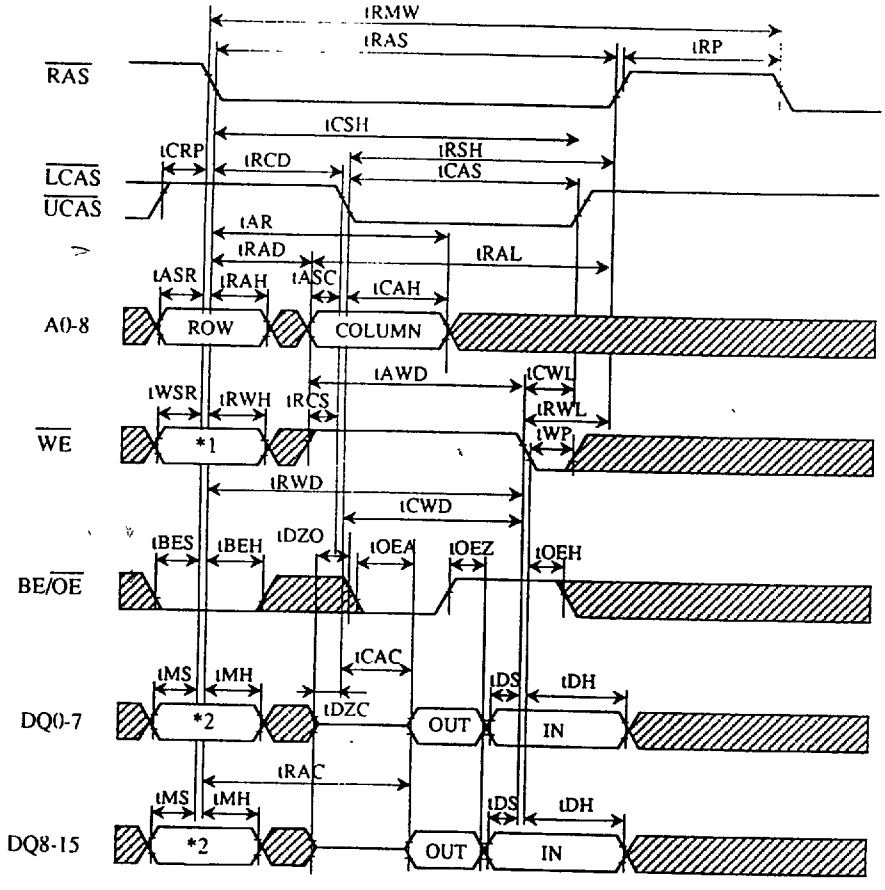
LATE WRITE CYCLE - $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active -



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

: "H" or "L"

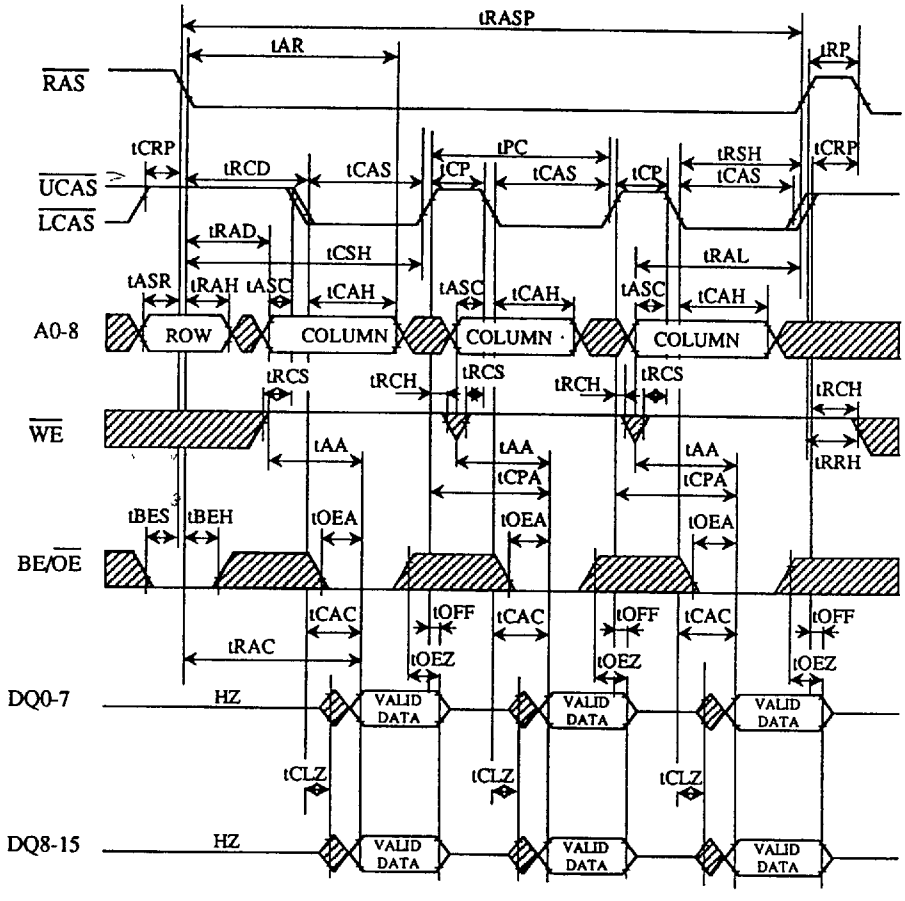
READ MODIFY WRITE CYCLE - $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active -



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

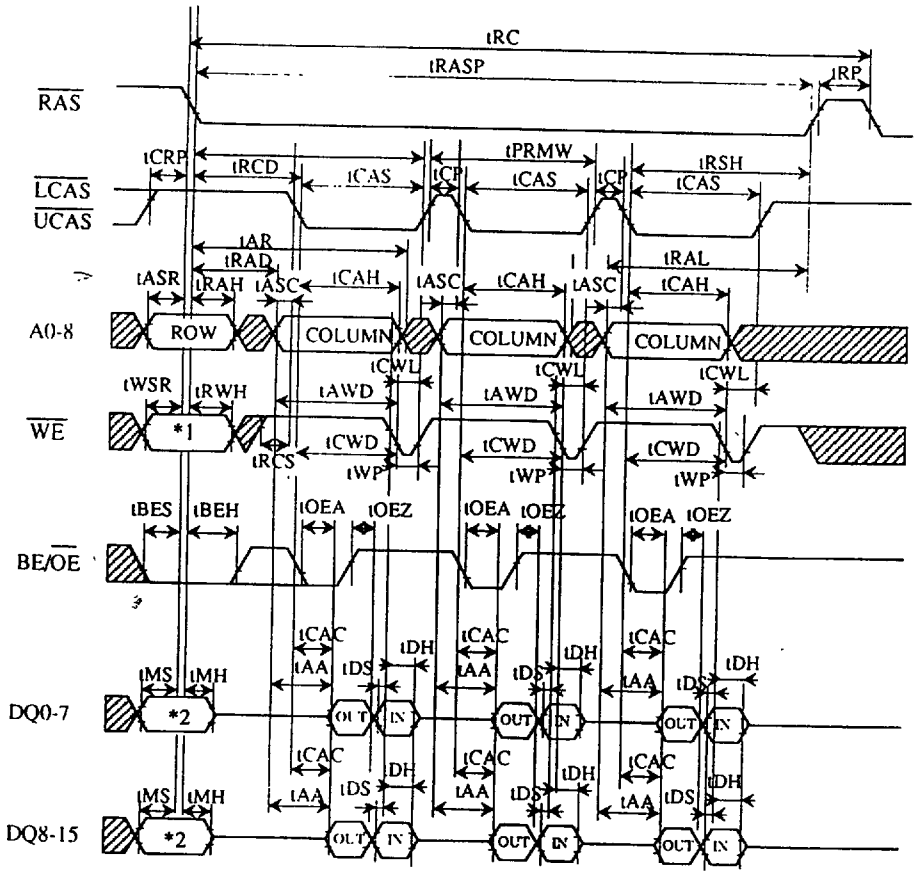
▨ : "H" or "L"

FAST PAGE MODE READ CYCLE



▨ : "H" or "L"

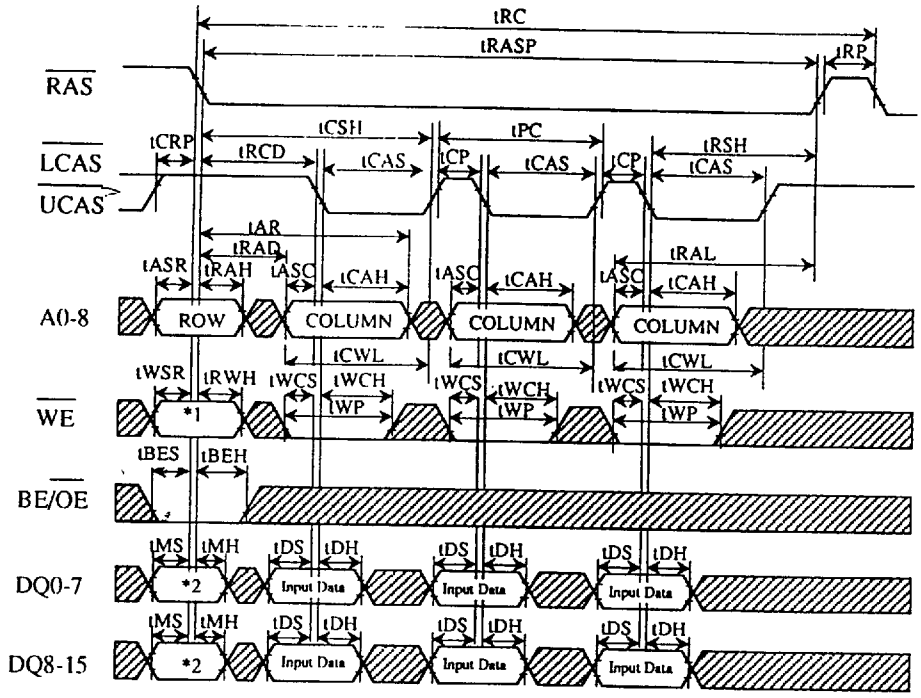
FAST PAGE MODE READ MODIFY WRITE CYCLE



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

▨ : "H" or "L"

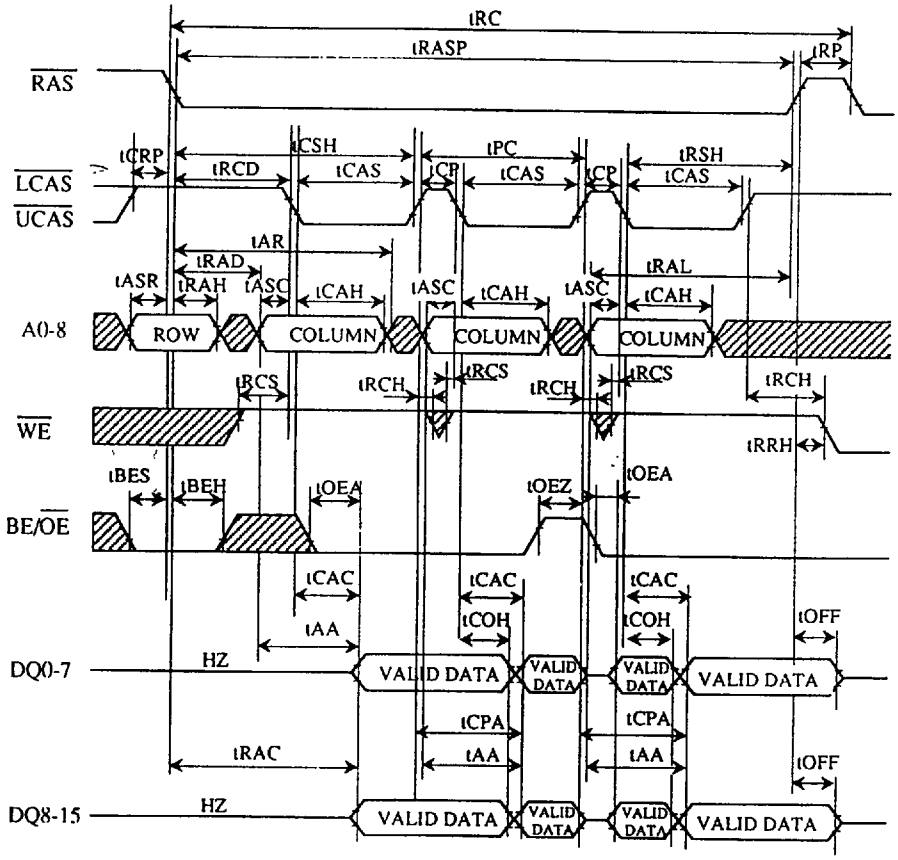
FAST PAGE MODE EARLY WRITE CYCLE



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

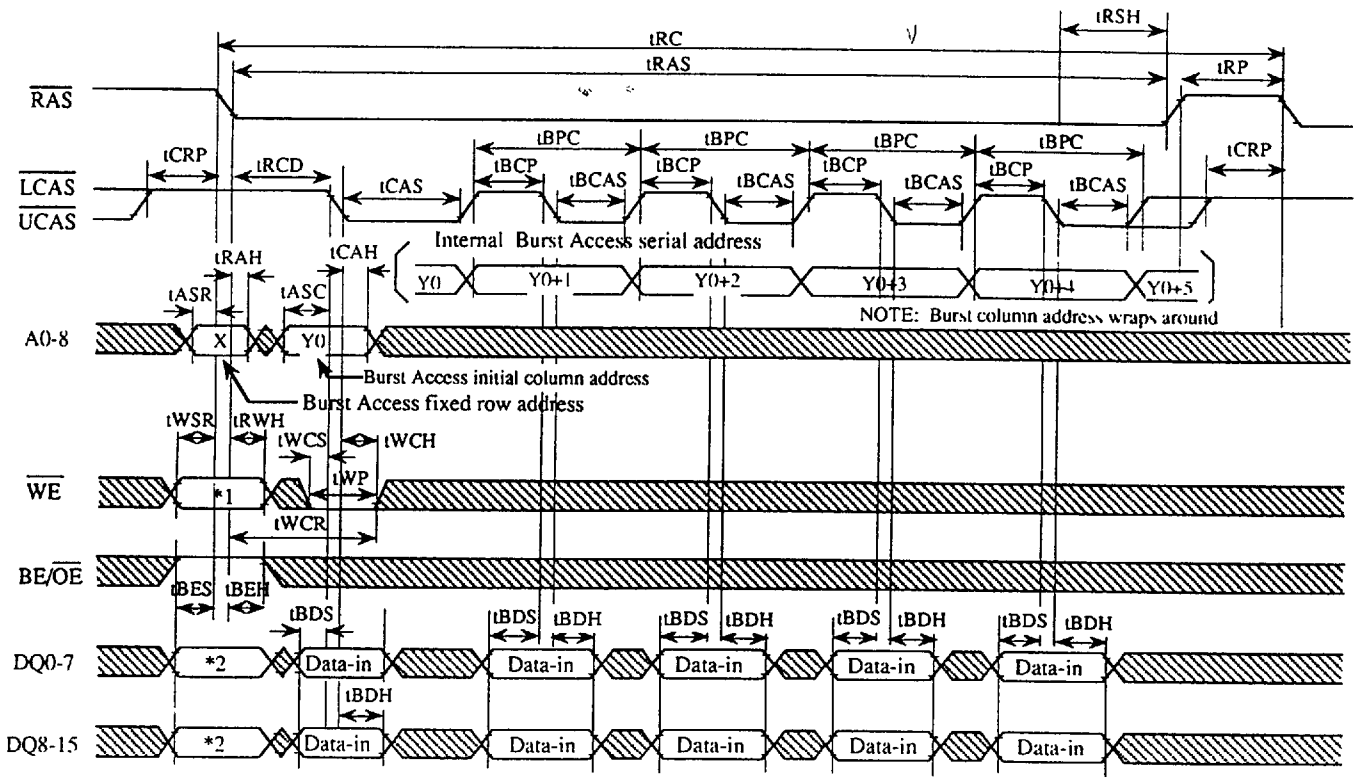
: "H" or "L"

EXTENDED PAGE MODE READ CYCLE



: "H" or "L"

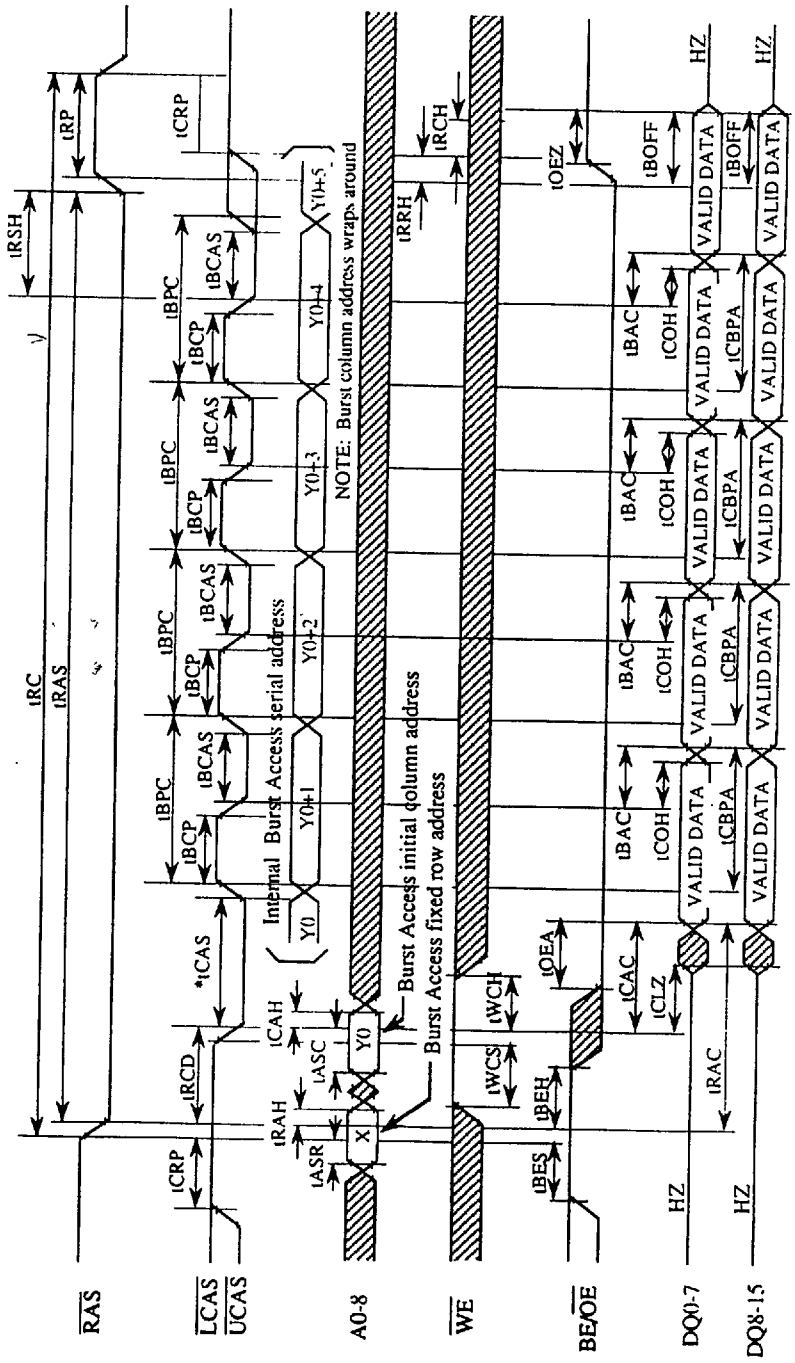
BURST MODE WRITE CYCLE - $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active -



*1	High		Low	
*2	High	Low	High	Low
Write	Non-masked	Non-masked	Non-masked	Masked

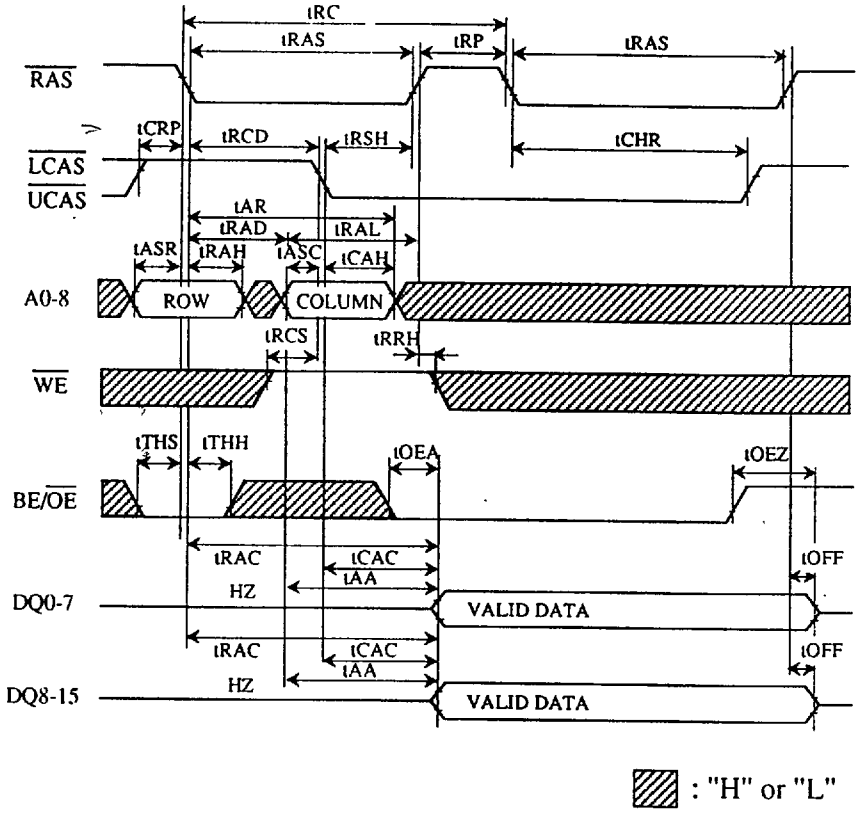
▨ : "H" or "L"

BURST MODE READ CYCLE



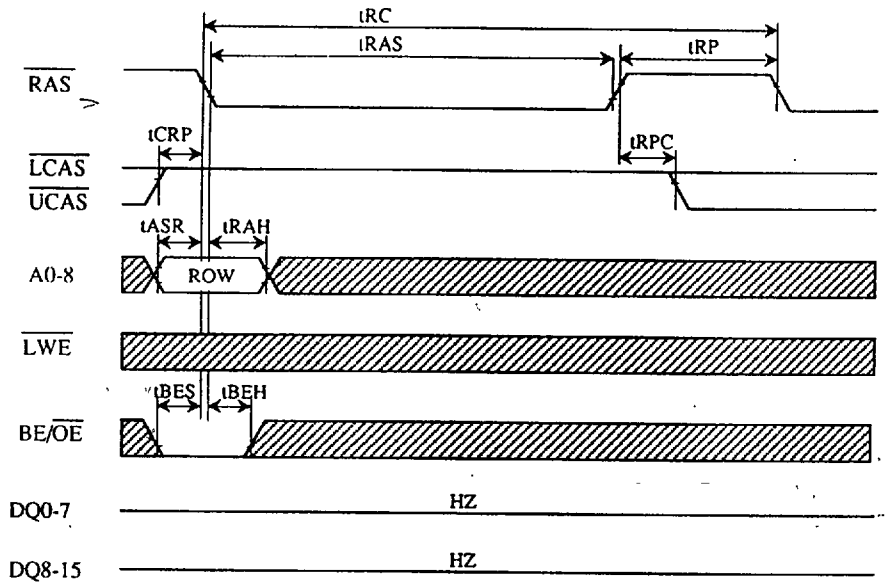
*tCAS = 30ns (Min) at BURST READ TIMING

HIDDEN REFRESH CYCLE



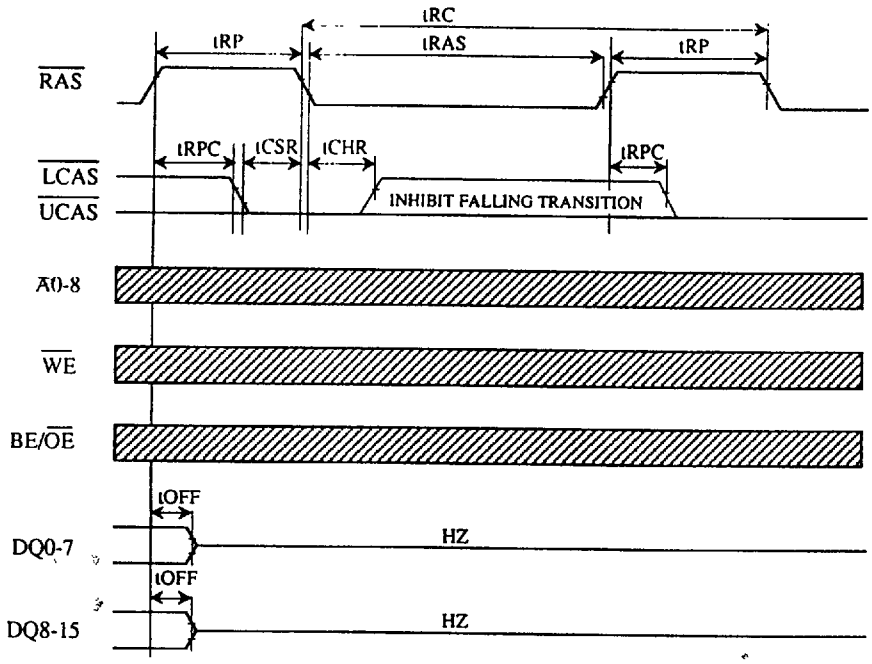
: "H" or "L"

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



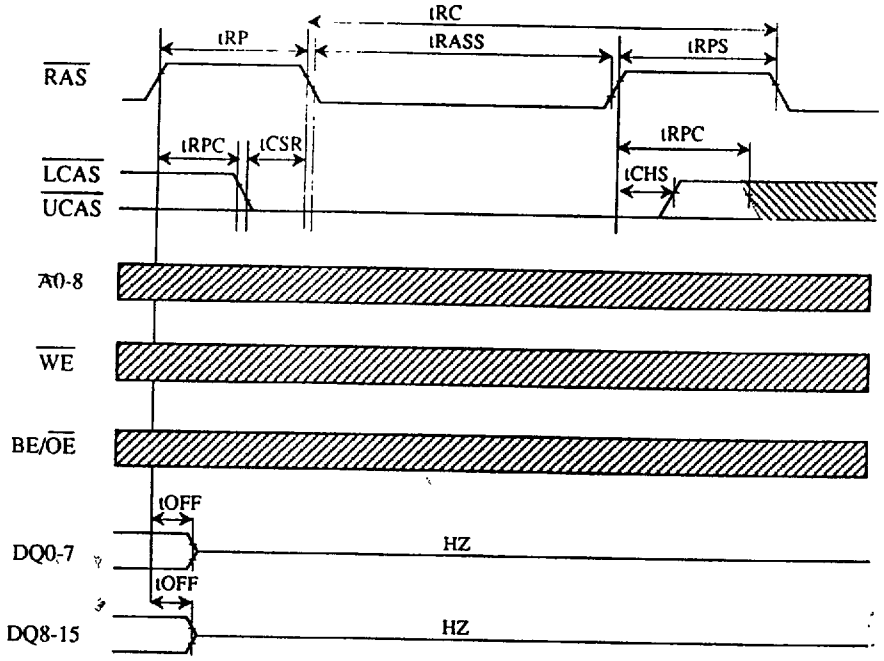
: "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



▨ : "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ SELFREFRESH CYCLE



▨ : "H" or "L"