HI-8000 Features

REAL TIME LOW-POWER μ PROCESSOR COMPATIBLE CLOCK/TIMER/ALARM/ CALENDARS/STOPWATCH/ EVENT COUNTER

- Multiplex address/data bus for easy interface to MC146805, MC6801, 8085 and 8086
- Counts seconds, minutes, hours, day of week, date, months and years
- Max count is 128 years with 15.3 μs resolution
- On chip oscillator
- May be used with any processor having separate address and data busses such as the 8080, 6802, etc.
- 3 microprocessor clock drivers
- 1 Hz output
- Low power battery standby
- 16 bit clock independent timer counter with on chip oscillator, interrupt and square wave output
- 12/24 hour mode
- Leap year compensation
- Programmable prescaler to 1 Hz (21 bits)
- Stopwatch and elapse timer with external trigger
- Sophisticated alarm interrupt
- Software sync. of clock
- Leap year is year Ø

ORIG

S-198 KES

002702

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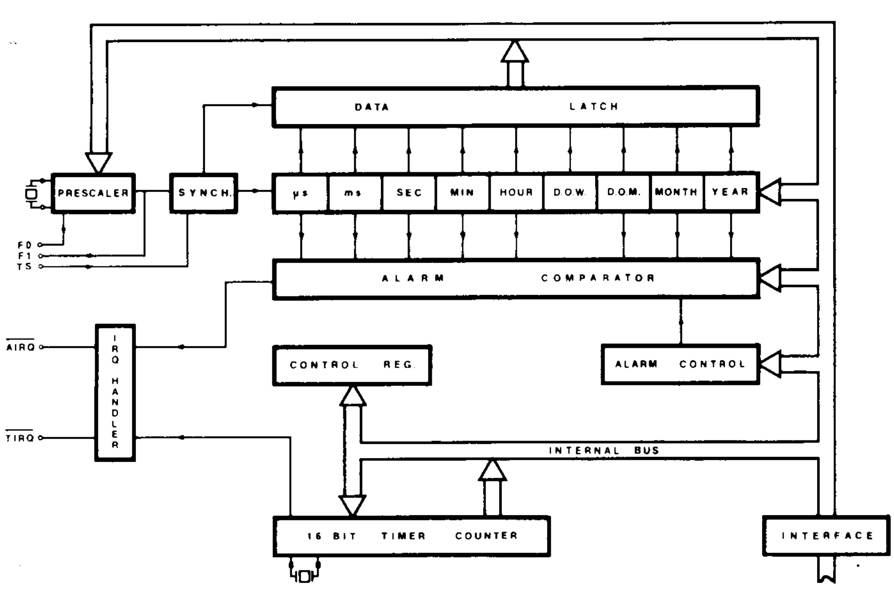
General Description

The HI-8000 is a μP bus oriented REAL-TIME CLOCK with a max. count of 128 years and a max. resolution of 3μs. The clock has 3 programmable prescalers, 4 buffered clock outputs and an ALARM interrupt. The ALARM is individually programmable for all clock registers. The clock has the ability to measure elapsed time and split time through the use of a dual rank storage on all counter registers. Provisions to build a crystal controlled oscillator have been made. The REAL TIME CLOCK has automatic leap year compensation and operates in a 12 hour mode with AM/PM indicators or in a 24 hour mode. Mode selection is under software control. All clock registers count in a binary mode. The count sequence of the individual registers is equivalent to a regular wrist-watch with calendar.

The HI-8000 also has an independent 16 bit timer-counter. Circuitry to build an on chip oscillator, read back, interrupt and square wave output capabilities are provided.

The IC interfaces easily with any μP that uses a multiplexed address/data bus like the MC146805, MC6801, 8085, 8048 and 8086. The HI-8000 is specially well suited in applications where standby power and battery backup are of concern.



HI-8000

REAL TIME LOW-POWER μ PROCESSOR COMPATIBLE CLOCK/TIMER/ALARM/ CALENDARS/STOPWATCH/EVENT COUNTER

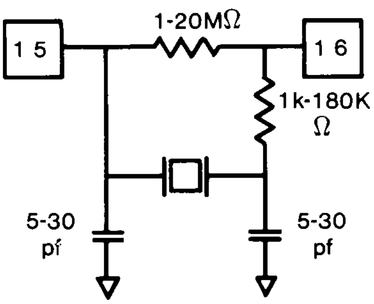
HOLT INC.
INTEGRATED CIRCUITS
8 Chrysler Ave.,
Irvine, CA 92714
(714) 859-8800

Real Time Clock

OSCILLATOR

The HI-8000 has on chip circuitry to build a crystal oscillator with an external parallel resonant crystal, two capacitors and two resistors. If another frequency source, that provides adequate input levels is available, pin 15 can then be used as an input. The max. frequency is 2.097152 MHz, the min. is 1 Hz. Pin 17 is a buffered output of the oscillator that can be used as a µP clock driver. The output will be disabled with the absence of the SU signal, however, the oscillator continues operation as long as V_{BB} is within operating limits. Fig. 1 shows typical circuit configuration for REAL TIME CLOCK oscillator. Component values depend on Xtal and its operating frequency. Typical range of values is shown below.

Fig. 1



NOTE: The maximum resolution for the real time clock is $\frac{1}{2^{16}}$ sec = 15.259µs. Pin 17, 18, 19 and 21 are the buffered frequency outputs of the oscillator (fo), the prescaler [fo/(N1+1)], the first divide by (N1+1) counter (fo/[(N1+1)(N2+1) and 1 Hz respectively. The outputs 17, 18 and 19 are only enabled when the SYSTEM -UP input is enabled. (Shutdown for battery standby operation).

The 1 sec output is an open drain output and is still active in battery standby mode.

PRESCALER AND STAGES

The HI-8000 uses a software controllable and programmable 5 bit divide by (N+1) prescaler followed by two fully programmable 8 bit divide by (N+1) up-counters with load and readback feature and an ALARM comparator section. Each of the three counters provides a clock output on pins 18, 19 and 21, respectively. The particular 3 counter arrangement allows the use and generation of many different frequencies that may be required in a system application. In order to use the HI-8000 as REAL TIME CLOCK, the following rule must be observed

$$fo/(N1+1) \bullet (N2+1) \bullet (N3+1) = 1\ Hz$$

Example

A particular application requires a µP clock of 0.8 MHz, the real time clock should have a resolution of 1/100 sec. This means that N3 = 99, and (N1+1) • (n2+1) = 8000 for fo = 800 kHz.

N1 = 31
N2 = 249
N3 = 99

5-BIT PRESCALER

The 5-bit prescaler is a divide by N+1 up counter. The counter is programmed over the data bus and can be enabled or disabled through Bit 1 of the HI-8000 CONTROL register. When disabled, the counter is reset to 0. This feature can be used to synchronize the clock to the exact time of day.

8-BIT DIVIDE BY N+COUNTERS

Counter 1 and Counter 2 are divide by (N+1) up counters, which are programmed over the data bus. The loaded value of N cannot be *read back*, however, the current count of the counters can be read back. The counters are the first 2 stages of the REAL TIME CLOCK.

SECONDS COUNTER CLOCK

The clock of the seconds counter can be enabled and disabled with Bit 5 of the CONTROL register. This allows to stop the internal 1 Hz clock without stopping the clocks of outputs 17, 18, 19, and 21. This feature allows to synchronize the clock with an accuracy of better than 1 sec. (See synchronization of REAL TIME CLOCK).

CLOCK STAGES

All clock stages are fully programmable and look to the user like memory locations. Each stage is tied into the ALARM system with the exception of the Day of Week (DOW) stage. The max. achievable resolution is 15.3 µs.

The resolution selected depends on the particular application. A typical resolution is for example .1ms (N2 and N3= 99). All clock stages count in a binary mode. The HI-8000 has the following stages:

Counter 1, Counter 2, Seconds, Minutes, Hours, Day of Week, Day of Month, Months and Years.

The typical clock stage has 3 sections, the actual REAL TIME counter, the Readback Latch and the ALARM section. The time keeping element is the REAL TIME counter that can be preset through the data bus. The current state of the counter can be read through the Readback Latch. In order to take a real time reading, a COPY LATCH command or a 0/1 transition on pin 20 has to be generated. This updates the Readback Latches of the entire REAL TIME CLOCK. Then the Readback Latches of interest are read.

COUNTING SEQUENCE OF INDIVIDUAL STAGES

COUNTER	MIN	MAX	NOTES
SECONDS	0	59	
MINUTES	0	59	
HOURS	1	12	12 HOUR MODE MSB = AM/PM INDICATOR
HOURS	0	23	MSB = 0
DOW	1	7	
DOM	1	28, 29, 30, 31	MONTH AND YEAR DEPENDENT
MONTHS	1	12	
YEARS	0	127	

NOTE: HOURS, DOW, DOM, MONTHS CAN BE PRESET TO Ø

ALARM, ALARM ENABLE AND INTERRUPT

The ALARM section consists of a comparator for the particular stage and an ALARM latch against which the REAL TIME Counter is compared. The ALARM comparator of each individual stage can be enabled or disabled through a corresponding bit in the ALARM CONTROL register. An ALARM interrupt is generated when all enabled comparators show equivalence.

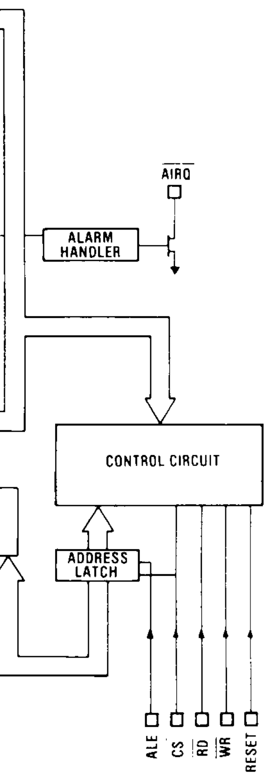
The interrupt flip-flop can be reset by software. The interrupt flip-flop is an edge triggered device which means that the change from the unequal to the equal state of the comparator circuit is what sets the $\overline{AIRQ}$ flip-flop.

ALARM CONTROL REGISTER

The ACR can be accessed through the address HEX 31 with a write operation. The following drawing shows the bit/stage allocation. 1 = enable.

ALARM CONTROL REGISTER

B7	B6	B5	B4	B3	B2	B1	BØ
YR	MO	DOM	HRS	MIN	SEC	CTR2	CTR1



NCHRONIZING THE AL TIME CLOCK

o clock by resetting B1 of the NTROL register. Program N for all nter stages and set all clock stages esired time. Set B1 at time coincice. The best achievable accuracy $\frac{1}{F_{osc}}$ + software delay + internal P DELAY.

Timer

OPERATING MODES

TIMER (CLOCK INDEPENDENT)

The HI-8000 has a 16 bit high frequency, programmable divide by N counter with readback that is entirely independent of the REAL TIME CLOCK. The circuitry to build a crystal oscillator by adding two capacitors, two resistors and a crystal is included, an external frequency source can also be used to drive the counter. The TIMER has a maskable interrupt output. (Interrupt gets set when counter reaches 0 state), and a SQUARE WAVE output. The period of the square wave is equal to two times the interrupt rate. The interrupt flip-flop and the counter's clock can be controlled with the CONTROL register through bits B4 and B3, respectively.

FREE RUNNING DIVIDE BY N MODE

N = 1 to 65535
The timer's operating mode is selected through the CONTROL REGISTER. In the free running divide by N mode, the timer generates a square wave output at the $\overline{TSW}$ output that has the frequency $\frac{fo}{2N}$

The interrupt output $\overline{TIRQ}$ will go low the first time the counter reaches 0, it can be reset by a control command, the square wave output ($\overline{TSW}$) will reset at the same time.

TIME DELAY MODE

In the Time Delay Mode, the timer generates an interrupt after N clock pulses and then stops. The counting cycle can be started by generating an internal RESET signal or by reloading the LSB of the divide by N counter. The counter clock can be enabled or disabled through the appropriate BIT of the CONTROL REGISTER.

NOTE: The TIMER is only functional with the presence of the SYSTEM-UP signal. Due to the high max. frequency of the TIMER, no provisions have been made to synchronize the uP-cycle with the TIMER clock, precautions have to be taken when reading the counter stages "on the fly" to assure correct data.

HI-8000 ADDRESS UTILIZATION

HEX WR	HEX RD	FUNCTION	# BITS	LIMITS LOW	HIGH	NOTES
20	ØØ	CLOCK COUNTER 1	8	Ø	255	
21	Ø1	CLOCK COUNTER 2	8	Ø	255	
22	Ø2	SECOND COUNTER	6	Ø	59	
23	Ø3	MINUTE COUNTER	6	Ø	59	
24	Ø4	HOUR COUNTER	5	Ø/1	23/12	8TH BIT AM/PM IND.
25	Ø5	DAY OF WEEK COUNTER	3	1	7	
26	Ø6	DAY OF MONTH COUNTER	5	1	31	
27	Ø7	MONTH COUNTER	4	1	12	
28	Ø8	YEAR COUNTER	7	1	127	
29	—	ALARM COMPARATOR CLOCK COUNTER 1	8	Ø	255	
2A	—	ALARM COMPARATOR CLOCK COUNTER 2	8	Ø	255	
2B	—	ALARM COMPARATOR SECONDS	6	Ø	59	
2C	—	ALARM COMPARATOR MINUTES	6	Ø	59	
2D	—	ALARM COMPARATOR HOURS	5	Ø/1	23/12	8TH BIT AM/PM IND.
2E	—	ALARM COMPARATOR DAY OF MONTH	5	1	31	
2F	—	ALARM COMPARATOR MONTHS	4	1	12	
3Ø	—	ALARM COMPARATOR YEARS	7	Ø	127	
31	—	ALARM CONTROL REGISTER	8	Ø	255	
32	—	CLEAR ALARM IRQ	—	—	—	DATA INDEPENDENT
33	—	N CLOCK COUNTER 1	8	Ø	255	
34	—	N CLOCK COUNTER 2	8	Ø	255	
35	—	N CLOCK PRESCALER	5	Ø	31	
36	—	MASTER RESET	—	—	—	DATA INDEPENDENT
37	17	LSB OF N COUNTER TIMER	8	Ø	255	RESET COUNTER
38	18	MSB OF N COUNTER TIMER	8	Ø	255	N>Ø TO COUNT
39	—	CLEAR TIMER IRQ	—	—	—	DATA INDEPENDENT
3A	—	CONTROL REGISTER	7	Ø	127	
3B	—	COPY LATCH	—	—	—	DATA INDEPENDENT

CONTROL REGISTER

1 = ENABLE

Fig.3

B7	B6	B5	B4	B3	B2	B1	BØ
NOT USED	ALARM IRQ ENABLE	SECONDS COUNTER ENABLE	TIMER IRQ ENABLE	TIMER MODE Ø = FREE RUN	TIMER CLOCK ENABLE	CLOCK PRESCALER ENABLE	12/24 HOUR MODE 1 = 12 HR

Software and Hardware Considerations

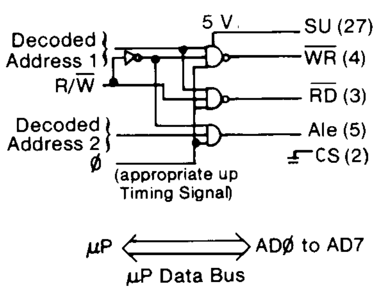
POWER UP CONDITION

A) WITHOUT BATTERY BACKUP
(PINS 27 and 28 = 5.0V)
After every power-up condition, the HI-8000 has to be initialized by applying a RESET Pulse to pin 26 or by doing a software MASTER RESET and clearing the CONTROL register. The clock oscillator will start up, but the prescaler is disabled. The clock interrupt is masked off. The TIMER oscillator will start up, but its counters are disabled. The interrupt is masked off and the square wave output ($\overline{TSW}$) FF is reset.

B) WITH BATTERY BACKUP
The presence or absence of the SU input signal enables or disables outputs f0, f1, f2, $\overline{TIRQ}$ and $\overline{TSW}$. The 1Hz- and AIRQ are open drain outputs and are still operational with the presence of VBB only, the clock independent timer and the µP interface is shut down and forced into a low power mode. When the +5V supply recovers, all disabled outputs will be enabled again. The timer will come up disabled and has to be reinitialized. All timer related outputs will come up in the high state.

NON MULTIPLEXED ADDRESS DATA BUS OPERATION

The HI-8000 can be easily addressed by any µ processor with separate address and data busses. Below is a typical interface.



Address 1 is the address that the µp reads and writes to when it is accessing the HI-8000.
Address 2 is the address that the µP uses when it addresses a specific HI-8000 function.
Decoded Address 1 and Decoded Address 2 are used to enable the HI-8000 when it is being accessed.

THE CONTROL REGISTER (CR)

The CR is a Bit register that can be loaded over the address HEX 3A. The register cannot be read back. Fig. 3 shows the individual bit assignments.

COMMENTS

The HI-8000 can be used with a variety of different µPs with a minimum of external components.

1. The HI-8000 appears to the programmer like memory with two exceptions that have to be observed; unutilized address space should not be accessed, *any read operation from the HI-8000 has to be preceded by a write operation to the same address as the read operation.*
2. The CHIP SELECT line is latched internally with the trailing transition of the ALE signal. RD pulses must not be presented to the HI-8000 unless the $\overline{CS}$ input is low.
3. None of the inputs should be left floating, the data bus should be in a defined logic state when not in use in order to minimize current consumption.
4. The SU input is a control signal input used to control various outputs and internal circuitry, the input does not draw any power.
5. Allow at least 7µs between copy latch command or TS transition and the write prior to read operation.

LOW POWER OPERATION

For applications where power consumption is a main concern, the crystal oscillator frequency should be chosen as low as possible. Using a readily available watch crystal (32.768 KHz) is a good compromise between power consumption, availability and cost of the crystal.

BATTERY BACKUP

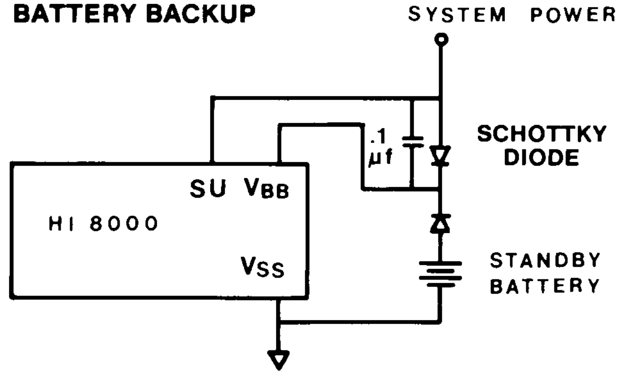


Fig. 2

Electrical Specifications

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{BB}	−.5 to 6.0	V_{dc}
Input Voltage, All Inputs	V_{IN}	−.5 to V_{BB}	V_{dc}
DC Current Drain Per Pin	I	20.0	mA
Operating Temperature Range	TA	−40 to +80	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Operating Voltage Range	V_{DD}	1.5 to 5.0	V_{dc}

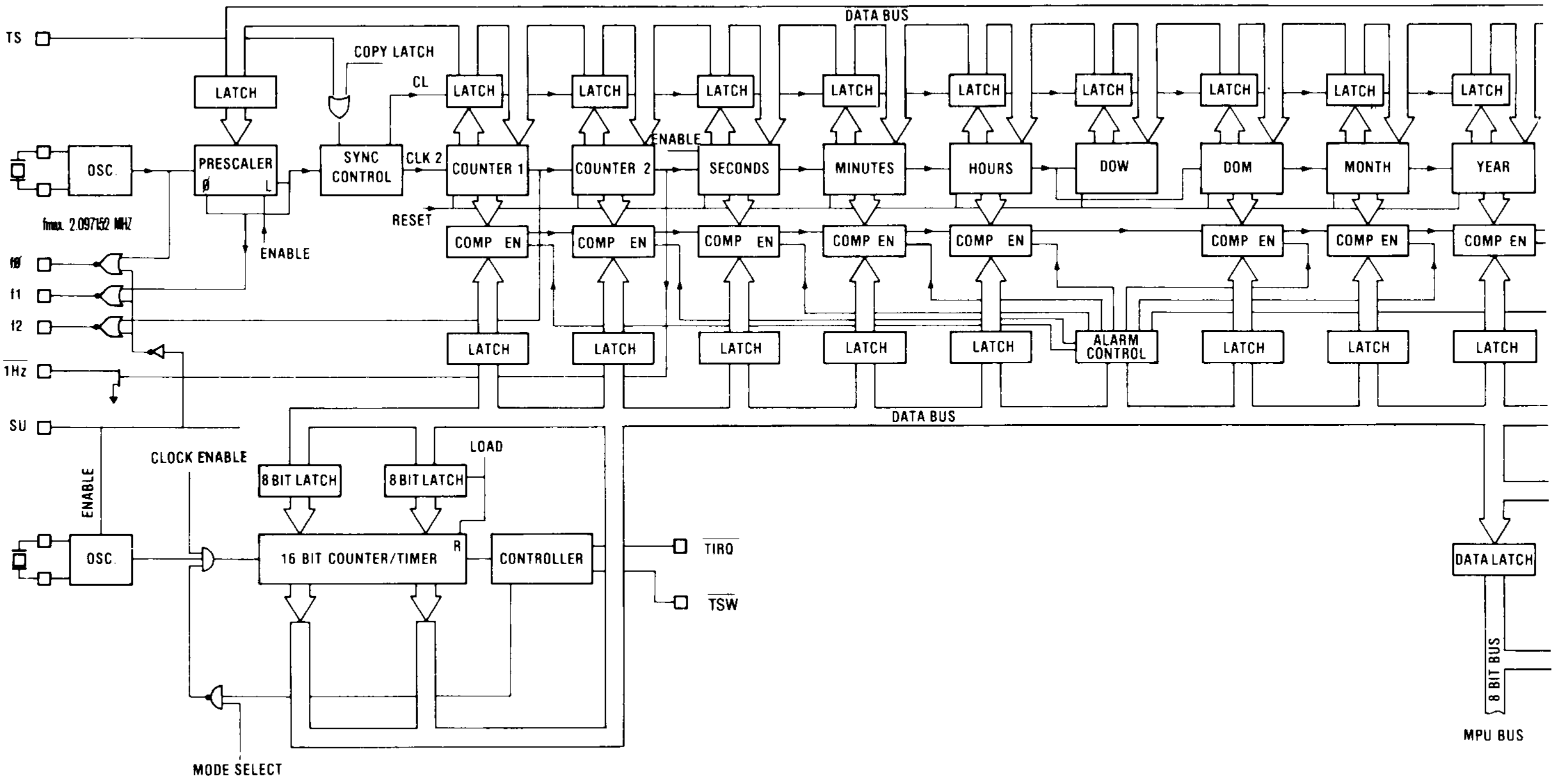
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage (all inputs)	V_{IL}	.5	—	.8	V
Input High Voltage (all except TOI and COI)	V_{IH}	2.0	—	V_{BB}	V
Input High Voltage (TOI and COI)	V_{IH1}	3.0	—	V_{BB}	V
Output Low Voltage (ADØ to AD7) for I_{OH} = .8 mA	V_{OL}	—	.15	.4	V
Output Low Voltage ($\overline{TIRQ}$, $\overline{AIRQ}$, $\overline{TSW}$, f_0, f_1, f_2, COO and TOO) for I_{OL} = .4 mA	V_{OL1}	—	.15	.4	V
Output High Voltage (ADØ to AD7) for I_{OH} = .2 mA	V_{OH}	2.4	4.0	—	V
Output High Voltage $\overline{TIRQ}$, f_0, F_1, f_2, COO and TOO for I_{OH} = .1 mA	V_{OH1}	2.4	4.0	—	V
Input Leakage Current ($V_{SS} \leqslant V_{IN} \leqslant V_{BB}$)	I_{IL}	—	—	1	µA
Output Leakage Current ($V_{BB} \geqslant V_I \geqslant V_{SS}$) for ADØ to AD7	I_{OL}	—	—	1	µA
Output Leakage Current ($V_{BB} \geqslant V_I \geqslant V_{SS}$) for Open Drain Output 1 $\overline{Hz}$ and $\overline{AIRQ}$	I_{OL1}	—	—	1	µA
(1) Current Consumption (5V)	I_{BB}				
*for f_{CC} = 32kHz, f_{CT} = 0		—	40	—	µA
for f_{CT} = 32kHz, f_{CC} = 0		—	40	—	µA
*for f_{CC} = 1MHz, f_{CT} = 0		—	200	—	µA
for f_{CT} = 1MHz, f_{CC} = 0		—	200	—	µA
SU = 1 Operating Voltage	VBB	4.75	5.0	5.25	V
SU = Ø Operating Voltage		3.0		5.25	

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit.

(1) Current consumption in the SU = Ø mode is considerably lower at 3V.
For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{BB}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., Vss or V BB).

Block Diagram



Using the Real Time Clock

REAL TIME CLOCK

After power turn-on, load N for clock PRESCALER and clock counters 1 and 2 according to resolution and crystal frequency requirements. Stop and reset the PRESCALERS and select the 12/24 hours mode by setting the appropriate bits in the control register. 'ake a time reading, issue a COPY CH command or generate a ⎍ transition on the TS input, then read the register or interest.

ELAPSE-TIMER, CLOCK

In this mode, the HI-8000 is used as a REAL TIME CLOCK and the counter stages show the correct time of day and date. To measure elapse time, generate a COPY LATCH or a ⎍ transition on the TS input to generate your start reference. Read all clock registers of interest. To take a split or stop time reading, generate another COPY LATCH command or a ⎍ transition on the TS input. Take a new reading of all clock registers of interest and form the time difference between the two readings through a software algorithm.

ELAPSE TIMER ONLY

To start the time, software clear operation is performed (clock is in the running mode.) All clock stages are reset and will start counting with the trailing edge of $\overline{WR}$. to take a split time reading, generate a ⎍ transition on the TS input or a software controlled COPY LATCH operation. This will copy the state of the timer into corresponding registers from which the split time can be recovered. You can take multiple split time readings. To stop the timer for final elapse time reading, stop the timer by clearing the corresponding bit in the CONTROL REGISTER, issue a COPY LATCH command or a ⎍ transition on the TS input and read the clock register.

NOTE: A software MASTER RESET operation resets *all* counter stages of the REAL TIME CLOCK to zero. This means for the month counter for example, that it starts its counting sequence at zero, counts up to 12 and resets to one when the year counter is incremented.

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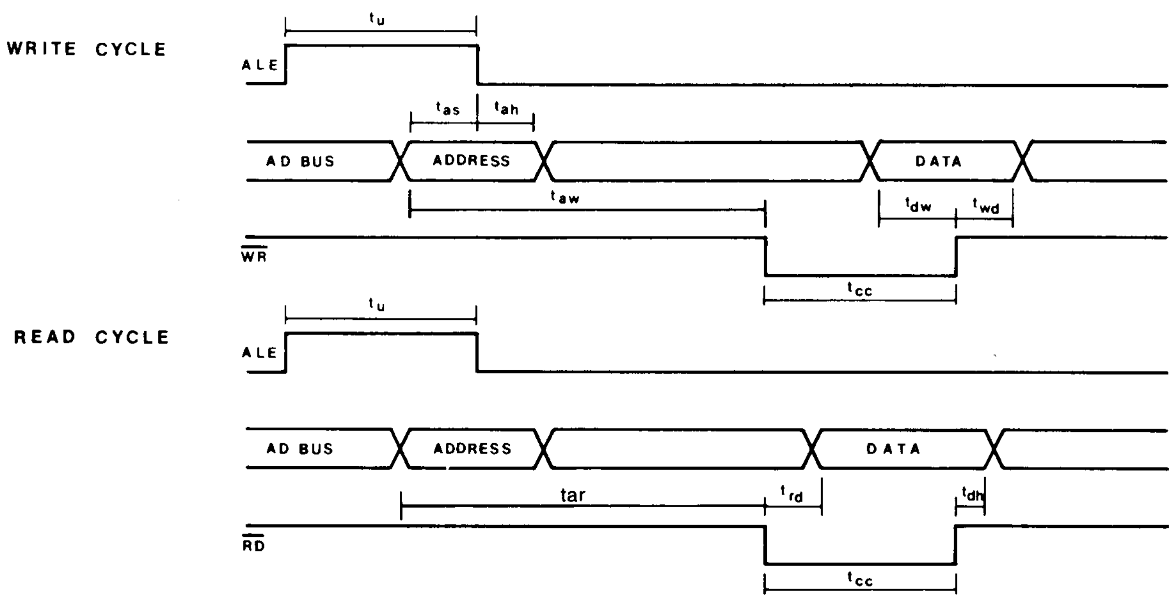
HI-8000

REAL TIME LOW POWER µ PROCESSOR COMPATIBLE CLOCK/TIMER/ ALARM/CALENDARS/ STOPWATCH/ EVENT COUNTER

TIMING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Real Time Clock Oscillator	$f_{cc\ max}$	2.1	—	—	MHz
Timer Clock Oscillator	$f_{ct\ max}$	.8	1.0	—	MHz
Pulse Width f_1, f_2, 1Hz	tpw1	.3	1.5	—	µs
Pulse Width f_0	tpw0	200	—	—	ns
ALE Pulse Width	tu	160	—	—	ns
Address Setup to ALE	tas	120	—	—	ns
Address Hold from ALE	tah	40	—	—	ns
Control Pulse Width $\overline{RD}$, $\overline{WR}$	tcc	320	—	—	ns
Data Setup before $\overline{WR}$	tdw	180	—	—	ns
Data Hold after $\overline{WR}$	twd	40	—	—	ns
Address Setup to $\overline{WR}$, $\overline{RD}$	taw, tar	160	—	—	ns
$\overline{RD}$ to Data Out (200pf Load)	trd	—	—	250	ns
Data Hold	tdh	—	200	300	ns
Pulse Width TS, RESET	tpwz	.3	1.0	—	µs

NOTE: All measurements taken at V_{BB} = 5.ØV, V_{SS} = ØV, T_A = 25°C unless otherwise specified.



HI-8000P = Plastic
C = Ceramic

HI-8000
PIN-ASSIGNMENT 28 PIN DIP

Plastic 16

TIMER SQUARE WAVE	$\overline{TSW}$	1	28	V BB (V DD)	
CHIP SELECT	$\overline{CS}$	2	27	SU	SYSTEM UP
READ	$\overline{RD}$	3	26	RESET	
WRITE	$\overline{WR}$	4	25	$\overline{TIRQ}$	TIMER INTERRUPT
ADDRESS LATCH ENABLE	ALE	5	24	TOI	TIMER OSCILLATOR
	ADO	6	23	TOO	TIMER OSCILLATOR
	AD1	7	22	$\overline{AIRQ}$	ALARM INTERRUPT
	AD2	8	21	$\overline{1\ Hz}$	
	AD3	9	20	TS	TRANSFER STROBE
	AD4	10	19	f2	PRESCALER OUTPUTS
	AD5	11	18	f1	
	AD6	12	17	f0	CLOCK BUFFER
	AD7	13	16	COO	CLOCK-OSCILLATOR
	GND (Vss)	14	15	COI	CLOCK-OSCILLATOR

4/20/84

HOLT INTEGRATED CIRCUITS INC
8 Chrysler Ave.,
Irvine, CA 92714
(714) 859-8800