

## Dual A/D Converter

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs ( $\bar{C}_A$  and  $\bar{C}_B$ ) operate from MECL III or MECL 10,000 digital levels. When  $\bar{C}_A$  is at a logic high level,  $Q_0$  will be at a logic high level provided that  $V_1 > V_2$  ( $V_1$  is more positive than  $V_2$ ).  $\bar{Q}_0$  is the logic complement of  $Q_0$ . When the clock input goes to a low logic level, the outputs are latched in their present state.

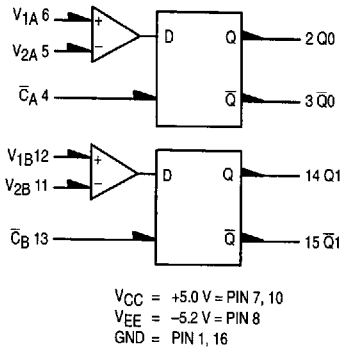
Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

**MC1650**  
**MC1651**



L SUFFIX  
CERAMIC PACKAGE  
CASE 620-10

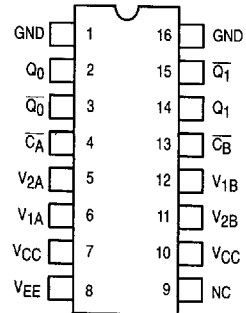
### LOGIC DIAGRAM



- $P_D = 330 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 3.5 \text{ ns typ (MC1650)}$   
=  $3.0 \text{ ns typ (MC1651)}$
- Input Slew Rate =  $350 \text{ V}/\mu\text{s (MC1650)}$   
=  $500 \text{ V}/\mu\text{s (MC1651)}$
- Differential Input Voltage:  $5.0 \text{ V (-30}^\circ\text{C to +85}^\circ\text{C)}$
- Common Mode Range:  
-  $-3.0 \text{ V to +2.5 V (-30}^\circ\text{C to +85}^\circ\text{C (MC1651)}$   
-  $-2.5 \text{ V to +3.0 V (-30}^\circ\text{C to +85}^\circ\text{C (MC1650)}$
- Resolution:  $\leq 20 \text{ mV (-30}^\circ\text{C to +85}^\circ\text{C)}$
- Drives  $50 \Omega$  lines

Number at end of terminal denotes pin number for L package (Case 620).

### PIN ASSIGNMENT



**4**

### TRUTH TABLE

$\bar{C}$	$V_1, V_2$	$Q_{0n+1}$	$\bar{Q}_{0n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	X X	$Q_{0n}$	$\bar{Q}_{0n}$



MC1650 MC1651

**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Limits						Unit	
		-30°C		+25°C		+85°C			
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	Positive Negative	$I_{CC}$ $I_E$				25* 55*			mAdc
Input Current	MC1650 MC1651	$I_{in}$				10 40			$\mu$ Adc
Input Leakage Current	MC1650 MC1651	$I_R$				7.0 10.0			$\mu$ Adc
Clock Input Current		$I_{inH}$				350			
Output Voltage	Logic 1	$V_{OH}$	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc
Output Voltage	Logic 0	$V_{OL}$	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc
Threshold Voltage (Note 2.)	Logic 1	$V_{OHA}$	-1.065		-0.980		-0.910		Vdc
Threshold Voltage (Note 2.)	Logic 0	$V_{OLA}$		-1.630		-1.600		-1.555	Vdc

1. All data is for 1/2 MC1650 or MC1651, except data marked (\*) which refers to the entire package.
2. These tests are done in order indicated. See Figure 5.
3. Maximum Power Supply Voltages (beyond which device life may be impaired):  $|V_{EE}| + |V_{CC}| \geq 12$  Vdc.

4.

All Temperature	$V_{A3}$	$V_{A4}$	$V_{A5}$	$V_{A6}$
MC1650	+3.0	+2.98	-2.5	-2.48
MC1651	+2.5	+2.48	-3.0	-2.98

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**ELECTRICAL CHARACTERISTICS** (continued)

② Test Temperature			TEST VOLTAGE VALUES (Volts)										V <sub>CC</sub> <sup>3</sup>	V <sub>EE</sub> <sup>3</sup>
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAMin</sub>	V <sub>ILAmx</sub>	V <sub>A1</sub>	V <sub>A2</sub>	V <sub>A3</sub>	V <sub>A4</sub>	V <sub>A5</sub>	V <sub>A6</sub>		
-30°C			-0.875	-1.890	-1.180	-1.515	+0.02	+0.02	See Note 4.				+5.0	-5.2
+25°C			-0.810	-1.850	-1.095	-1.485	+0.02	+0.02	See Note 4.				+5.0	-5.2
+85°C			-0.700	-1.830	-1.025	-1.440	+0.02	+0.02	See Note 4.				+5.0	-5.2
Characteristic	Symbol	TEST VOLTAGE APPLIED TO PINS LISTED BELOW										(V <sub>CC</sub> ) Gnd		
		V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAMin</sub>	V <sub>ILAmx</sub>	V <sub>A1</sub>	V <sub>A2</sub>	V <sub>A3</sub>	V <sub>A4</sub>	V <sub>A5</sub>	V <sub>A6</sub>			
Power Supply Drain Current	Pos Neg I <sub>CC</sub> I <sub>E</sub>	4,13	4,13			6,12 6,12							1,5,11,16 1,5,11,16	
Input Current	MC1650 MC1651 I <sub>in</sub>	4	13			12		6					1,5,11,16	
Input Leakage Current	MC1650 MC1651 I <sub>R</sub>	4	13			12				6			1,5,11,16	
Clock Input Current	I <sub>inH</sub>	4	13			6,12							1,5,11,16	
Output Voltage	Logic 1 V <sub>OH</sub>	4,13				6,12 5,11 5,11	5,11 6,12	6,12 5,11	5,11 6,12	5,11 6,12	6,12 5,11		1,5,11,16 1,6,12,16 1,16 1,16 1,5,11,16 1,6,12,16 1,16 1,16	
Output Voltage	Logic 0 V <sub>OL</sub>	4,13				5,11 6,12	6,12 5,11	5,11 6,12	6,12 5,11	6,12 5,11	5,11 6,12		1,5,11,16 1,6,12,16 1,16 1,16 1,5,11,16 1,6,12,16 1,16 1,16	
Threshold Voltage Note 2.	Logic 1 V <sub>OHA</sub>		13	4 4	4 4	6 6	6 6						1,5,16	
Threshold Voltage Note 2.	Logic 0 V <sub>OLA</sub>		13	4 4	4 4	6 6	6 6						1,5,16	

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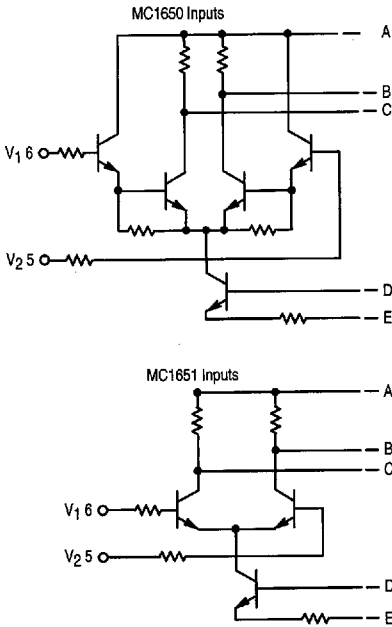
- All data is for 1/2 MC1650 or MC1651, except data marked (\*) which refers to the entire package.
- These tests are done in order indicated. See Figure 5.
- Maximum Power Supply Voltages (beyond which device life may be impaired): |V<sub>EE</sub>| + |V<sub>CC</sub>| ≥ 12 Vdc.

4.

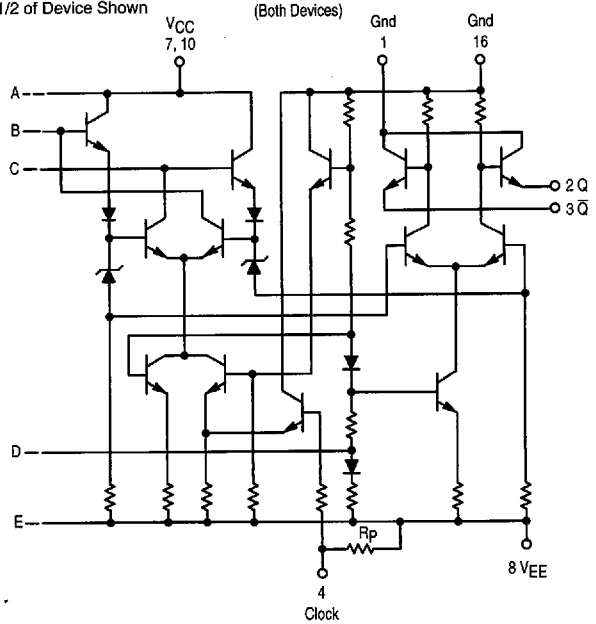
All Temperature	V <sub>A3</sub>	V <sub>A4</sub>	V <sub>A5</sub>	V <sub>A6</sub>
MC1650	+3.0	+2.98	-2.5	-2.48
MC1651	+2.5	+2.48	-3.0	-2.98

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC1650 MC1651



CIRCUIT SCHEMATIC  
1/2 of Device Shown



SWITCHING TEST VOLTAGE VALUES

@ Test Temperature

(Volts)						
VR1	VR2	VR3	VX	VXX	VCC <sup>1</sup>	VEE <sup>1</sup>
+2.0	See Note 4		+1.04	+2.0	+7.0	-3.2
+2.0			+1.11	+2.0	+7.0	-3.2
+2.0			+1.19	+2.0	+7.0	-3.2

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Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions (See Figures 1-3)						
		Min	Max	Min	Max	Min	Max								
Switching Times	t <sub>pd</sub>	2.0	5.0	2.0	5.0	2.0	5.7	ns	VR1 to V2, VX to Clock, P1 to V1, or, VR2 to V2, VX to Clock, P2 to V1, or, VR3 to V2, VX to Clock, P3 to V1.						
Propagation Delay (50% to 50%) V-Input Clock <sup>2</sup>										2.0	4.7	2.0	4.7	2.0	5.2
Clock Enable <sup>3</sup>	t <sub>setup</sub>	—	—	2.5	—	—	—	ns	VR1 to V2, P1 to V1, P4 to Clock						
Clock Aperture <sup>3</sup>	t <sub>ap</sub>	—	—	1.5	—	—	—	ns							
Rise Time (10% to 90%)	t <sub>+</sub>	1.0	3.5	1.0	3.5	1.0	3.8	ns	VR to V2, VX to Clock, P1 to V1.						
Fall Time (10% to 90%)	t <sub>-</sub>	1.0	3.0	1.0	3.0	1.0	3.3	ns							

NOTES:

1. Maximum Power Supply Voltages (beyond which device life may be impaired:

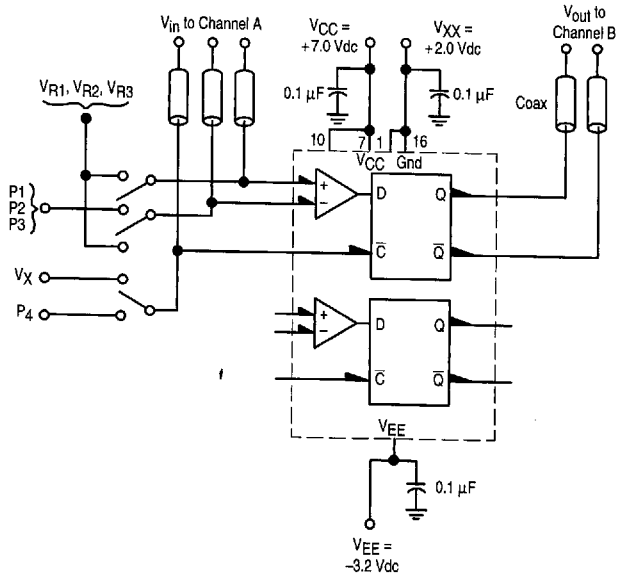
$$|V_{CC}| + |V_{EE}| \geq 12 \text{ Vdc.}$$

2. Unused clock inputs may be tied to ground.

3. See Figure 3.

All Temperatures	VR2	VR3
MC1650	+4.9	-0.4
MC1651	+4.4	-0.9

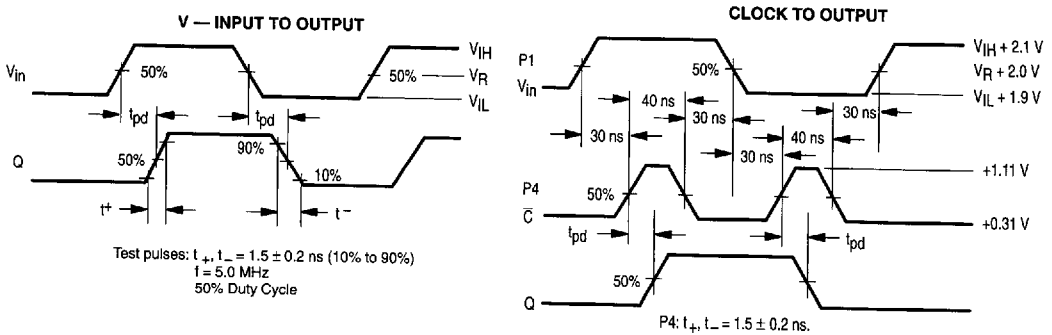
FIGURE 1 — SWITCHING TIME TEST CIRCUIT @ 25°C



Note: All power supply and logic levels are shown shifted 2.0 volts positive.  
 50 ohm termination to ground located in each scope channel input.  
 All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

FIGURE 2 — SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

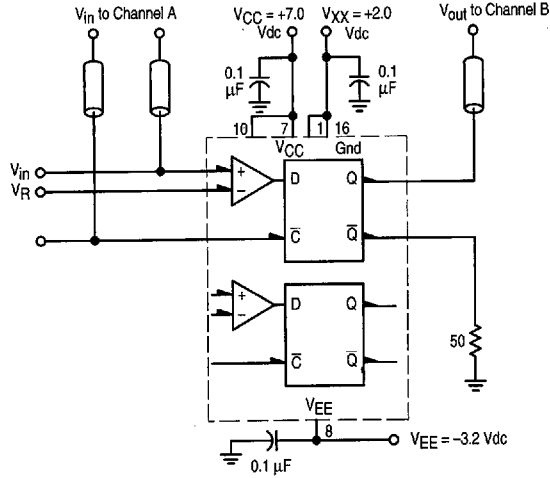


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TEST PULSE LEVELS

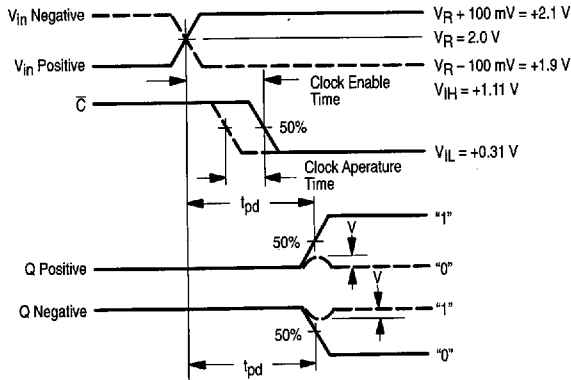
	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V <sub>IH</sub>	+2.1 V	+2.1 V	+5.0 V	+4.5 V	-0.3 V	-0.8 V
V <sub>R</sub>	+2.0 V	+2.0 V	+4.9 V	+4.4 V	-0.4 V	-0.9 V
V <sub>IL</sub>	+1.9 V	+1.9 V	+4.8 V	+4.3 V	-0.5 V	-1.0 V

FIGURE 3 — CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50 ohm termination to ground located in each scope channel input.  
All input and output cables to the scope are equal lengths of 50 ohms coaxial cable.

**ANALOG SIGNAL POSITIVE AND NEGATIVE SLEW CASE**

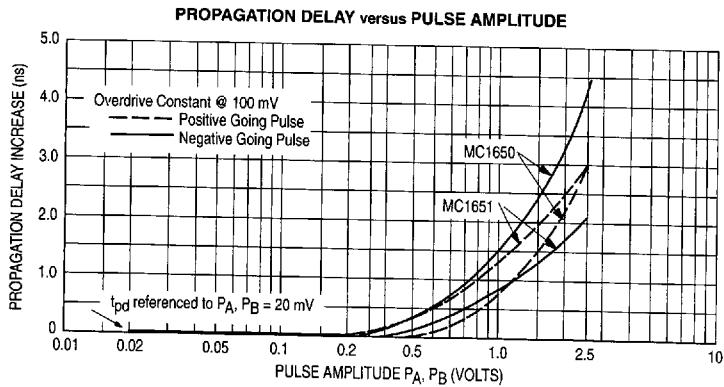
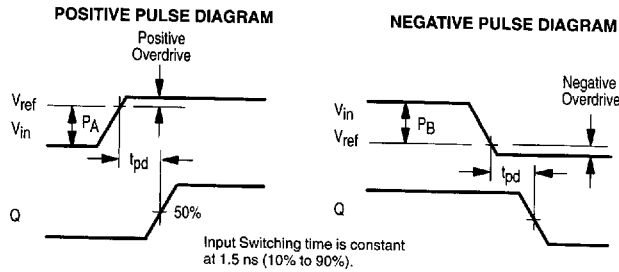
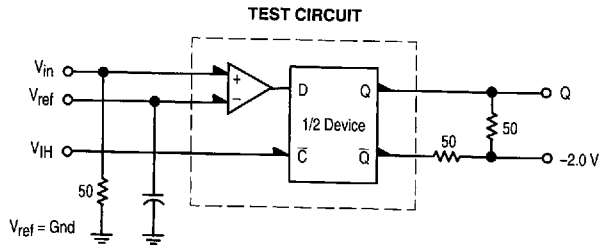


- Clock enable time = minimum time between analog and clock signal such that output switches, and  $t_{pd}$  (analog to Q) is not degraded by more than 200 ps.
- - - - - Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

Note: All power supply and logic levels are shown shifted 2.0 volts positive.

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**FIGURE 4 — PROPAGATION DELAY ( $t_{pd}$ ) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE**



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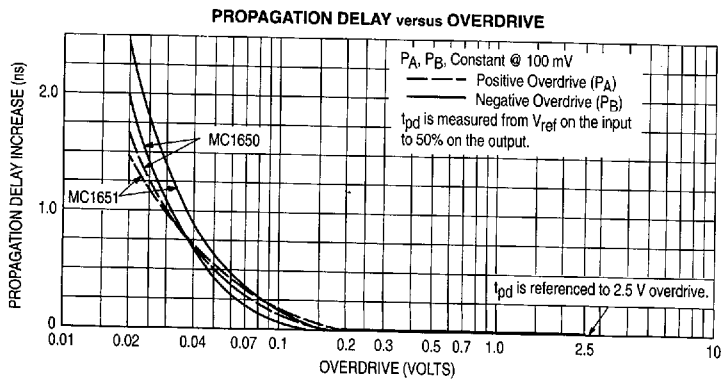


FIGURE 5 — LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

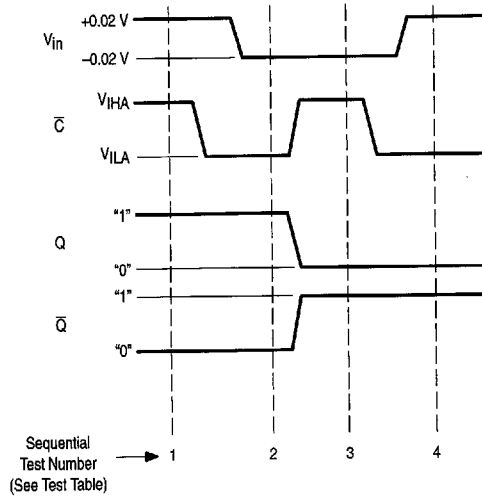
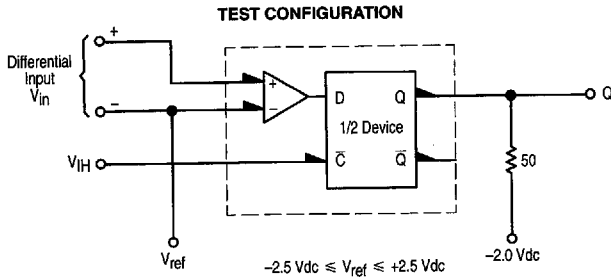
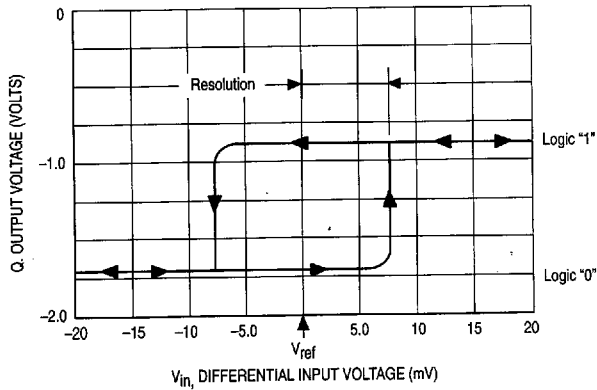


FIGURE 6 — TRANSFER CHARACTERISTICS (Q versus  $V_{in}$ )



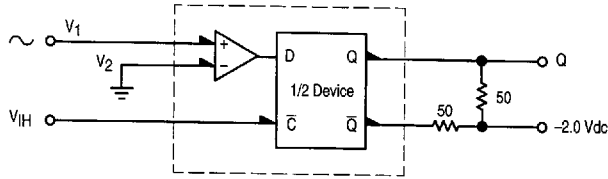
**TYPICAL TRANSFER CURVES**



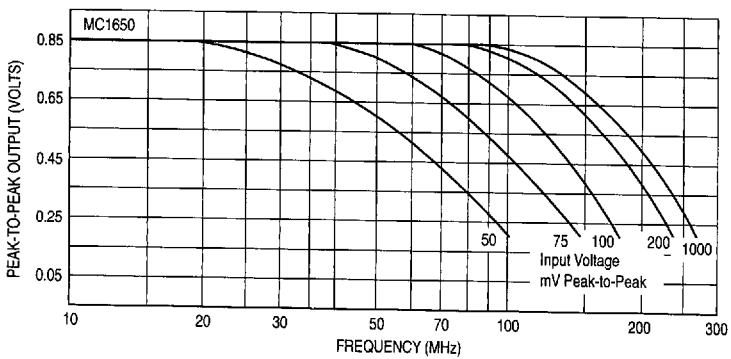
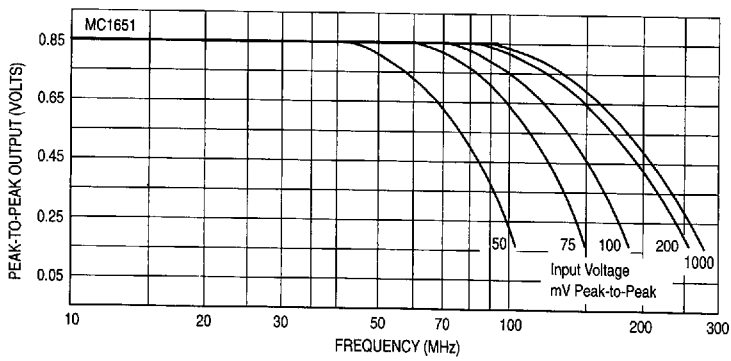
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FIGURE 7 — OUTPUT VOLTAGE SWING versus FREQUENCY

(A) TEST CIRCUIT



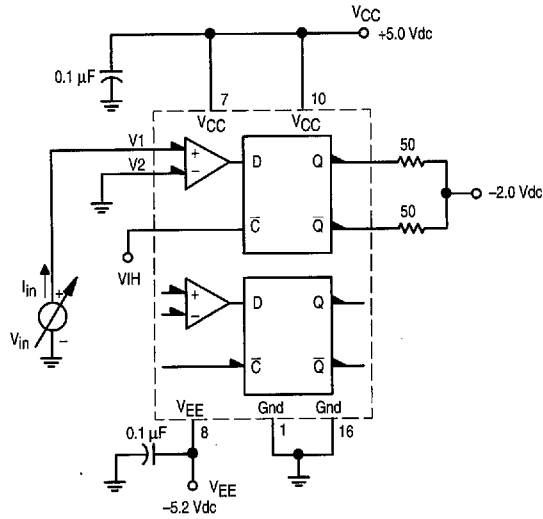
(B) TYPICAL OUTPUT LOGIC SWING versus FREQUENCY



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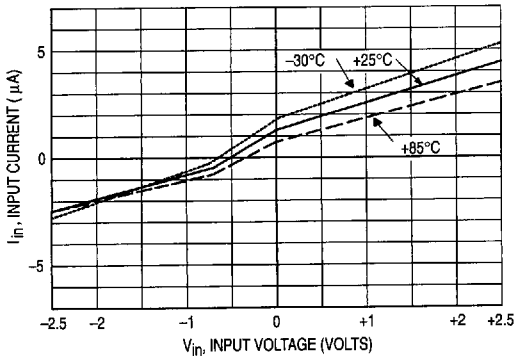
FIGURE 8 — INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



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Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)

