

**FEATURES**

- Differential 50Ω ECL outputs
- Choice between differential PECL or TTL clock input
- Single +5V power supply
- V<sub>BB</sub> output for single-ended use
- Multiple power and ground pins to minimize noise
- Specified within-device skew
- ESD protection of 2000V
- Fully compatible with Motorola MC10H/100H606
- Available in 28-pin PLCC package

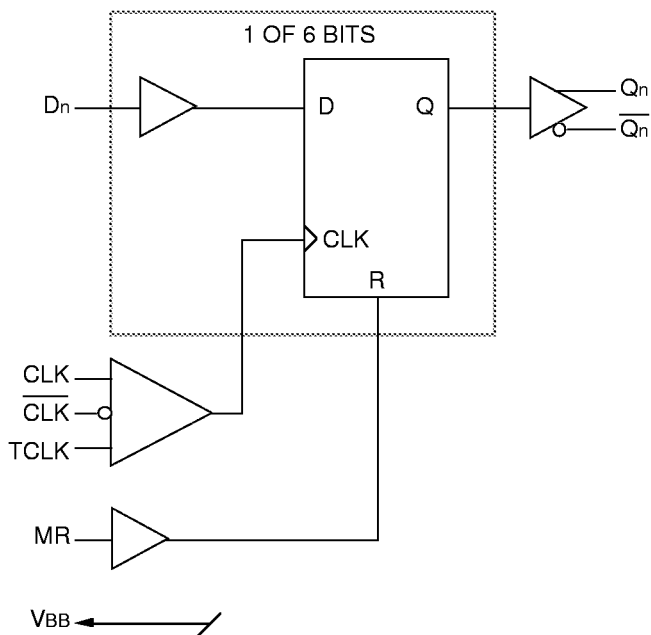
**DESCRIPTION**

The SY10/100H606 are 6-bit, registered, single supply TTL-to-PECL translators. The devices feature differential PECL outputs as well as a choice between either a differential PECL clock input or a TTL clock input. The asynchronous master reset control is a PECL level input.

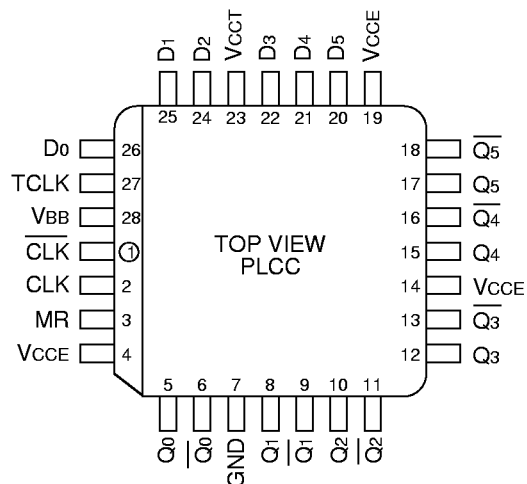
With its differential ECL outputs and TTL inputs, the H606 device is ideally suited for the transmit function of a HPPI bus-type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with 10K logic levels, while the 100H device is compatible with 100K logic levels.

**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
D <sub>0</sub> – D <sub>5</sub>	TTL Data Inputs
CLK, CLK̄	Differential PECL Clock Inputs
TCLK	TTL Clock Input
MR	PECL Master Reset Input
Q <sub>0</sub> – Q <sub>5</sub>	True PECL Outputs
Q̄ <sub>0</sub> – Q̄ <sub>5</sub>	Inverted PECL Outputs
V <sub>CC</sub> E	PECL V <sub>cc</sub> (5.0V)
V <sub>CC</sub> T	TTL V <sub>cc</sub> (5.0V)
GND	TTL/PECL Ground
V <sub>BB</sub>	V <sub>BB</sub> Reference Output (PECL)

## TRUTH TABLE

Dn	MR	TCLK/CLK	Qn + 1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = Low to High Transition.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C			TA= +25°C			TA= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>CC</sub> L	Supply Current	—	18	30	—	18	30	—	18	30	mA	Outputs LOW
I <sub>CC</sub> H	Supply Current	—	13	25	—	13	25	—	13	25	mA	Outputs HIGH
I <sub>GND</sub>	Supply Current	—	75	90	—	75	90	—	75	95	mA	

## TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>IH</sub>	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	
V <sub>IL</sub>	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	
V <sub>IK</sub>	Input Clamp Voltage	—	-1.2	—	-1.2	—	-1.2	V	I <sub>IN</sub> = -18mA
I <sub>IH</sub>	Input HIGH Current	—	20	—	20	—	20	μA	V <sub>IN</sub> = 2.7V V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current	—	-0.6	—	-0.6	—	-0.6	mA	V <sub>IN</sub> = 0.5V

## 10H PECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

$V_{CC} = V_{CE} = 5.0V \pm 5\%$

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	225	—	145	—	145	μA	
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	
V <sub>IH</sub>	Input HIGH Voltage	3830	4160	3870	4190	3930	4280	mV	V <sub>CC</sub> = 5.0V
V <sub>IL</sub>	Input LOW Voltage	3050	3520	3050	3520	3050	3555	mV	V <sub>CC</sub> = 5.0V
V <sub>OH</sub>	Output HIGH Voltage	3980	4160	4020	4190	4080	4270	mV	V <sub>CC</sub> = 5.0V
V <sub>OL</sub>	Output LOW Voltage	3050	3370	3050	3370	3050	3400	mV	V <sub>CC</sub> = 5.0V
V <sub>BB</sub>	Output Bias Voltage	3620	3730	3650	3750	3690	3810	mV	V <sub>CC</sub> = 5.0V

### NOTE:

1. PECL V<sub>IL</sub>, V<sub>IH</sub>, V<sub>OL</sub>, V<sub>OH</sub>, V<sub>BB</sub> are given for V<sub>CC</sub> = V<sub>CE</sub> = 5.0V and will vary 1:1 with power supply.

## 100H PECL DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

 $V_{CC} = V_{EE} = 5.0V \pm 5\%$ 

Symbol	Parameter	TA= 0°C		TA= +25°C		TA= + 85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	225	—	145	—	145	μA	
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	
V <sub>IH</sub>	Input HIGH Voltage	3835	4120	3835	4120	3835	4120	mV	V <sub>CC</sub> = 5.0V
V <sub>IL</sub>	Input LOW Voltage	3190	3525	3190	3525	3190	3525	mV	V <sub>CC</sub> = 5.0V
V <sub>OH</sub>	Output HIGH Voltage	3975	4120	3975	4120	3975	4120	mV	V <sub>CC</sub> = 5.0V
V <sub>OL</sub>	Output LOW Voltage	3190	3380	3190	3380	3190	3380	mV	V <sub>CC</sub> = 5.0V
V <sub>BB</sub>	Output Bias Voltage	3620	3740	3620	3740	3620	3740	mV	V <sub>CC</sub> = 5.0V

### NOTE:

 1. PECL V<sub>IL</sub>, V<sub>IH</sub>, V<sub>OL</sub>, V<sub>OH</sub>, V<sub>BB</sub> are given for V<sub>CC</sub> = V<sub>CE</sub> = 5.0V and will vary 1:1 with power supply.

## AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = V_{CE} = 5.0V \pm 5\%$ 

Symbol	Parameter	TA= 0°C			TA= +25°C			TA= + 85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PD</sub>	Propagation Delay TCLK+ +	0.800	—	2.800	0.800	—	2.800	0.800	—	2.800	ns	
t <sub>PD</sub>	Propagation Delay TCLK+ -	0.800	—	2.800	0.800	—	2.800	0.800	—	2.800	ns	
t <sub>PD</sub>	Propagation Delay CLK+ +	0.800	—	2.800	0.800	—	2.800	0.800	—	2.800	ns	
t <sub>PD</sub>	Propagation Delay CLK+ -	0.800	—	2.800	0.800	—	2.800	0.800	—	2.800	ns	
t <sub>PD</sub>	Propagation Delay MR+ -	0.800	—	2.800	0.800	—	2.800	0.800	—	2.800	ns	
t <sub>S</sub>	Set-up Time	1.5	0.5	—	1.5	0.5	—	1.5	0.5	—	ns	
t <sub>H</sub>	Hold Time 1.5	0.5	—	1.5	0.5	—	1.5	0.5	—	ns		
t <sub>PW</sub>	Minimum Pulse Width CLK	1.5	—	—	1.5	1.0	—	1.5	—	—	ns	
t <sub>PW</sub>	Minimum Pulse Width MR	1.5	—	—	1.5	—	—	1.5	—	—	ns	
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time	—	—	2.0	—	1.0	2.0	—	—	2.0	ns	
t <sub>RES/REC</sub>	Reset/Recovery Time	2.5	2.0	—	2.5	2.0	—	2.5	2.0	—	ns	

## PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H606JC	J28-1	Commercial
SY10H606JCTR	J28-1	Commercial
SY100H606JC	J28-1	Commercial
SY100H606JCTR	J28-1	Commercial

**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

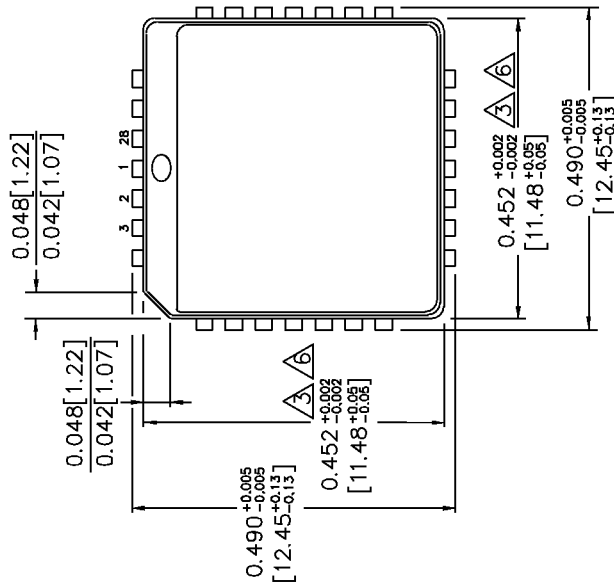
FILE/REV #: PD0008A03

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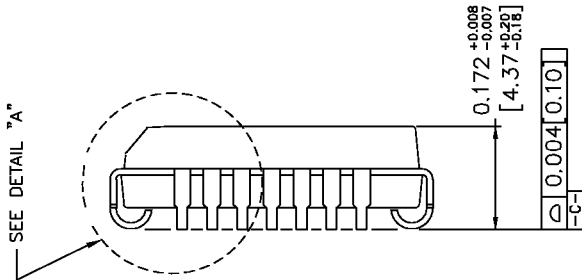
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REV	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

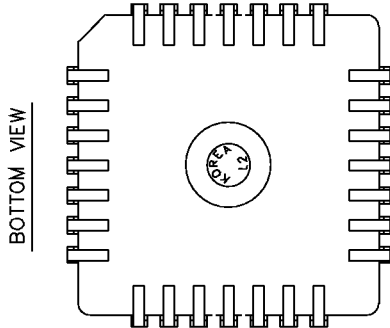
TOP VIEW



SIDE VIEW

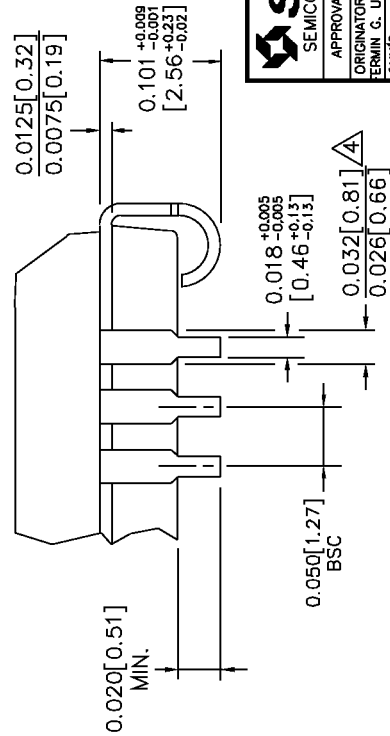


SEE DETAIL "A"



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

**SYNERGY**  
SEMICONDUCTOR

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FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A  
REVISION: 03