MICRO NETWORKS

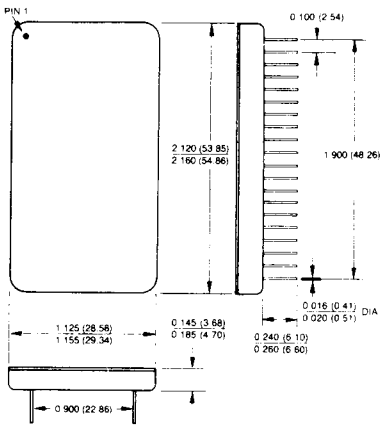
MN6249

2MHz, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- 2MHz Sampling Rate With Internal T/H Amplifier
- 12MHz Input Bandwidth
- FFT Testing
- Minimum 68dB Signal-to-Noise Ratio to Nyquist
- Typical −78dB Harmonics Over Full Bandwidth
- Small 40-Pin DIP
- No Missing Codes Guaranteed Over Temperature
- TTL Compatible Digital Inputs and Outputs
- 3-State Output Buffer
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

40 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN6249 is a 2MHz, 12-bit sampling A/D converter which offers outstanding dynamic as well as static performance. This sampling A/D contains an internal T/H amplifier and a 12-bit, subranging A/D converter in a single, 40-pin, triple-wide DIP package. The internal T/H amplifier allows the A/D converter to digitize 1MHz full-scale input signals at rates up to 2MHz. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 68dB minimum signal-to-noise ratio (SNR, rms-to-rms) and up to −78dB harmonics and spurious noise.

MN6249 is configured such that the internal T/H amplifier is completely transparent. The T/H's operational mode is internally controlled by the A/D timing logic. Users need only supply start convert commands at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and specification/testing eliminates the need for potentially confusing and often misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.

MN6249 is an excellent choice for digitizing analog signals in systems that require both high-resolution and high-speed in as small a package as possible. Typical applications include spectrum, vibration, waveform and transient analysizers; radar, sonar and video digitizers; medical imaging equipment; digital filters; and multiplexed or simultaneous-sampling data-acquisition systems.

MN6249 is manufactured in Micro Networks MIL-STD-1772 qualified facility, and for military/aerospace and harsh environment industrial applications, the MN6249 H/B is available with Environmental Stress Screening while the MN6249 H/B CH is 100% screened to MIL-H-38534.

Contact factory for availability of CH devices.

February 1990

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN6249 2MHz 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN6249J, K	0°C to +70°C (case)
MN6249S, T	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
Positive Supply (+Vcc, Pin 19)	−0.5 to +18 Volts
Negative Supply (−Vcc, Pin 25)	+0.5 to −18 Volts
Logic Supply (+Vdd, Pin 5, 29, 40)	−0.5 to +7 Volts
−5.2V Supply (−Vee, Pin 14)	0 to −7 Volts
Digital Inputs (Pins 7, 12)	−0.5 to +5.5 Volts
Analog Inputs:	
10V Range (Pin 16)	−7 to +7 Volts
5V Range (Pin 17)	−3.5 to +3.5 Volts
Reference Output Current	10mA

ORDERING INFORMATION

PART NUMBER — **MN6249X/B CH**

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" suffix to "S" or "T" models for Environment Stress Screening.

Add "CH" suffix to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.

Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V, −Vee = −5.2V unless otherwise indicated)

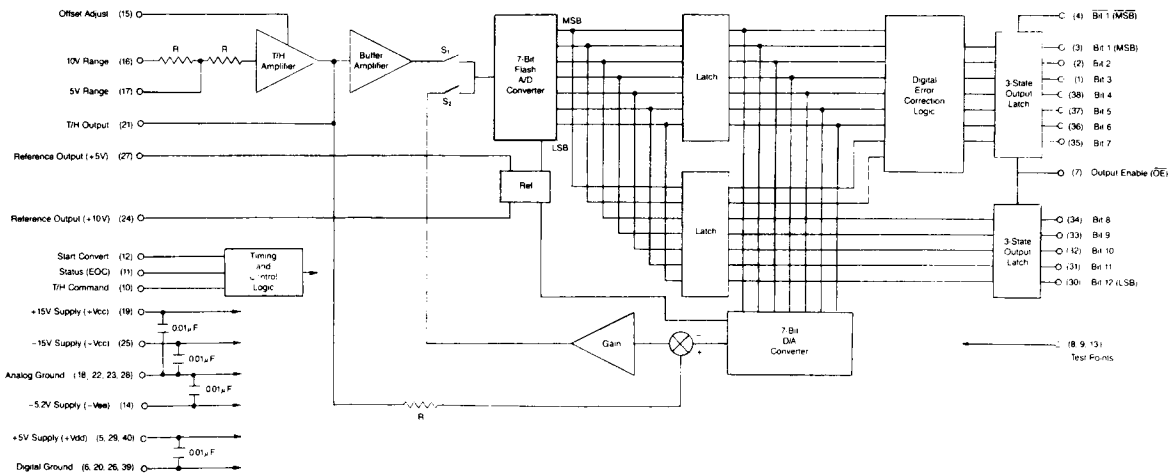
ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V Range		±2.5		Volts
10V Range		±5.0		Volts
Input Impedance (Note 1): Resistance: 5V Range		500		Ω
10V Range		1000		Ω
Capacitance		10		pF
Offset Adjustment Range: 5V Range		±50		mV
10V Range		±100		mV
DIGITAL INPUTS (Start Convert, $\overline{OE}$)				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.7V)			+20	μA
Logic "0" (V_{IL} = +0.4V)			−0.4	mA
DIGITAL OUTPUTS (Parallel, Status, T/H Control, $\overline{MSB}$)				
Output Coding		COB		
		CTC		
Logic Levels: Logic "1" ($I_{source} \leq 100\mu A$)	+2.7			Volts
Logic "0" ($I_{sink} \leq 2mA$)			+0.5	Volts
Leakage Current (B1 - B12 in High-Z State): Logic "1" (V_{OH} = +2.7V)			+10	μA
Logic "0" (V_{OL} = +0.4V)			−10	μA
INTERNAL REFERENCE				
Reference Output (Pin 24): Voltage		+10		Volts
Drift (Note 1)		±10		ppm/°C
Output Current (Notes 1, 2)		2		mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc Supply	±14.5	±15.0	±15.5	Volts
+Vdd Supply	+4.75	+5.0	+5.25	Volts
−Vee Supply	−5.0	−5.2	−5.4	Volts
Power Supply Rejection (Note 3): +Vcc Supply	−50	−65		dB
−Vcc Supply	−50	−70		dB
+Vdd Supply	−35	−50		dB
−Vee Supply	−60	−80		dB
Current Drains: +Vcc Supply		65	75	mA
−Vcc Supply		80	95	mA
+Vdd Supply		210	240	mA
−Vee Supply		50	60	mA
Power Consumption		3485		mW

DYNAMIC CHARACTERISTICS	J	K	S	T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	2	2	2	2	MHz
Maximum A/D Conversion Time (Note 5)	400	400	400	400	nsec
Signal-to-Noise Ratio (SNR, Note 6): Initial (+25°C)	66	68	66	68	dB
T_{min} to T_{max} (Note 11)	64	66	64	66	dB
Harmonics and Spurious Noise (Note 7): Initial (+25°C)	−70	−72	−70	−72	dB
T_{min} to T_{max} (Note 11)	−67	−70	−67	−70	dB
Small Signal Bandwidth	12	12	12	12	MHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C)	1	1	1	1	LSB
T_{min} to T_{max} (Note 11)	1.5	1	1.5	1	LSB
Resolution for No Missing Codes: Initial @+25°C	12	12	12	12	Bits
T_{min} to T_{max} (Note 11)	12	12	12	12	Bits
Bipolar Zero Error (Notes 8, 9): Initial (+25°C)	0.3	0.2	0.3	0.2	%FSR
T_{min} to T_{max}	0.5	0.4	0.5	0.4	%FSR
Full-Scale Accuracy Error (Notes 8, 10): Initial (+25°C)	0.25	0.20	0.25	0.20	%FSR
T_{min} to T_{max} (Note 11)	0.40	0.30	0.40	0.30	%FSR

SPECIFICATION NOTES:

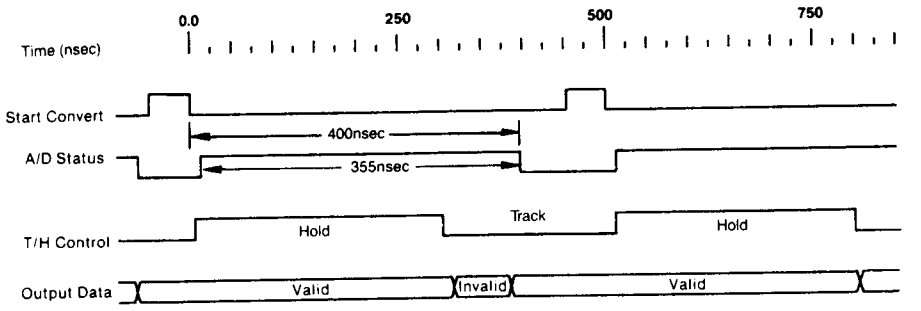
1. This parameter is listed for reference only and is not tested.
2. If the internal reference is used to drive an external load, the load must not change during a conversion.
3. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 or the 0000 0000 0000 to 0000 0000 0001 output transition occurs versus a change in power supply voltage.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 2MHz rate. Obviously, the devices may be operated at lower sampling frequencies if desired.
5. When Status is high, the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input (0dB) sine wave at any frequency up to 941.41 KHz and is specified as a minimum.
7. This parameter represents the highest signal-to-non-fundamental component ratio (harmonic or spurious, in-band or out-of-band) in the output spectrum and is specified as a minimum.
8. Adjustable to zero with an external potentiometer.
9. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 to 1000 0000 0000. The ideal value at which this transition should occur is −½LSB.
10. Full-scale accuracy specifications apply at both positive and negative full-scale and are defined as the differences between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0001 to 0000 0000 0000 for positive full-scale and from 1111 1111 1110 to 1111 1111 1111 for negative full-scale. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full-scale voltage. The latter ideally occurs ½LSB above the nominal negative full-scale voltage.
11. MN6249J and MN6249K are specified for 0°C to +70°C operation. MN6249S, S/B and MN6249T, T/B are fully specified for −55°C to +125°C operation.

BLOCK DIAGRAM



Test Points are connected to internal circuitry and should not be connected to externally.

TIMING DIAGRAM



TIMING DIAGRAM NOTES:

1. Minimum start convert pulse width is 50nsec. The rising edge of start convert resets internal timing circuits ensuring that T/H Control (pin 10) is set to a logic "0" and that the first conversion made upon "powerup" is valid. The falling edge of Start Convert initiates the conversion, and Start Convert must remain low for 350nsec minimum.
2. Status rises to a "1" typically 45nsec after the falling edge of Start Convert.
3. Conversion time is defined as the time from the falling edge of Start Convert to the falling edge of Status and is specified as 400nsec maximum.
4. Digital output data from the previous conversion remains valid typically 280nsec after the falling edge of Start and 235nsec after the rising edge of Status.
5. Digital output data is valid on the falling edge of Status.
6. Output data is enabled and becomes valid a maximum of 50nsec after Output Enable ($\overline{OE}$, pin 7) is brought low.
7. The falling edge of T/H Control occurs 300nsec maximum after the falling edge of Start Convert.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN6249 is a 12-bit, sampling, A/D converter consisting of a high-speed A/D converter and its companion T/H amplifier. The A/D section is a multistage (two-step) A/D converter. It employs the Micro Networks Serial-Parallel conversion technique (sometimes referred to as the subranging technique) with digital error correction. The technique uses two 7-bit flash A/D converters (actually a single 7-bit flash converter is used twice) in a configuration that yields a resolution (12 bits) that is beyond the practical limits of what can be achieved in a single high-resolution flash converter. For a detailed discussion of the Serial-Parallel conversion technique and digital error correction, please refer to the MN5245/5246 data sheet.

The Start Convert signal must be a positive pulse with a minimum pulse width of 50nsec (100nsec maximum if continuously converting at maximum conversion rate) and must remain low during the conversion for a minimum of 350nsec. The rising edge of Start Convert resets the timing logic ensuring that all timing pulses are set to the proper state and that the first conversion following "power on" produces valid digital output data. The falling edge of Start Convert initiates the conversion setting T/H Control Output and Status (E.O.C.) to logic "1's". The T/H Control Output signal remains a logic "1" for 300nsec maximum after the falling edge of Start Convert and returns to a logic "0" when the "analog-processing" portion of the conversion is complete. Status remains a logic "1" for 400nsec maximum after the falling edge of Start Convert. Status returning low signifies that the conversion process is complete and that parallel output data is valid.

The internal T/H amplifier enables the MN6249 to sample and digitize analog input signals while maintaining SNR (rms-signal-to-rms-noise) and harmonic distortion performance specifications. The T/H amplifier's mode of operation is controlled by the internal control logic circuitry. When a conversion is initiated by the falling edge of Start Convert, the T/H amplifier is switched from the track mode to the hold mode, indicated by the T/H Control Output changing from a logic "0" to a logic "1". The internal T/H amplifier remains in the hold mode during the "analog processing" portion of the conversion cycle. Once the analog processing is complete, and the analog input signal no longer needs to be held at a constant value, the T/H is switched to track mode to acquire and track the next analog input signal to be converted (T/H Control Output changes from a logic "1" to a logic "0"). This allows the T/H amplifier's acquisition time to overlay the "digital processing" portion of the conversion cycle.

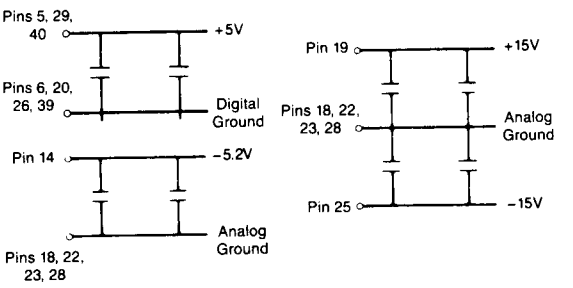
Valid parallel output data is available on the falling edge of Status and remains valid during the next conversion for 280nsec (typ) after the next falling edge of Start Convert. See Timing Diagram. This allows the use of rising and falling edges of either Start Convert or Status for latching output data.

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracy and performance from the MN6249. Analog Ground (pins 18, 22, 23, 28) is not connected internally to Digital Ground (pins 6, 20, 26, 39). All ground pins should be tied together as close to the unit as possible and connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

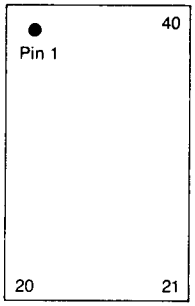
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

A 0.1μF capacitor should be connected from Gain Adjust (pin 27) to system analog ground.



POWER SUPPLY DECOUPLING

PIN DESIGNATIONS



1	Bit 3	40	+5V Supply (+Vdd)
2	Bit 2	39	Digital Ground
3	Bit 1 (MSB)	38	Bit 4
4	$\overline{\text{Bit 1 (MSB)}}$	37	Bit 5
5	+5V Supply (+Vdd)	36	Bit 6
6	Digital Ground	35	Bit 7
7	Output Enable ($\overline{\text{OE}}$)	34	Bit 8
8	T.P.	33	Bit 9
9	T.P.	32	Bit 10
10	T/H Control Output	31	Bit 11
11	Status (EOC)	30	Bit 12 (LSB)
12	Start Convert	29	+5V Supply (+Vdd)
13	T.P.	28	Analog Ground
14	−5.2V Supply (−Vee)	27	Gain Adjust
15	Offset Adjust	26	Digital Ground
16	10V Range	25	−15V Supply (−Vcc)
17	5V Range	24	Reference Output (+10V)
18	Analog Ground	23	Analog Ground
19	+15V Supply (+Vcc)	22	Analog Ground
20	Digital Ground	21	T/H Output

Notes: "Test Points" (T.P.) are connected to internal circuitry and should not be connected to externally.

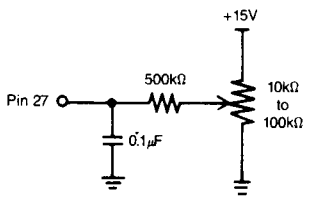
INTERNAL T/H AMPLIFIER — As stated earlier, MN6249's internal T/H amplifier is configured in such a way as to be transparent to the user. The T/H's output is connected directly to the input of the A/D converter, and its operational mode is controlled directly by the internal control logic circuitry. Consequently, users of the MN6249 need not burden themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6249 and are, in fact, impossible to directly test considering that the T/H output and control lines are not accessible at the device pins. The manner in which MN6249 is specified (input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc.) obviates the need for knowing the specific T/H time-domain performance specifications.

Note that the static errors (gain error, track-mode offset error, and pedestal) of the T/H function will add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D-converter offset error. However, when the A/D offset is functionally laser trimmed, it is done at the 2MHz sampling rate with the T/H is in the hold mode. Consequently, all error sources are compensated for. All static errors on MN6249 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

STATUS OUTPUT/DATA VALID—The Status or End of Conversion (E.O.C., pin 11) is set to a logic "1" by the falling edge of Start Convert; remains high during the conversion; and is set to a logic "0" when the conversion is complete. Digital output data is valid on the falling edge of Status and remains valid 280nsec after Start Convert goes low initiating the next conversion. When making successive conversions, any of the edges occurring during the beginning of the data-valid period (fall of Status, falling edge of the next Start Convert, rising edge of Status, etc.) are best suited for this purpose. Also, output data can be enabled during this data-valid period by bringing Output Enable ($\overline{\text{OE}}$, pin 7) low. The delay from the falling edge of $\overline{\text{OE}}$ to output data enabled is 50nsec maximum.

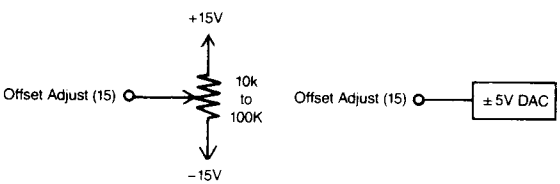
GAIN ADJUST — Pin 27 on MN6249 serves a unique function. The device's internal +5V ±2% reference is brought out at this point and can be used to drive external loads. If used for this purpose, pin 27 should be buffered with a FET-input device as drawing more than 5μA from the internal reference will affect MN6249 accuracy and linearity. Pin 27 can also be used as a Reference In point if it is necessary to operate MN6249 from an external reference. An application requiring an external reference might be one in which it is necessary to have a number of devices operate from the same reference in order to track each other in changing temperatures. The applied reference should be +5V ±250mV.

Pin 27 also functions as the gain-adjust point for MN6249. Gain adjustment is accomplished using a 10kΩ to 100kΩ trimming potentiometer and a 500kΩ series resistor as shown below. The series resistor can be ±20% carbon composition or better. The multiturn potentiometer should have a TCR of 100ppm/°C or less to minimize drift with temperature. Gain adjusting is normally accomplished by applying the analog input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition is ideally supposed to take place and adjusting the pot until the transition is observed.



Gain Adjust Range= ±0.2% FSR

OFFSET ADJUST — Initial offset error of the MN6249 can be adjusted to zero by applying a voltage to Offset Adjust (pin 15). A 50μΩ resistor is connected from Offset Adjust (pin 15) to the internal T/H amplifier's summing junction. This allows the output of a voltage-output DAC or the wiper of a potentiometer to be connected directly to Offset Adjust (pin 15).



ORDERING INFORMATION

Part Number	Specified Temperature Range	No Missing Codes Over Temp.	Integral Linearity Over Temp.	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
MN6249J	0°C to +70°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	–70dB
MN6249K	0°C to +70°C	12 Bits	±1LSB	2MHz	1MHz	68dB	–72dB
MN6249S	–55°C to +125°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	–70dB
MN6249S/B[1]	–55°C to +125°C	12 Bits	±1.5LSB	2MHz	1MHz	66dB	–70dB
MN6249S/B CH[2]	–55°C t0 +125°C	12 Bits	±1.5LSB	2MHz	1MHz	68dB	–70dB
MN6249T	–55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	–72dB
MN6249T/B[1]	–55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	–72dB
MN6249T/B CH[2]	–55°C to +125°C	12 Bits	±1LSB	2MHz	1MHz	68dB	–72dB

1. Includes Environmental Stress Screening.
2. Fully compliant to MIL-H-38534.

DIGITAL OUTPUT CODING

Analog Input		Digital Output	
±5V	±2.5V	MSB	LSB
–5.0000	–2.5000	1111 1111 1111	
–4.9988	–2.4994	1111 1111 111Ø*	
–0.0036	–0.0018	1000 0000 000Ø*	
–0.0012	–0.0006	ØØØØ ØØØØ ØØØØ*	
+0.0012	+0.0006	0111 1111 111Ø*	
+4.9964	+2.4982	0000 0000 000Ø*	
+5.0000	+2.5000	0000 0000 0000	

NOTES:

1. For a 12-bit converter with a 5 Volt FSR, 1LSB=1.22mV. For a 12-bit converter with a 10 Volt FSR, 1LSB=2.44mV.
2. Coding is complementary offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.