M5M5260AP, AJ-25, -30, -35

262144-BIT(262144-WORD BY 1-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M5260A is a family of 262144-word by 1-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They includes a power-down feature as well.

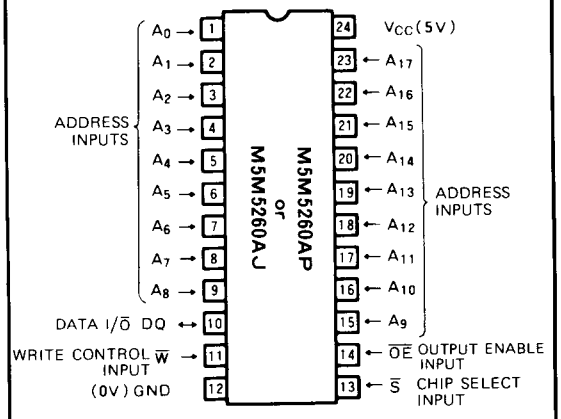
FEATURES

- Fast access time M5M5260AP, AJ-25 . . . . 25ns (max)
  M5M5260AP, AJ-30 . . . . 30ns (max)
  M5M5260AP, AJ-35 . . . . 35ns (max)
- Low powder dissipation
  Active . . . . . 300mW (typ)
  Stand by . . . . . 5mW (typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- $\overline{OE}$ prevents data contention in the I/O bus

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 24P4Y (DIP)
24P0J (SOJ)

FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

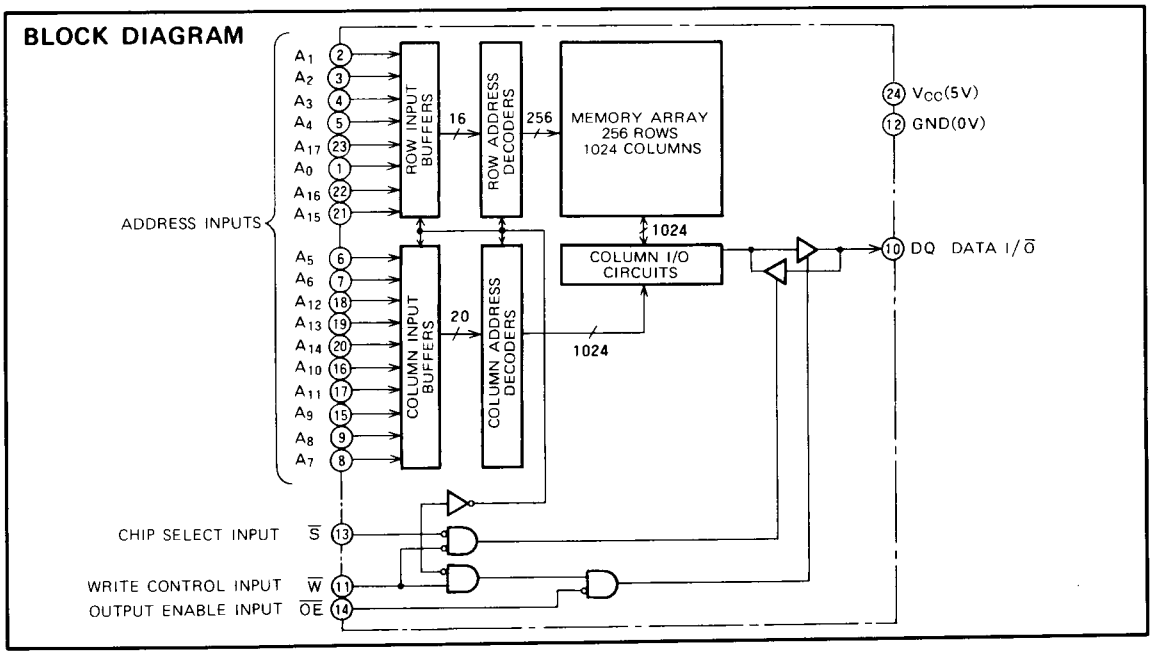
In a read operation, after setting $\overline{W}$ to high $\overline{S}$ and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	−3.5* ~ 7	V
V_I	Input voltage		−3.5* ~ 7	V
V_O	Output voltage		−3.5* ~ 7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		−0 ~ 70	°C
Tstg(bias)	Storage temperature (bias)		−10 ~ 85	°C
Tstg	Storage temperature		−65 ~ 150	°C

* Pulse width = 20 ns, In case of DC: −0.5V

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−3*		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}+0.3	V

* Pulse width = 20 ns, In case of DC: −0.5V

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0 ~ V_{CC}				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O = 0 ~ V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})} = V_{IL}$ Output open	AC (minimum cycle)			140	mA
			DC		60	75	mA
I_{CC2}	Stand by current	$V_{I(\overline{S})} = V_{IH}$	AC (minimum cycle)			40	mA
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			30	mA
I_{CC3}	Stand by current	$V_{I(\overline{S})} \geqq V_{CC}$ − 0.2V Other $V_I \leqq$ 0.2V or $V_I \geqq V_{CC}$ − 0.2V			1	10	mA
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz				5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz				7	pF

Note 1. Current flow into an IC is positive, out is negative.
* Pulse width = 20 ns, In case of DC: −0.5V

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

MEASUREMENT CONDITIONS

Input pulse levels . . . . . V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time 5ns
Input timing reference level 1.5V
Output timing reference level . . V_{OH} = 2V, V_{OL} = 0.8V
Output loads . . . . . Fig. 1, Fig. 2

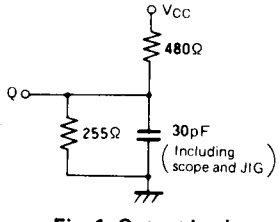


Fig. 1 Output load

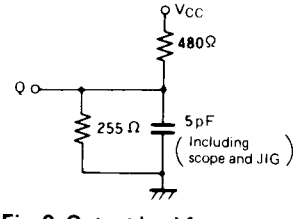


Fig. 2 Output load for t_{en}, t_{dis}

READ CYCLE

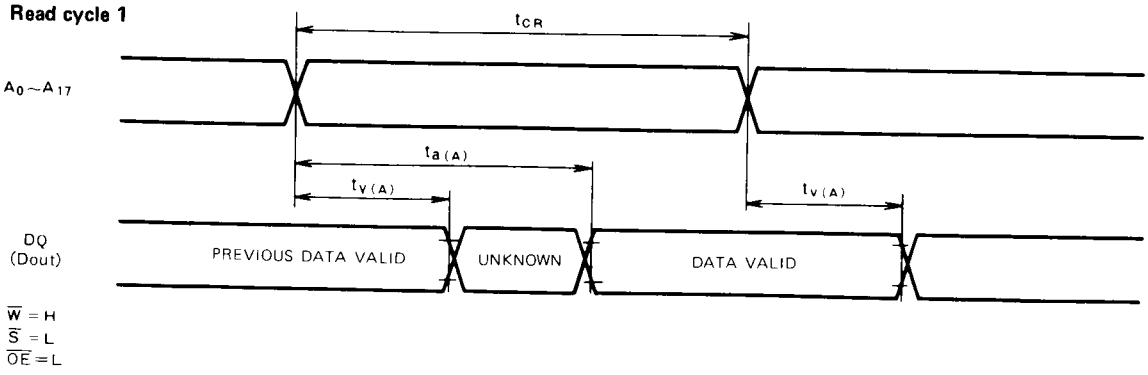
Symbol	Parameter	M5M5260A-25			M5M5260A-30			M5M5260A-35			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	25			30			35			ns
$t_{a(A)}$	Address access time			25			30			35	ns
$t_{a(S)}$	Chip select access time			25			30			35	ns
$t_{a(OE)}$	Output enable access time			15			20			25	ns
$t_{v(A)}$	Data valid time after address	3			5			5			ns
$t_{en(S)}$	Chip selection to output active	0		15	0		15	0		20	ns
$t_{dis(S)}$	Output disable time from CS	3			5			5			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0			0			0			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		10	0		10	0		15	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power down time after chip deselection			25			30			35	ns

WRITE CYCLE

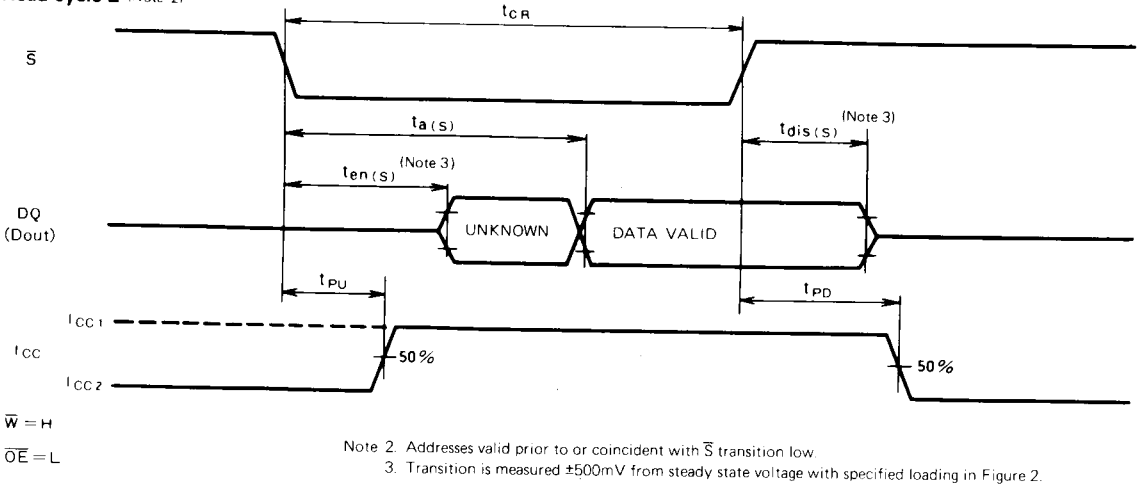
Symbol	Parameter	M5M5260A-25			M5M5260A-30			M5M5260A-35			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	25			30			35			ns
$t_{su(S)}$	Chip select setup time	20			20			25			ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0			0			0			ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0			0			0			ns
$t_{w(W)}$	Write pulse width	10			15			15			ns
$t_{rec(W)}$	Write recovery time	3			3			5			ns
$t_{su(D)}$	Data setup time	15			15			15			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time from W	0		10	0		10	0		15	ns
$t_{en(W)}$	Output enable time from W	0			0			0			ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	15			20			25			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0			0			0			ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	0			0			0			ns

TIMING DIAGRAMS

Read cycle 1

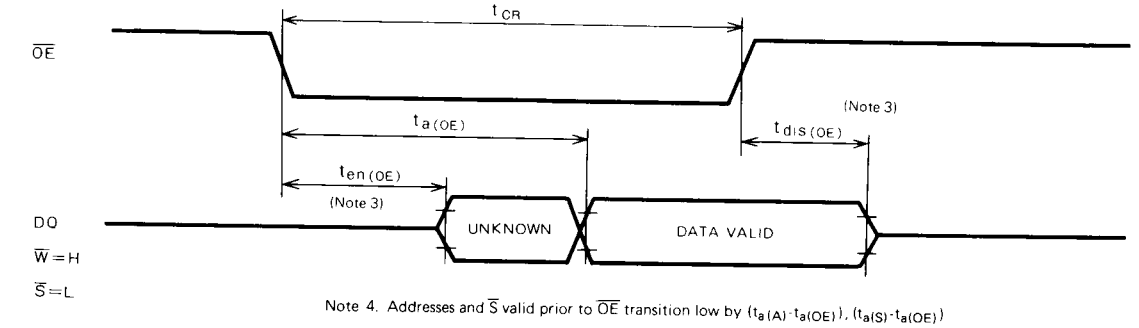


Read cycle 2 (Note 2)



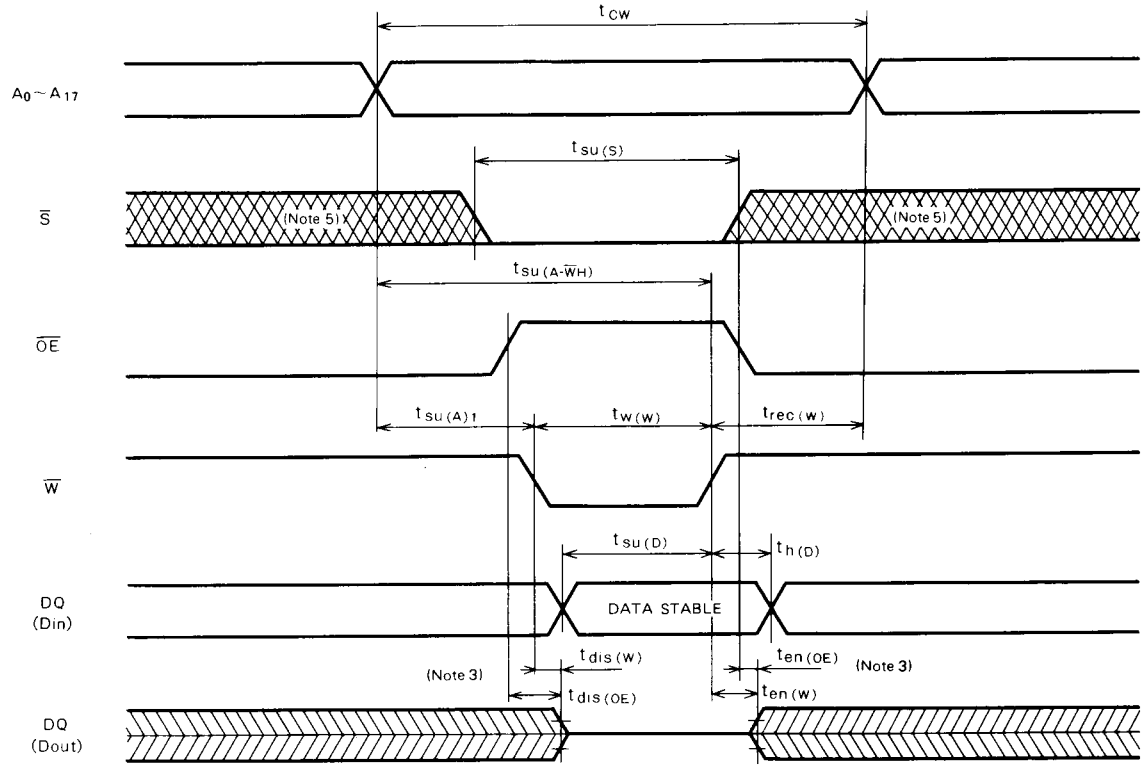
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 4)

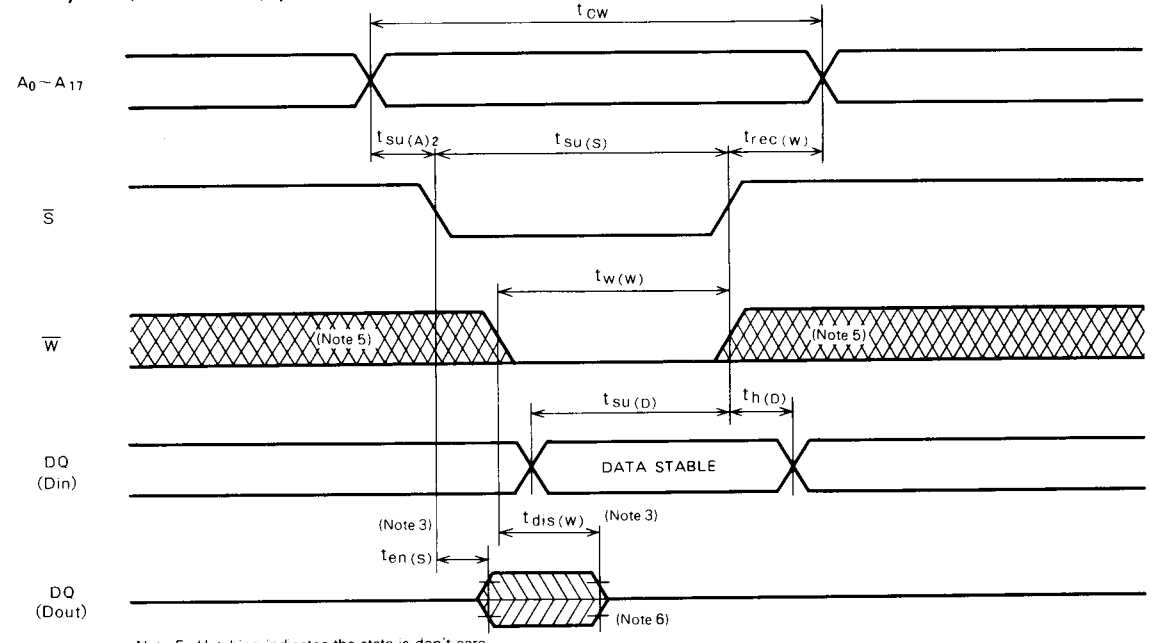


Note 4. Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by $(t_{a(A)}-t_{a(OE)})$, $(t_{a(S)}-t_{a(OE)})$

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 5. Hatching indicates the state is don't care.
6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.