KS54AHCT 182
KS74AHCT

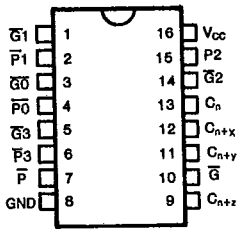
Look Ahead Carry Generator

FEATURES

- **Compatible Carry Functions for direct ALU connection**
- **Cascadable to perform look-ahead across n-bit adders.**
- **High output current drive: I_{OL} = 8mA @ V_{OL} = 0.5V**
- **Low power consumption characteristic of CMOS**
- **Direct interface capability to TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**

  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

PIN CONFIGURATION



DESCRIPTION

The '182 is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or group of adders. These devices can be cascaded to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjuction with the AHCT181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true from, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 182 are:

$$C_{n+x} = G0 + P0\ Cn$$
$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ Cn$$
$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$
$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

PIN DESIGNATIONS

Designation	Pin No	Function
$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	3,1,14,5	Active Low Carry Generate Inputs
$\overline{P0}$,$\overline{P1}$,$\overline{P2}$,$\overline{P3}$	4,2,15,6	Active Low Carry Propagate Inputs
Cn	13	Carry Input, Active HIGH
Cn+x, Cn+y, Cn+z	12,11,9	Carry Outputs
$\overline{G}$	10	Active Low Carry Generate Output
$\overline{P}$	7	Active Low Carry Propagae Output
V_{CC}	16	Supply Voltage
GND	8	Ground

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FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR C_n+x OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_n+x
L	X	X	H
X	L	H	H
All other combinations			L

Cn+y OUTPUT

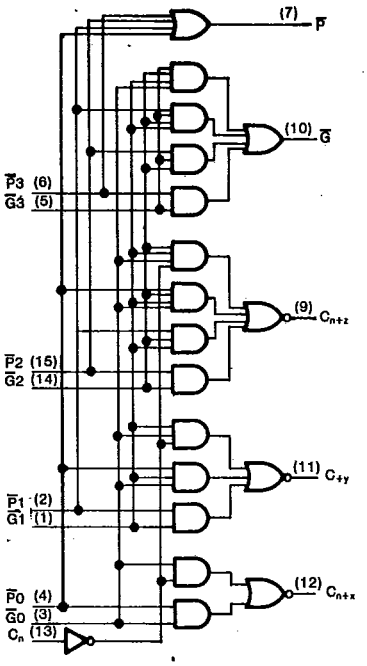
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

Cn+z OUTPUT

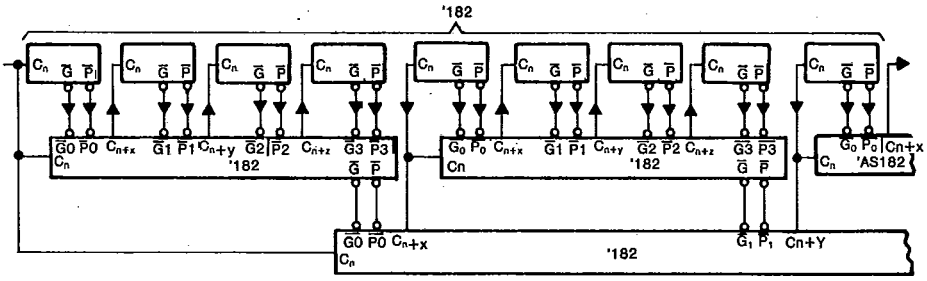
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high-level, L = low level, X = don't care
Any inputs not shown in a given table are don't care with respect to that output.

LOGIC DIAGRAM



Figure; THE '182 IN A 64-BIT LOOK-AHEAD CARRY CIRCUIT



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Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74AHCT T_a = −40°C to +85°C	KS54AHCT T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤2 ns), AHCT182

Characteristic	Symbol	Conditions†	T_a = 25°C, V_{CC} = 5.0V	KS74AHCT T_a = −40°C to +85°C, V_{CC} = 5.0V ± 10%		KS54AHCT T_a = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, $\overline{Pi}$ or $\overline{Gi}$ to $C_{n+x}C_{n+y}$, C_{n+z}	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, $\overline{Pi}$ or $\overline{Gi}$ to $\overline{G}$	t_{PLH}	C_L=50pF	12		20		24	ns
	t_{PHL}		12		20		24	
Propagation Delay, C_n to C_{n+x}, C_{n+y}, C_{n+z}	t_{PLH}	C_L=50pF	15		21		26	ns
	t_{PHL}		15		21		26	
Propagation Delay $\overline{Pi}$ to $\overline{P}$	t_{PLH}	C_L=50pF	11		18		21	ns
	t_{PHL}		11		18		21	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}							pF

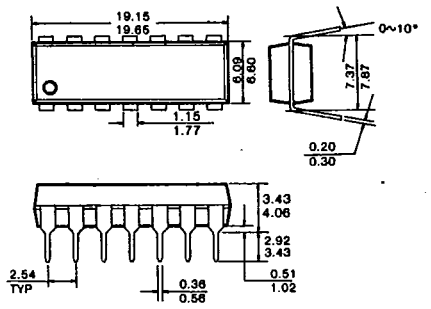
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

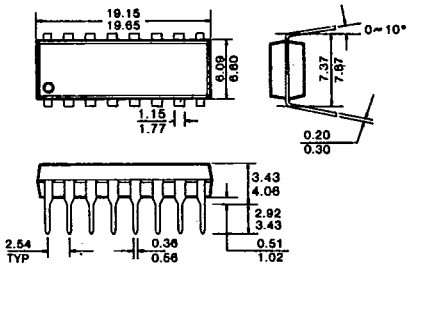
T-90-20

1. PLASTIC PACKAGES

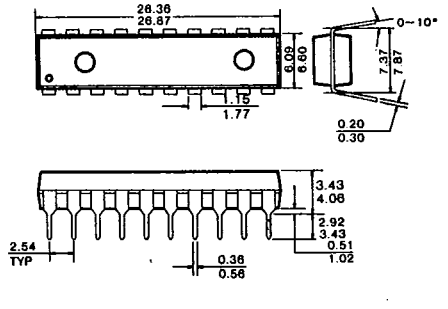
14-Pin Plastic DIP **Units: mm**



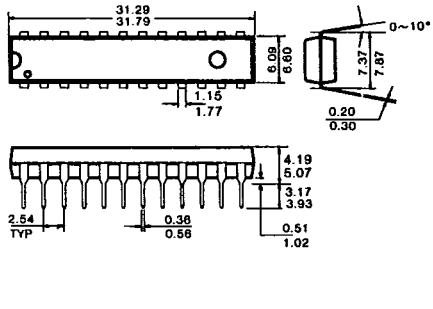
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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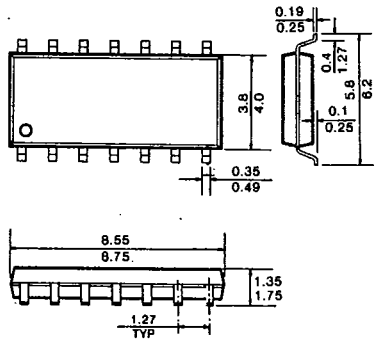
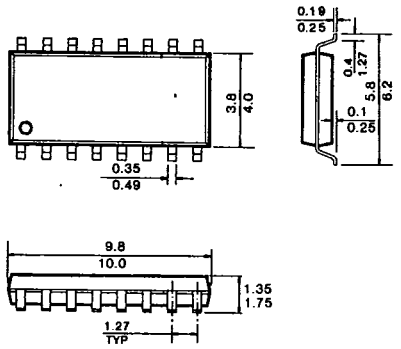
14-Pin SOP

Unit: mm



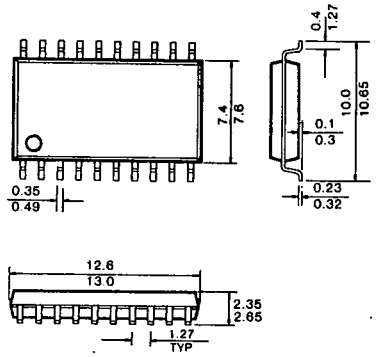
16-Pin SOP

Unit: mm



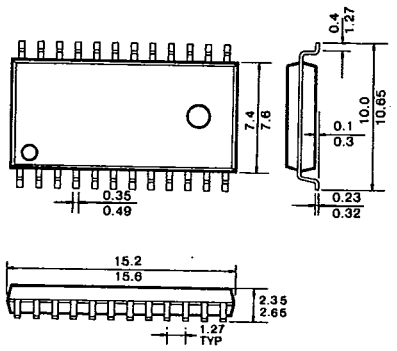
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

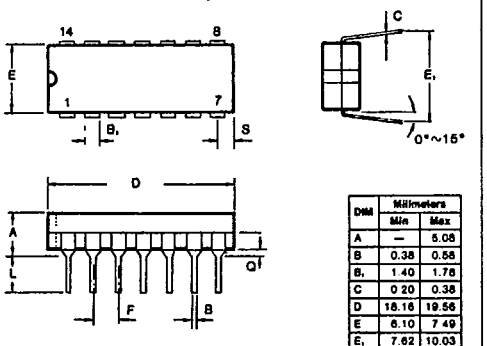


PACKAGE DIMENSIONS

T-90-20

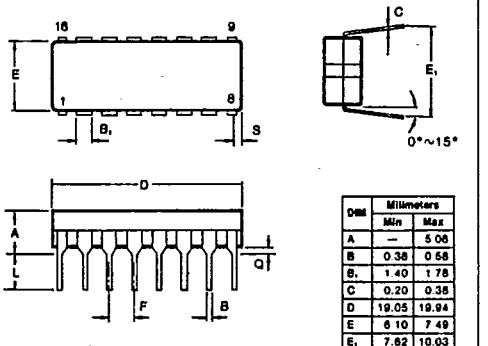
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



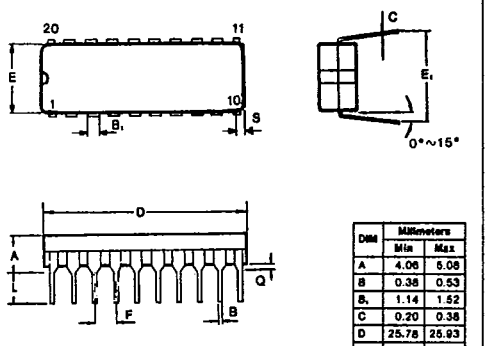
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



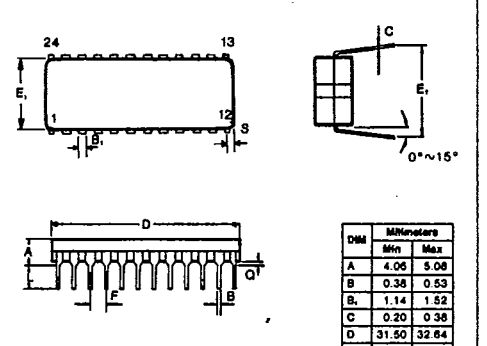
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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