32,768 WORD×9 Bit High Speed BiCMOS Static RAM

FEATURES

- **Fast Access Time: 8, 9, 10, 12ns (Max.)**
- **Low Power Dissipation**
  - **Standby (TTL) : 110mA (max.)**
  - **(CMOS): 20mA (max.)**
  - **Operating KM69B257AJ-8: 185mA (Max.)**
  - **KM69B257AJ-9: 185mA (Max.)**
  - **KM69B257AJ-10: 175mA (Max.)**
  - **KM69B257AJ-12: 165mA (Max.)**
- **Single 5V ± 10% Power Supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Three State Outputs**
- **Standard Pin Configuration**
  - **KM69B257AJ: 32-pin SOJ (300 mil)**

GENERAL DESCRIPTION

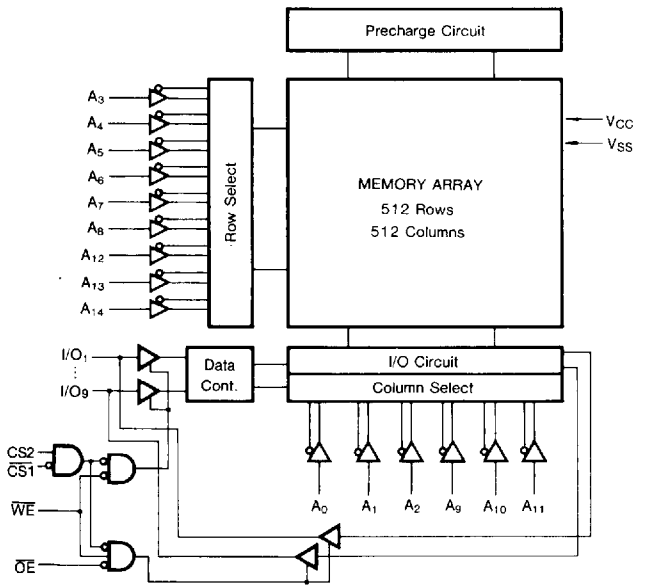
The KM69B257A is a 294,912-bit ultra high-speed Static Random Access Memory organized as 32,768 words by 9 bits. The device is manufactures using Samsung's advanced BiCMOS process.

The KM69B257A has an output enable pin which operates faster than address access time at read cycle.

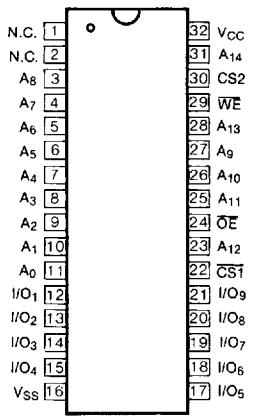
The KM69B257A has been designed for high speed applications. It is particulary well suited for applications requiring high speed, local instruction cache large byte wide cache, or very fast data buffering in personal computers, workstations, and communications. The parity (9th) bit markes the KM69B257A ideal for OLTP system, and i486 based system.

The KM69B257A is packaged in a 300 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS (Top View)



Pin Name	Pin Function
A_0-A_{14}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS_1}$, CS_2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1-I/O_9	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5**	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

* V_{IL} (min.) = −2.0V ac (pulse width ≤ 8ns) for I ≤ 20mA
** V_{IH} (max.) = V_{CC} +2V ac (pulse width ≤ 8ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Item	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or WE=V_{IL}, V_{OUT}=Vss to Vcc		—	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS1}$=V_{IL}, CS2=V_{IH} I_{OUT}=0mA	8ns	—	185	mA
			9ns	—	185	mA
			10ns	—	175	mA
			12ns	—	165	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or CS2=V_{IL} V_{IN}=V_{IH}/V_{IL}, Min. Cycle		—	2	mA
	I_{SB1}	$\overline{CS1}$ ≥ Vcc-0.2V, or CS2 ≤ 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ Vcc−0.2V		—	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA		2.4	—	V

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note: Capacitance is sampled and not 100% tested.

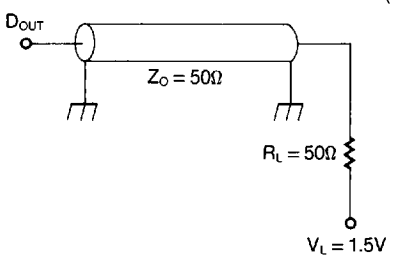
AC CHARACTERISTICS

TEST CONDITIONS

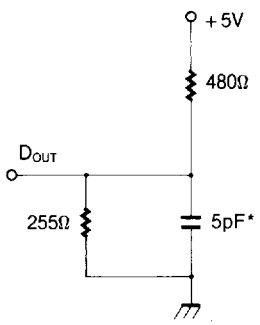
(T_A = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{OLZ}, t_{OHZ}, t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



READ CYCLE

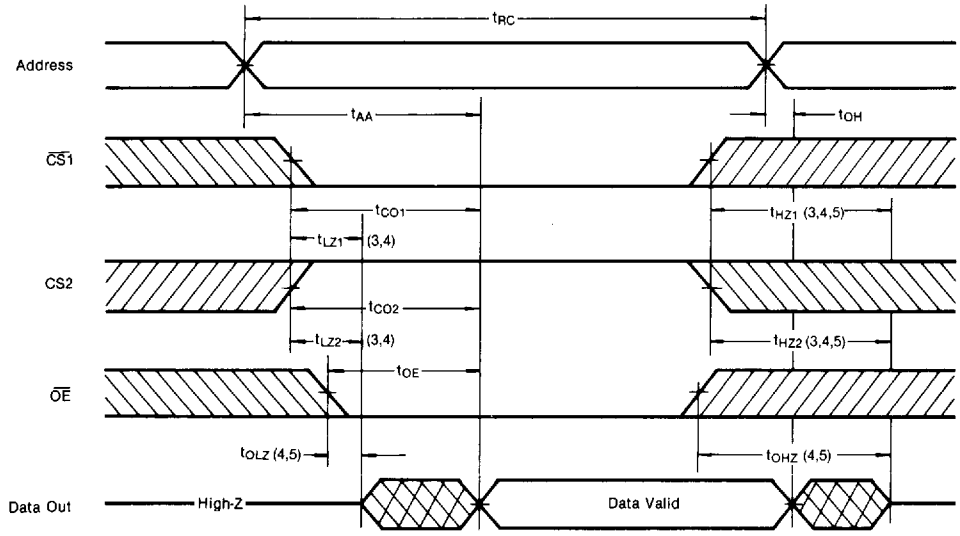
Parameter	Symbol	KM69B257A-8		KM69B257A-9		KM69B257A-10		KM69B257A-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8		9		10		12		ns
Address Access Time	t_{AA}		8		9		10		12	ns
Chip Select to Output	t_{CO1}, t_{CO2}		8		9		10		12	ns
Output Enable to Valid Output	t_{OE}		4		5		5		6	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	3		3		3		3		ns
Output Enable to Low-Z Output	t_{OLZ}	0		0		0		0		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	4	0	5	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns

WRITE CYCLE

Parameter	Symbol	KM69B257A-8		KM69B257A-9		KM69B257A-10		KM69B257A-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8		9		10		12		ns
Chip Select to End of Write	t_{CW}	6		7		7		9		ns
Address Set-up Time	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	6		7		7		9		ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6		7		7		9		ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP}	8		9		10		12		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}	0	4	0	5	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4		5		5		6		ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	3		3		3		3		ns

TIMING DIAGRAMS

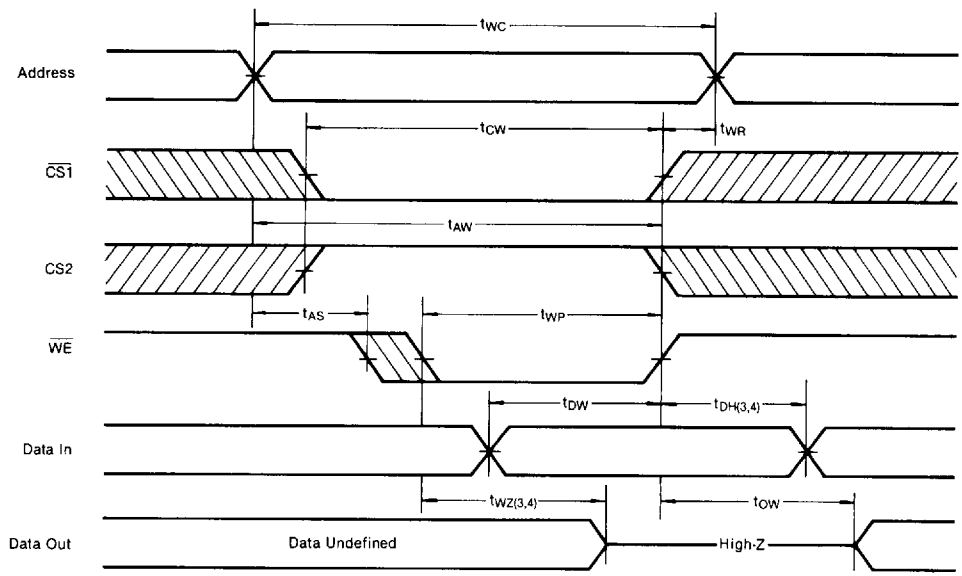
TIMING WAVEFORM OF READ CYCLE



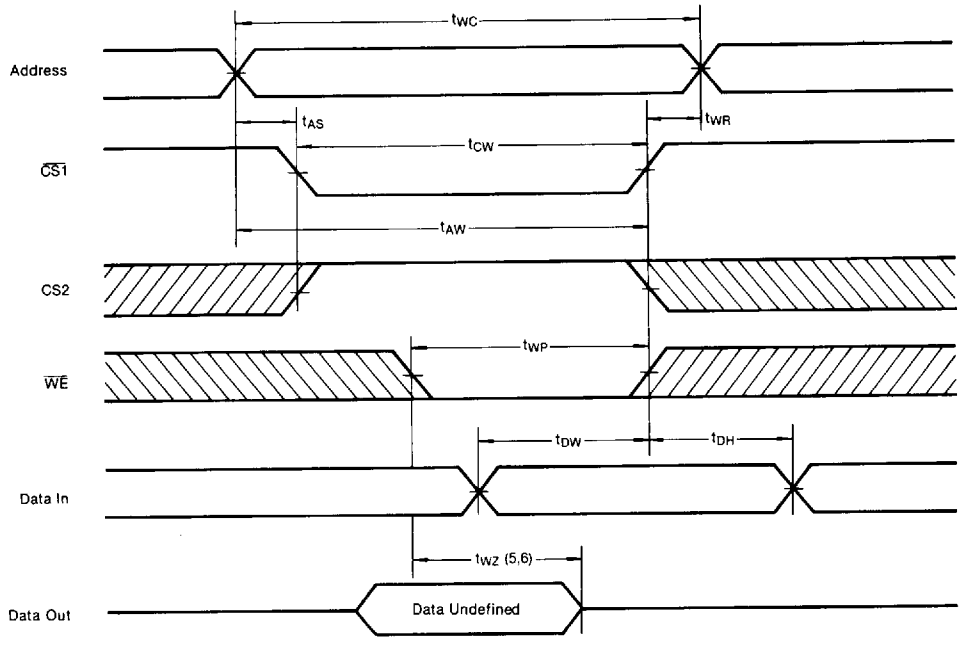
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.

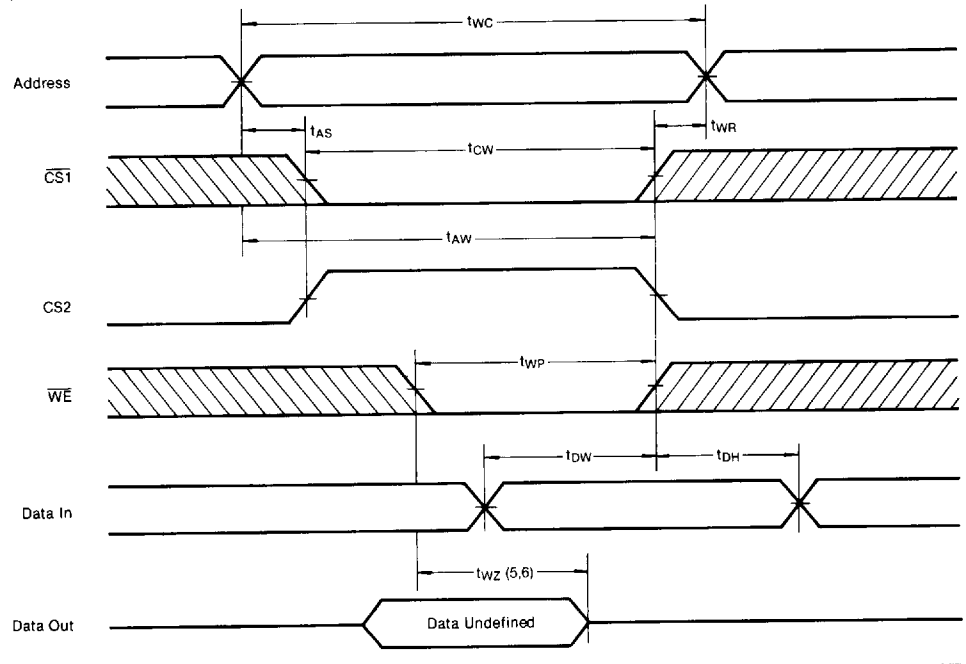
TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}$, $\overline{CS1}$,CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
9. **For common I/O applications, minimization or elimination of bus contention conditions is neessary during read and write cycles.**

FUNCTIONAL DESCRIPTION

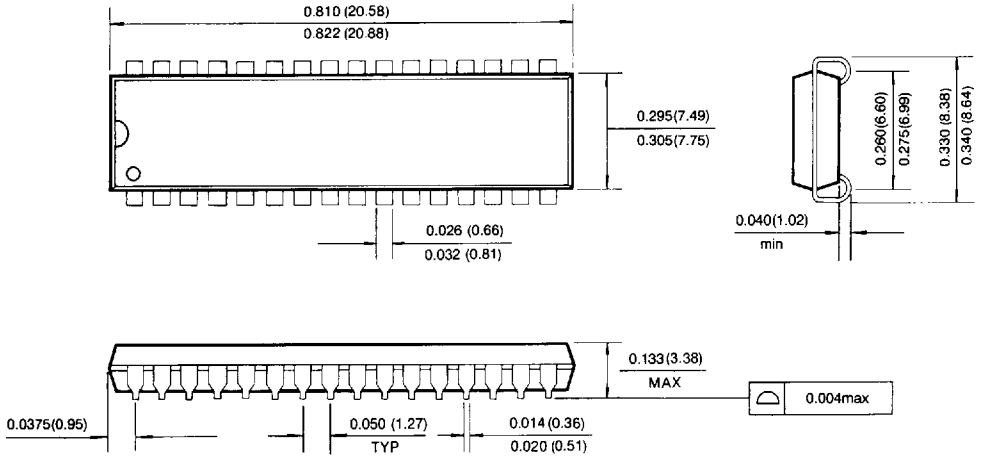
$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
X	L	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

PACKAGE DIMENSIONS

32 PIN SMALL OUT LINE J FORM PACKAGE (300mil)

Unit: Inches (millimeters)



*Note: Do not include mold protrusion