MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM411000
MCM41L1000

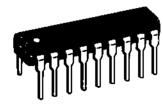
2

1M x 1 CMOS Dynamic RAM
Page Mode

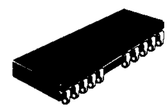
The MCM411000 is a 1.0µ CMOS high-speed dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM411000 requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300 mil dual-in-line plastic package (DIP) and a 300 mil SOJ plastic package.

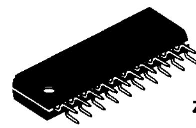
- Three-State Data Output
- Common I/O with Early Write
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM411000 = 8 ms
  MCM41L1000 = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC})
  MCM411000-70 and MCM41L1000-70 = 70 ns (Max)
  MCM411000-80 and MCM41L1000-80 = 80 ns (Max)
- Low Active Power Dissipation:
  MCM411000-70 and MCM41L1000-70 = 440 mW (Max)
  MCM411000-80 and MCM41L1000-80 = 385 mA (Max)
- Low Standby Power Dissipation:
  MCM411000 and MCM41L1000 = 11 mW (Max, TTL Levels)
  MCM411000 = 5.5 mW (Max, CMOS Levels)
  MCM41L1000 = 1.65 mW (Max, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707B-01



J PACKAGE
300 MIL SOJ
CASE 822B-01



Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A-01

PIN NAMES

A0 – A9	Address Inputs
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

DUAL-IN-LINE

D	1	18	V_{SS}
$\overline{W}$	2	17	Q
$\overline{RAS}$	3	16	$\overline{CAS}$
TF	4	15	A9
A0	5	14	A8
A1	6	13	A7
A2	7	12	A6
A3	8	11	A5
V_{CC}	9	10	A4

SMALL OUTLINE

D	1	26	V_{SS}
$\overline{W}$	2	25	Q
$\overline{RAS}$	3	24	$\overline{CAS}$
TF	4	23	NC
NC	5	22	A9
A0	9	18	A8
A1	10	17	A7
A2	11	16	A6
A3	12	15	A5
V_{CC}	13	14	A4

ZIG-ZAG IN-LINE

A9	1	2	$\overline{CAS}$
Q	3	4	V_{SS}
D	5	6	$\overline{W}$
$\overline{RAS}$	7	8	TF
NC	9	10	NC
A0	11	12	A1
A2	13	14	A3
V_{CC}	15	16	A4
A5	17	18	A6
A7	19	20	A8

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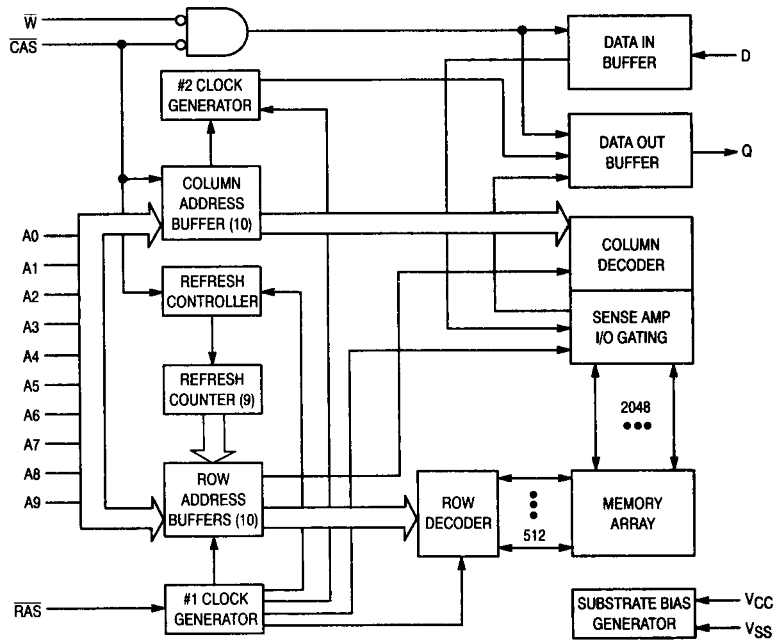
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Test Function Input Voltage	$V_{in(TF)}$	– 1 to V_{CC} + 0.5 V	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

2

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V
Test Function Input Voltage	$V_{IH(TF)}$	– 1.0	—	V_{CC} + 0.5	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns	I_{CC1}	— —	80 70	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycle MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns	I_{CC3}	 — —	 80 60	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle MCM411000-70 and MCM41L1000-70, t_{PC} = 50 ns MCM411000-80 and MCM41L1000-80, t_{PC} = 55 ns	I_{CC4}	 — —	 70 50	mA	1, 3, 4
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM411000 MCM41L1000	I_{CC5}	— —	1.0 300	mA µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM411000-70 and MCM41L1000-70, t_{RC} = 140 ns MCM411000-80 and MCM41L1000-80, t_{RC} = 160 ns	I_{CC6}	 — —	 70 60	mA	1
V_{CC} Power Supply Current, Battery Back-Up Mode — MCM41L1000 only (t_{RC} = 125 µs; t_{RAS} = 1 µs, $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A9, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	3
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable)	I_{CC8}	—	5	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Measured with one address transition per page mode cycle.
4. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	D, A0 – A9	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	
Output Capacitance	Q	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM411000-70 MCM41L1000-70		MCM411000-80 MCM41L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	140	—	160	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	165	—	190	—	ns	7
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	75	—	85	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	ns	7, 8
Access Time from $\overline{CAS}$ (Typ. = 16 ns @ 70°C)	t_{CELQV}	t_{CAC}	—	20	—	25	ns	7, 9
Access Time from Column Address	t_{AVQA}	t_{AA}	—	35	—	40	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	50	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	12
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	25	10,000	ns	13
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	22	55	ns	14
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	17	40	ns	15
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	12	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	40	—	42	—	ns	16

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be either at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
7. Measured with a current load equivalent to 2 TTL (–200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \le t_{RCD}$ (max).
9. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
10. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Transition times are measured between V_{IH} and V_{IL}.
13. t_{RASP} is determined by the $\overline{RAS}$ pulse width in the fast page mode cycle.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled by t_{AA}.
16. t_{AR}, t_{WCR} and t_{DHR} referenced to t_{RAD} (min)

READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM411000-70 MCM41L1000-70		MCM411000-80 MCM41L1000-80		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	17
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	—	10	—	ns	17
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	40	—	42	—	ns	16
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	18, 19
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	ns	18, 19
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	40	—	42	—	ns	16
Refresh Period MCM411000 MCM41L1000	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	19, 20
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	—	25	—	ns	20
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	—	80	—	ns	20
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	—	40	—	ns	20
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	15	—	20	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	10	—	10	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{REHCEH}	t_{RHCP}	45	—	50	—	ns	

NOTES:

17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
19. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
20. t_{WCS} is not a restrictive operating parameter; it is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

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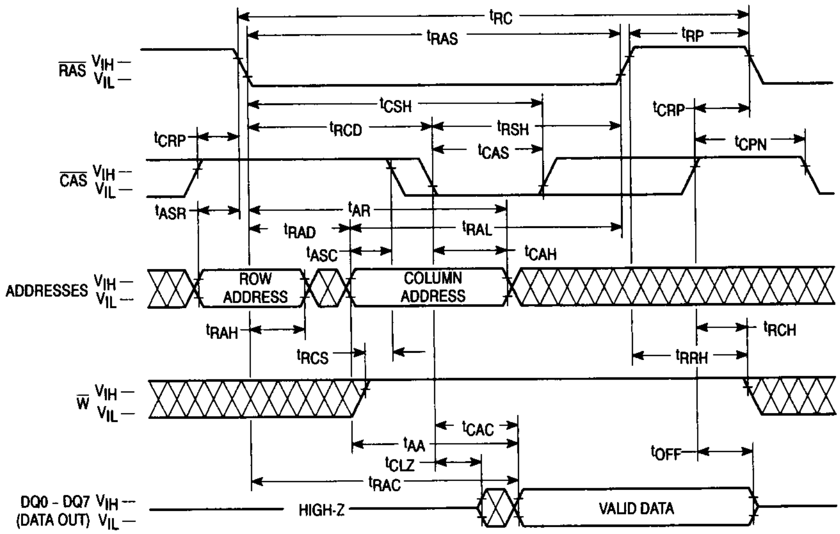
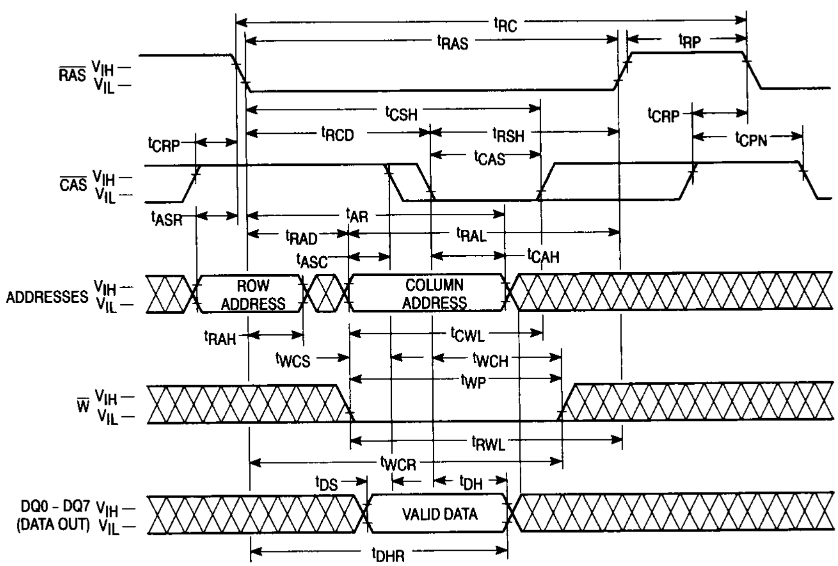
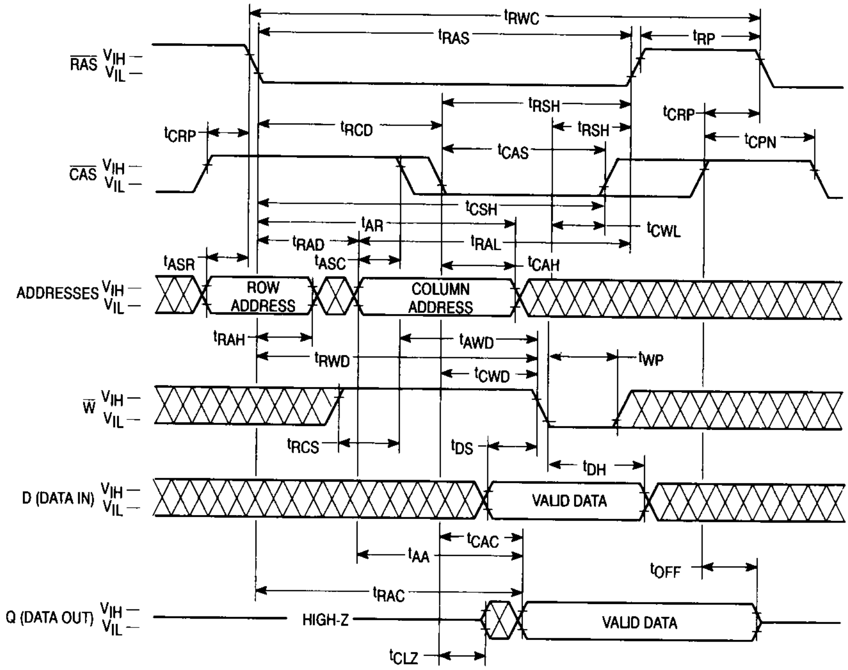
READ CYCLE



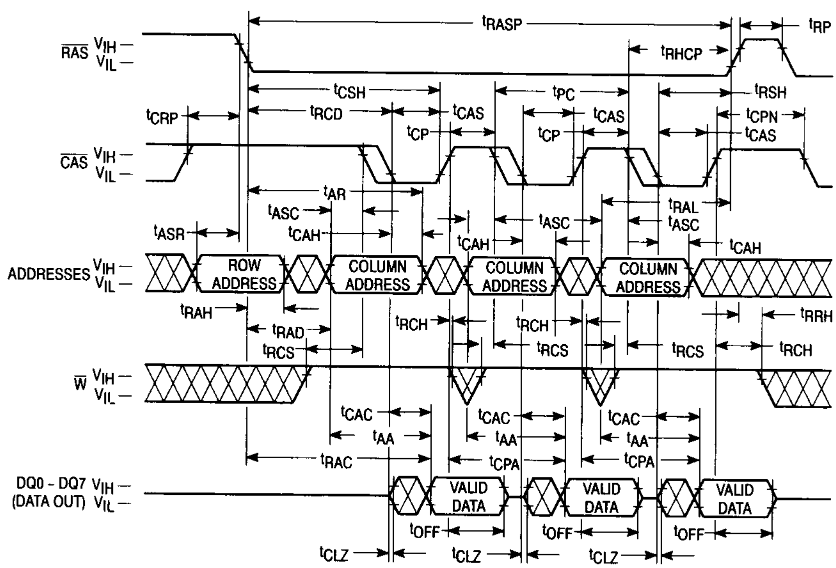
EARLY WRITE CYCLE



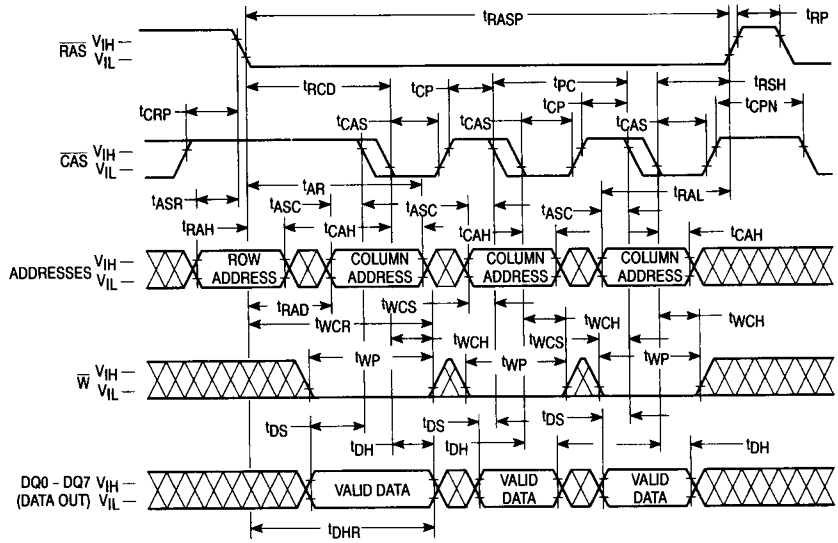
READ-WRITE CYCLE



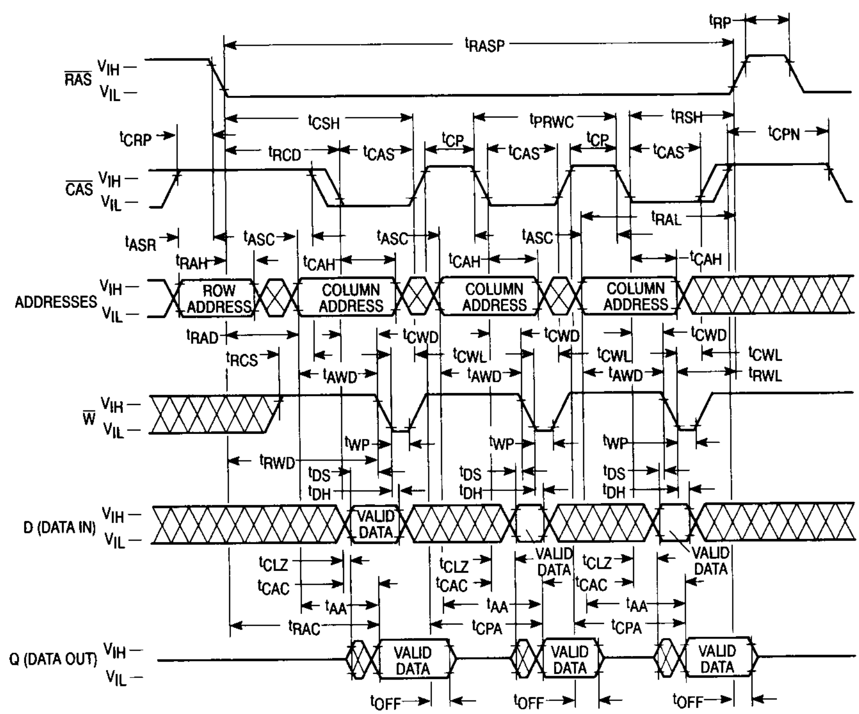
FAST PAGE MODE READ CYCLE



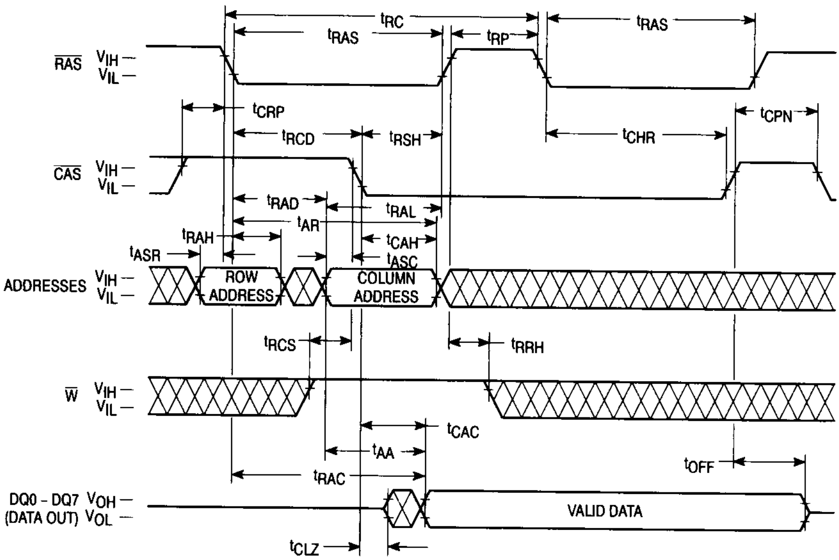
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



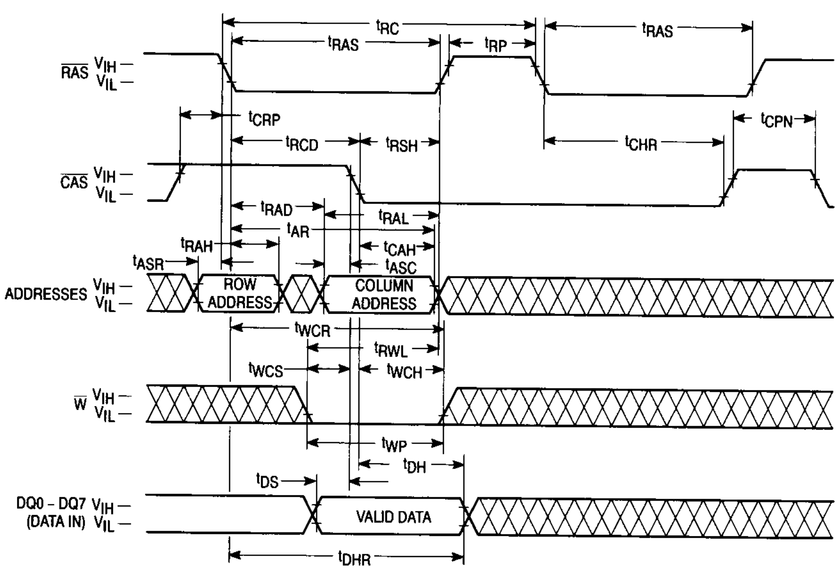
FAST PAGE MODE READ-WRITE CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



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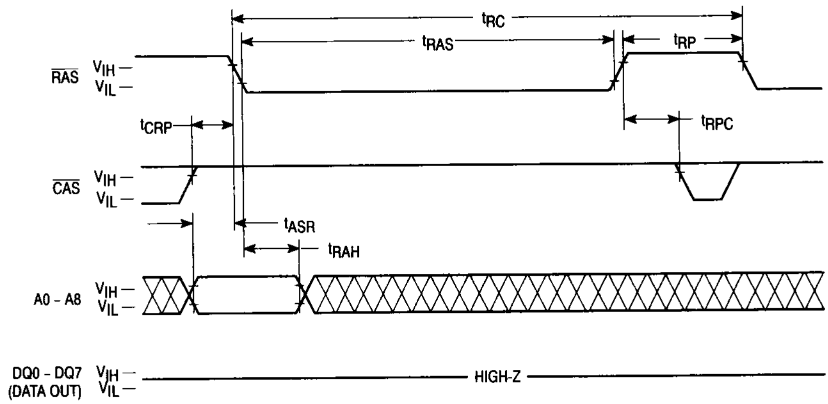
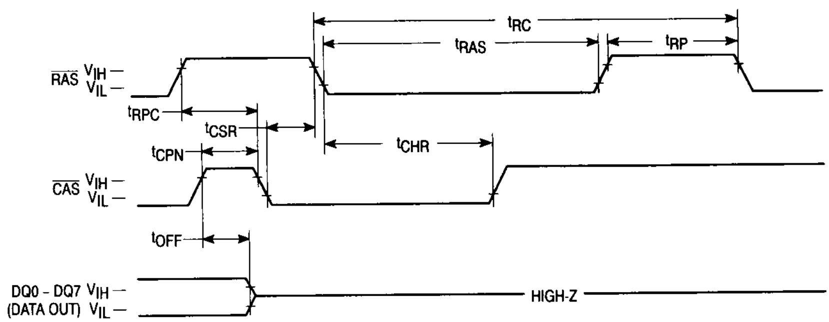
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A8 are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 – A8 are Don't Care)



DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$-only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follows.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read modes.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate — see note 20 of AC Operating Conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the 1M dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). A read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). The operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}.

2

Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM411000 require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM411000. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM411000 and 64 milliseconds on the MCM41L1000.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh**, **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

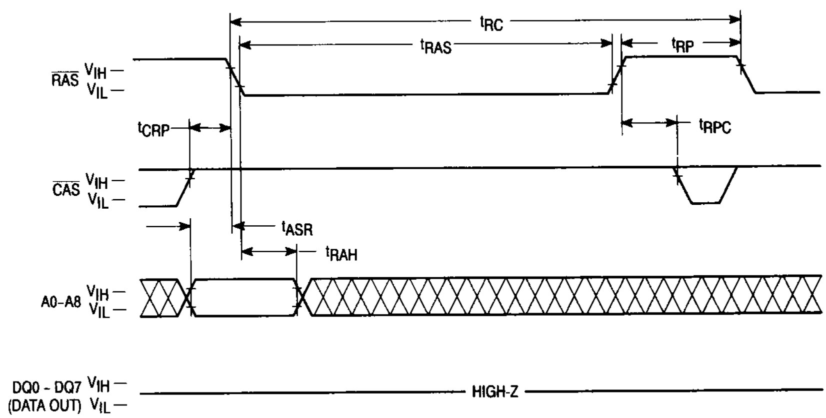
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
($\overline{\text{W}}$ and A8 are Don't Care)



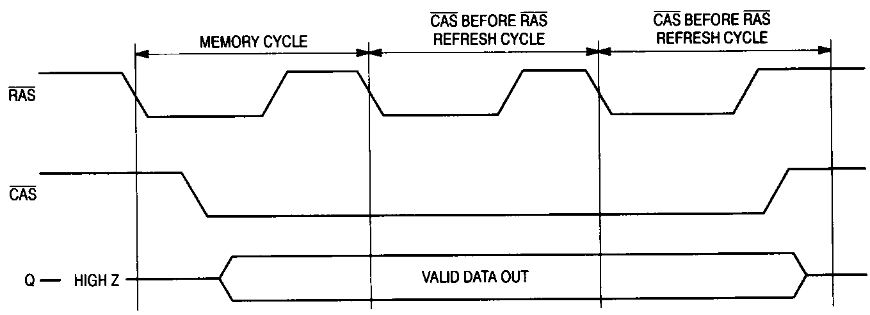


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 411000 or 41L1000 X XX XX

- MCM — Motorola Memory Prefix
- 411000 or 41L1000 — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ, Z = Plastic ZIP)
- XX — Speed (70 = 70 ns, 80 = 80 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM411000P70	MCM411000J70	MCM411000J70R2	MCM411000Z70
MCM411000P80	MCM411000J80	MCM411000J80R2	MCM411000Z80
MCM41L1000P70	MCM41L1000J70	MCM41L1000J70R2	MCM41L1000Z70
MCM41L1000P80	MCM41L1000J80	MCM41L1000J80R2	MCM41L1000Z80

NOTE: For mechanical data, please see Chapter 10.