# MIC5810

## 10-Bit Serial-Input Latched Driver

**Preliminary Information**

## General Description

The MIC5810 is a 10-bit, serial-input, latched driver. Each high-voltage driver output features bipolar sourcing and DMOS sinking circuitry.

The MIC5810 logic operates from a 12V maximum supply voltage with driver outputs rated up to 60V. Each output can source up to 40mA and sink up to 15mA.

The MIC5810's CMOS logic inputs are compatible with TTL logic when the driver's logic supply is 5V. Pull-up resistors may be required when using higher logic supply voltages. A CMOS serial data output allows several latched drivers to be connected in series.

The MIC5810 can typically receive serial data at 5MHz with a 5V supply and 7.5MHz with a 12V supply.

The MIC5810 is available in the 18-pin plastic DIP and Wide SOIC in the –40°C to +85°C temperature range.

## Features

- 3.3MHz guaranteed data input (at $V_{DD}$ = 5V)
- Up to 12V logic supply
- Up to 60V load supply
  - 40mA Darlington source
  - 15mA active DMOS sink
- Low power dissipation

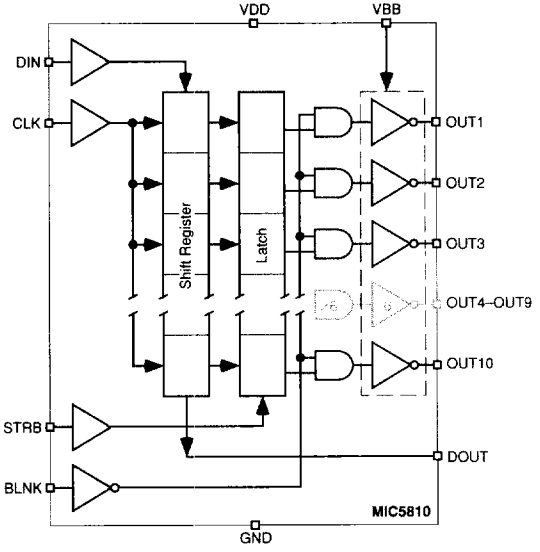
## Applications

- Vacuum fluorescent display
- Peripheral power driver

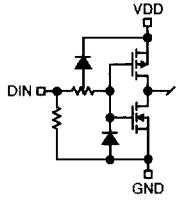
## Ordering Information

| Part Number | Temperature Range | Package |
|---|---|---|
| MIC5810BN | –40°C to +85°C | 18-pin DIP |
| MIC5810BWM | –40°C to +85°C | 18-pin Wide SOIC |

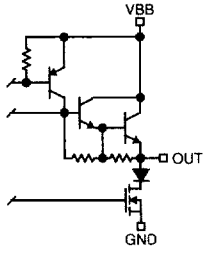
## Functional Diagrams




**MIC5810 Block Diagram**

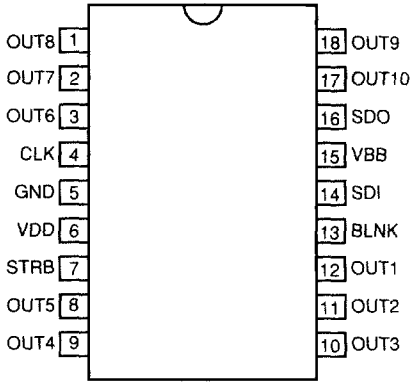



**Typical MIC5810 Logic Input**




**Typical MIC5810 Driver Output**

## Pin Configuration




**18-Pin DIP (N)**
**18-Pin Wide SOIC (WM)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1–3 | OUT8–OUT6 | Source/Sink Driver Output 8 through 6: See "Functional Diagrams: Typical MIC5810 Driver Output." |
| 4 | CLK | Clock (Input): CMOS input. Rising edge of clock pulse transfers DIN state into shift register. Existing shift register contents are moved toward DOUT pin. |
| 5 | GND | Ground: Logic and load return. |
| 6 | VDD | Logic Supply (input): +12V maximum. |
| 7 | STRB | Strobe (Input): Transfers register state to latch when high. STR may be continuously high to bypass latches. (Also see BLNK.) |
| 8–12 | OUT5–OUT1 | Source/Sink Driver Output 5 through 1: See "Functional Diagrams: Typical MIC5810 Driver Output." |
| 13 | BLNK | Blanking (Input): BLNK high disables all output source transistors and enables all output sink MOSFETs. If latch (STRB) is not used, blanking can be held high during serial data entry. |
| 14 | SDI | Serial Data Input: CMOS input to shift register. (Also see CLK.) |
| | NC | Not connected. |
| 15 | VBB | Load Supply (Input): +60V maximum. |
| 16 | SDO | Serial Data Output: CMOS Output. Provides output state of last bit in shift register. |
| 17,18 | OUT10, OUT9 | Source/Sink Driver Output 10 and 9: See "Functional Diagrams: Typical MIC5810 Driver Output." |

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## Absolute Maximum Ratings

Logic Supply Voltage ($V_{DD}$) ..... 15V
Driver Supply Voltage ($V_{BB}$) ..... 60V
Driver Output Current
  Source ($I_{OUT}$) ..... 40mA
  Sink ($I_{OUT}$) ..... 15mA
Serial Input Voltage ($V_{DIN}$) ..... –0.3V to $V_{DD}$ + 0.3V
Junction Temperature ($T_J$) ..... 150°C

## Operating Ratings

Logic Supply Voltage ($V_{DD}$) ..... 4.5V to 12V
Driver Supply Voltage ($V_{BB}$) ..... 60V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance
  PDIP $\theta_{JA}$ ..... 56°C/W
  SOIC $\theta_{JA}$ ..... 84°C/W

## Electrical Characteristics (5V)

$V_{DD}$ = 5V, $V_{BB}$ = 60V, $T_A$ = 25°C, unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CEX}$ | Output Leakage Current | $V_{OUT}$ = 0V, $T_A$ = +85°C | | –5.0 | –15 | µA |
| $V_{OUT(1)}$ | Output Voltage | $I_{OUT}$ = –25mA, $V_{BB}$ = 60V | 58 | 58.5 | | V |
| $V_{OUT(0)}$ | Output Voltage | $I_{OUT}$ = 1mA | | 1.0 | 1.5 | V |
| $I_{OUT(0)}$ | Output Pull-Down Current | $V_{OUT}$ = 5V to $V_{BB}$ | 2.0 | 3.5 | | mA |
| $V_{IN(1)}$ | Input Voltage | | 3.5 | | 5.3 | V |
| $V_{IN(0)}$ | Input Voltage | | –0.3 | | 0.8 | V |
| $I_{IN(1)}$ | Input Current | $V_{IN}$ = $V_{DD}$ | | 7 | 100 | µA |
| $I_{IN(0)}$ | Input Current | $V_{IN}$ = 0.8V | | 5 | 100 | µA |
| $V_{OUT(1)}$ | Serial Data | $I_{OUT}$ = –200µA | 4.5 | 4.7 | | V |
| $V_{OUT(0)}$ | Serial Data | $I_{OUT}$ = 200µA | | 200 | 250 | mV |
| $f_{CLK}$ | Maximum Clock Frequency | | 3.3 | 5.0 | | MHz |
| $I_{DD(1)}$ | Supply Current | all outputs high | | 100 | 300 | µA |
| $I_{DD(0)}$ | Supply Current | all outputs low | | 100 | 300 | µA |
| $I_{BB(1)}$ | Supply Current | outputs high, no load | | 0.7 | 2.0 | mA |
| $I_{BB(0)}$ | Supply Current | outputs low | | 10 | 100 | µA |
| $t_{PHL}$ | Blanking to Output Delay | $C_L$ = 30pF, 50% to 50% | | 300 | | ns |
| $t_{PLH}$ | Blanking to Output Delay | $C_L$ = 30pF, 50% to 50% | | 400 | | ns |
| $t_F$ | Output Fall Time | $C_L$ = 30pF, 90% to 10% | | 500 | | ns |
| $t_R$ | Output Rise Time | $C_L$ = 30pF, 10% to 90% | | 300 | | ns |
| $t_{DST}$ | Data Setup Time | see timing diagram | 75 | | | ns |
| $t_{DPW}$ | Data Pulse Width | see timing diagram | 150 | | | ns |
| $t_{DHT}$ | Data Hold Time | see timing diagram | 75 | | | ns |
| $t_{CPW}$ | Clock Pulse Width | see timing diagram | 150 | | | ns |
| $t_{SST}$ | Strobe Setup Time | see timing diagram | 300 | | | ns |
| $t_{SPW}$ | Strobe Pulse Width | see timing diagram | 100 | | | ns |
| $t_{OST}$ | Output Setup Time | see timing diagram | | 500 | | ns |

**General Note:** Devices are ESD protected; however, handling precautions are recommended.

## Electrical Characteristics (12V)

$V_{DD}$ = 12V, $V_{BB}$ = 60V, $T_A$ = 25°C, unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CEX}$ | Output Leakage Current | $V_{OUT}$ = 0V, $T_A$ = +85°C | | –5.0 | –15 | µA |
| $V_{OUT(1)}$ | Output Voltage | $I_{OUT}$ = –25mA, $V_{BB}$ = 60V | 58 | 58.5 | | V |
| $V_{OUT(0)}$ | Output Voltage | $I_{OUT}$ = 2mA | | 1.0 | 1.5 | V |
| $I_{OUT(0)}$ | Output Pull-Down Current | $V_{OUT}$ = 20V to $V_{BB}$ | 8.0 | 13 | | mA |
| $V_{IN(1)}$ | Input Voltage | | 10.5 | | 12.3 | V |
| $V_{IN(0)}$ | Input Voltage | | –0.3 | | 0.8 | V |
| $I_{IN(1)}$ | Input Current | $V_{IN}$ = $V_{DD}$ | | 50 | 240 | µA |
| $I_{IN(0)}$ | Input Current | $V_{IN}$ = 0.8V | | 15 | 240 | µA |
| $V_{OUT(1)}$ | Serial Data | $I_{OUT}$ = –200µA | 11.7 | 11.8 | | V |
| $V_{OUT(0)}$ | Serial Data | $I_{OUT}$ = 200µA | | 100 | 200 | mV |
| $f_{CLK}$ | Maximum Clock Frequency | | | 7.5 | | MHz |
| $I_{DD(1)}$ | Supply Current | all outputs high | | 200 | 500 | µA |
| $I_{DD(0)}$ | Supply Current | all outputs low | | 200 | 500 | µA |
| $I_{BB(1)}$ | Supply Current | outputs high, no load | | 0.7 | 2.0 | mA |
| $I_{BB(0)}$ | Supply Current | outputs low | | 10 | 100 | µA |
| $t_{PHL}$ | Blanking to Output Delay | $C_L$ = 30pF, 50% to 50% | | 200 | | ns |
| $t_{PLH}$ | Blanking to Output Delay | $C_L$ = 30pF, 50% to 50% | | 300 | | ns |
| $t_F$ | Output Fall Time | $C_L$ = 30pF, 90% to 10% | | 200 | | ns |
| $t_R$ | Output Rise Time | $C_L$ = 30pF, 10% to 90% | | 400 | | ns |

**General Note:** Devices are ESD protected; however, handling precautions are recommended.

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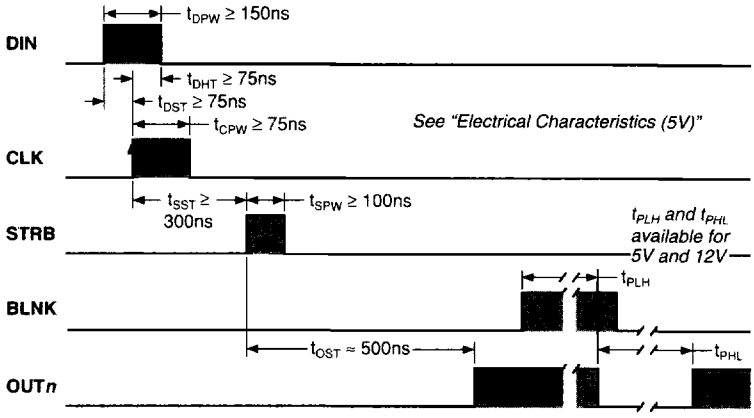
## Timing Diagram




**5V Timing Characteristics**

## Functional Description

Refer to the Block Diagram and Timing Diagram.

### Data Input

Data is transferred to the shift register on the rising edge of the clock pulse. Data must be present at SDI (serial data input) prior to the rising edge of the clock pulse (data setup time), and must remain for a time (data hold time) following the rising edge of the clock pulse.

### Shift Register

Data is shifted one bit at a time toward the SDO (serial data output) end of the shift register at each rising edge of the clock pulse.

### Latch

All shift register data bits are transferred to the latch when STRB (strobe) is high. STRB may be continuously held high for transparent operation. Data is valid for strobing to the latches after the strobe setup time. Data will appear at the outputs, if BLNK is low, after the output setup time.

### Blanking

When BLNK (blanking) is high, all outputs are forced low. Blanking can be used during data entry.

## Truth Table

| SDI | CLK | Shift Register | SDO | STRB | Latch | BLNK | OUT*n* |
|---|---|---|---|---|---|---|---|
| | | $I_1$ $I_2$ $I_3$ ... $I_N$ | | | $I_1$ $I_2$ $I_3$ ... $I_N$ | | $I_1$ $I_2$ $I_3$ ... $I_N$ |
| H | ↑ | H $R_1$ $R_2$ ... $R_{N-1}$ | $R_{N-1}$ | | | | |
| L | ↑ | L $R_1$ $R_2$ ... $R_{N-1}$ | $R_{N-1}$ | | | | |
| X | ↓ | $R_1$ $R_2$ $R_3$ ... $R_N$ | $R_N$ | | | | |
| | | X X X ... X | X | L | $R_1$ $R_2$ $R_3$ ... $R_N$ | | |
| | | $P_1$ $P_2$ $P_3$ ... $P_N$ | $P_N$ | H | $P_1$ $P_2$ $P_3$ ... $P_N$ | L | $P_1$ $P_2$ $P_3$ ... $P_N$ |
| | | | | | X X X ... X | H | L L L ... L |

L = Low Logic Level H = High Logic Level X = Don't Care P = Present State R = Previous State