PCMCIA/JEIDA DRAM

1. APPLICABLE CARD

• 8M Byte DRAM Card (DWF800SYD0)

2. OUTLINE OF FUNCTIONS AND FEATURES

The DWF800STD0 is a 2M words × 26 bits dynamic RAM card mounting 16PCS 4M-bit CMOS dynamic RAMs and 8PCS 1M-bit CMOS dynamic RAMs.
The physical specification and electrical specification of the DWF800SYD0 conform to PCMCIA/JEIDA DRAM CARD and its features are as follows.

(1) Size of the card: 85.6 × 54.0 × 3.3 mm
(2) Connection by 88-pin connector
(3) Includes a by pass capacitor for noise reduction in the card.
(4) Buffers provided for all input signals except $\overline{RAS}$
(5) Delayed write mode and read modify mode are not available.
(6) Fast page mode is available.
(7) $\overline{RAS}$-only refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh are possible.
(8) Refresh cycle
Decentralized refresh : 1024 cycles/128 ms
Centralized refresh : 1024 cycles/64 ms

3. EXPLANATION OF PINS

1) A0 - A9
Address lines.
These lines are connected to all DRAMs through buffers.
Fix unused addresses to "H" level or "L" level.

2) DQ0 - DQ35
Data lines.
Each line consists of 36 bits in 8-bit units plus a parity bit.
Each signal is directly connected to DRAMs.

3) $\overline{WE}$
Write Enable (LOW Active)

4) $\overline{RAS0}$ - $\overline{RAS3}$
ROW address strobe signals (LOW Active)
Four banks consisting of 18 bits each are controlled by 4 signals.
Except between early write cycle and refresh cycle, don't make both $\overline{RAS0}$ and $\overline{RAS1}$ or both $\overline{RAS2}$ and $\overline{RAS3}$ active at the same time to avoid data bus collision.

5) $\overline{CAS0}$ - $\overline{CAS3}$
Column address strobe signals (LOW Active)
Four blocks consisting of 9 bits each are controlled by 4 signals.
The relationship between signals and blocks is as follows.
$\overline{CAS0}$ ··· DQ0 - DQ8, $\overline{CAS1}$ ··· DQ9 - DQ17
$\overline{CAS2}$ ··· DQ18 - DQ26, $\overline{CAS3}$ ··· DQ27 - DQ35

6) PD1 - PD8
Presence detect pins
These pins represent card configuration information. The relationship between pins and information is as follows.
PD1, PD2, PD3, PD4 ····· Device configuration
PD5 ····· Number of banks
PD6, PD7 ····· Access time
PD8 ····· Refresh time

7) V_{CC}
Supply voltage: +5 V ±5%

8) V_{SS}
Ground
All voltages are based on this pin.

9) NC
No connect

4. ELECTRICAL CHARACTERISTICS

4–1. Maximum Rating

Description	Rating	Unit	Remarks
Signal Voltage	–0.5 ~ V_{CC}+0.5	V	Under 6 V
Supply Voltage	–0.5 ~ +6.0	V	
Output Short-circuit Current	50	mA	
Power Dissipation		W	
Operating Temperature	0 ~ +55	°C	
Storage Temperature	–20 ~ +65	°C	

4–2. Recommended Operating Conditions

Description		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	V
Input Voltage (HIGH Level)	$\overline{RAS}$, I/O	V_{IH}	2.4	—	V_{CC}+0.5	V
	Others	V_{IH}	V_{CC}×0.7	—	V_{CC}+0.5	V
Input Voltage (LOW Level)	$\overline{RAS}$, I/O	V_{IL}	–0.5	—	0.8	V
	Others	V_{IL}	–0.5	—	0.8	V

4–3. DC Electrical Characteristics (Ta = 0 ~ 50°C, V_{CC} = 5 V ±5%)

Descripiton	Symbol	Min	Typ	Max	Unit	Measuring Conditions
Operating Current	I_{CC1}	—	650	1000	mA	$\overline{RAS}$, $\overline{CAS}$=cycling t_{RC}=min
Standby Current	I_{CC2}	—	2	4	mA	$\overline{RAS}$=$\overline{CAS}$=$\overline{WE}$= V_{CC}–0.5V I_{OUT}=0mA Address=0.5V or V_{CC}–0.5V
Standby Current	I_{CC3}	—	2	4	mA	$\overline{RAS}$=$\overline{WE}$=V_{CC}–0.5V $\overline{CAS}$=0.5V, I_{OUT}=0mA Address=0.5V or V_{CC}–0.5V
$\overline{RAS}$-only Refresh Current	I_{CC4}	—	1000	2000	mA	t_{RC}=160ns
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current	I_{CC5}	—	1000	2000	mA	t_{RC}=160ns
Fast Page Mode Current	I_{CC6}	—	—	1000	mA	$\overline{RAS}$=V_{IL}, tpc=55ns $\overline{CAS}$=cycling
Input Leakage Current	I_{LI}	–60	—	60	μA	0≤Vin≤6V
Output Leakage Current	I_{LO}	–60	—	60	μA	0≤Vin≤6V Dout=Disable
Output Voltage (HIGH Level)	V_{OH}	2.4	—	V_{CC}	V	Iout=–5mA
Output Voltage (LOW Level)	V_{OL}	0	—	0.4	V	Iout=4.2mA

Notes:
1. I_{CC} is determined by the output load condition when a device is selected. I_{CC} MAX is defined as I_{CC} in the output open condition.
2. When $\overline{RAS}$ = V_{IL}, address switching must be performed once or less.
3. When $\overline{CAS}$ = V_{IH}, address switching must be performed once or less.
4. V_{CC} –0.2 ≤ V_{IH} ≤ V_{CC} and 0 V ≤ V_{IL} ≤ 0.2 V

4–4. Capacitance

Description	Symbol	Min	Typ	Max	Unit	Notes
Address	C0	—	—	20	pF	1, 2
RAS	C1	—	—	60	pF	1, 2
CAS, WE	C2	—	—	20	pF	1, 2
Data	C3	—	—	45	pF	1, 2, 3

Address : A0 ~ A9
$\overline{RAS}$: $\overline{RAS0}$ ~ $\overline{RAS3}$
$\overline{CAS}$, $\overline{WE}$: $\overline{CAS0}$ ~ $\overline{CAS3}$, $\overline{WE}$
Data : DQ0 ~ DQ35

Notes:
1. This value is not a guaranty value but a sample value.
2. 25°C, f = 1 MHz, V_{CC} = 0 V
3. Value measured at $\overline{CAS}$ = V_{IH} in order to disable D_{OUT}.

4–5. AC Electrical Characteristics

Read, Write, Refresh (Common Parameters) (Ta = 0 ~ 50°C, VCC = 5 V ±5%)

Description	Symbol	Min	Max	Unit	Note
Random read/write time	tRC	160	—	ns	
$\overline{RAS}$ precharge time	tRP	70	—	ns	
$\overline{RAS}$ pulse width	tRAS	80	10000	ns	
$\overline{CAS}$ pulse width	tCAS	25	10000	ns	
Row address set-up time	tASR	7	—	ns	
Row address hold time	tRAH	12	—	ns	
Column address set-up time	tASC	0	—	ns	
Column address hold time	tCAH	20	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	tRCD	22	48	ns	8
$\overline{RAS}$/column address delay time	tRAD	17	33	ns	9
$\overline{RAS}$ hold time	tRSH	32	—	ns	
$\overline{CAS}$ hold time	tCSH	80	—	ns	
$\overline{CAS}$/$\overline{RAS}$ precharge time	tCRP	17	—	ns	
CAS delay time from data input	tDZC	0	—	ns	
Transition time	tT	3	50	ns	7
Refresh cycle	tREF	—	128	ms	16

Read Cycle (Ta = 0 ~ 50°C, VCC = 5 V ±5%)

Description	Symbol	Min	Max	Unit	Note
Access time from $\overline{RAS}$	tRAC	—	80	ns	2, 3
Access time from $\overline{CAS}$	tCAC	—	32	ns	3, 4, 13
Access time form address	tAA	—	47	ns	3, 5, 13
Read command set-up time	tRCS	0	—	ns	
Read command hold time (for $\overline{CAS}$)	tRCH	0	—	ns	15
Read command hold time (for $\overline{RAS}$)	tRRH	10	—	ns	15
Column address $\overline{RAS}$ read time	tRAL	47	—	ns	
Output buffer turn-off time	tOFF	0	27	ns	6
$\overline{CAS}$ data input delay time	tCDD	27	—	ns	

Write Cycle (Ta = 0 ~ 50°C, VCC = 5 V ±5%)

Descripiton	Symbol	Min	Max	Unit	Note
Write command set-up time	tWCS	0	—	ns	10
Write command hold time	tWCH	20	—	ns	
Data input set-up time	tDS	0	—	ns	11
Data input hold time	tDH	27	—	ns	11

Refresh Cycle (Ta = 0 ~ 50°C, VCC = 5 V ±5%)

Descripiton	Symbol	Min	Max	Unit	Note
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	tCSR	17	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	tCHR	20	—	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	tRPC	10	—	ns	
Normal mode $\overline{CAS}$ precharge time	tCPN	—	—	ns	

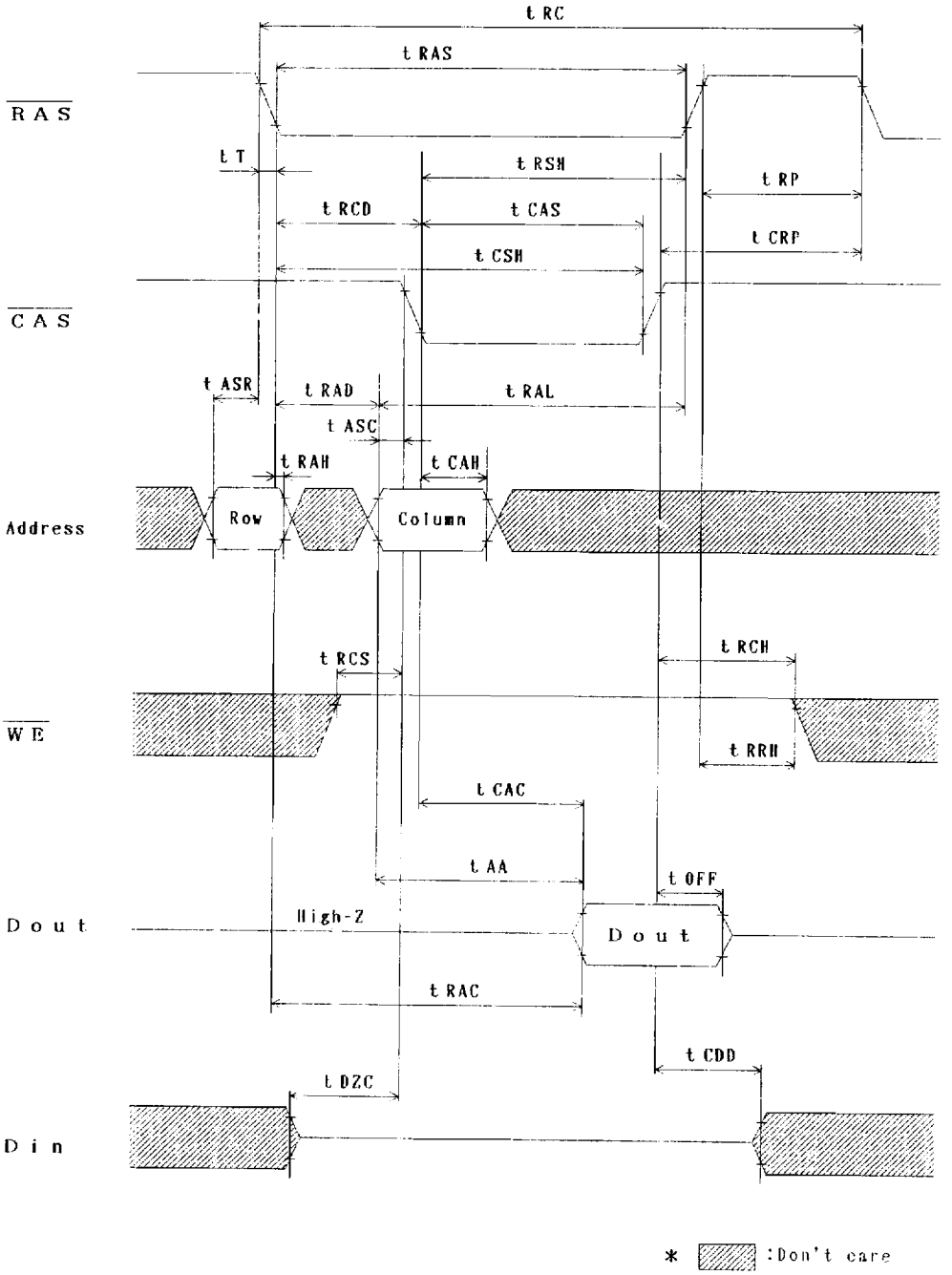
Fast Page Mode Cycle (Ta = 0 ~ 50°C, VCC = 5 V ±5%)

Description	Symbol	Min	Max	Unit	Note
Fast page mode cycle	tPC	55	—	ns	
Fast page mode $\overline{CAS}$ Precharge time	tCP	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	tRASC	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	tACP	—	57	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	57	—	ns	

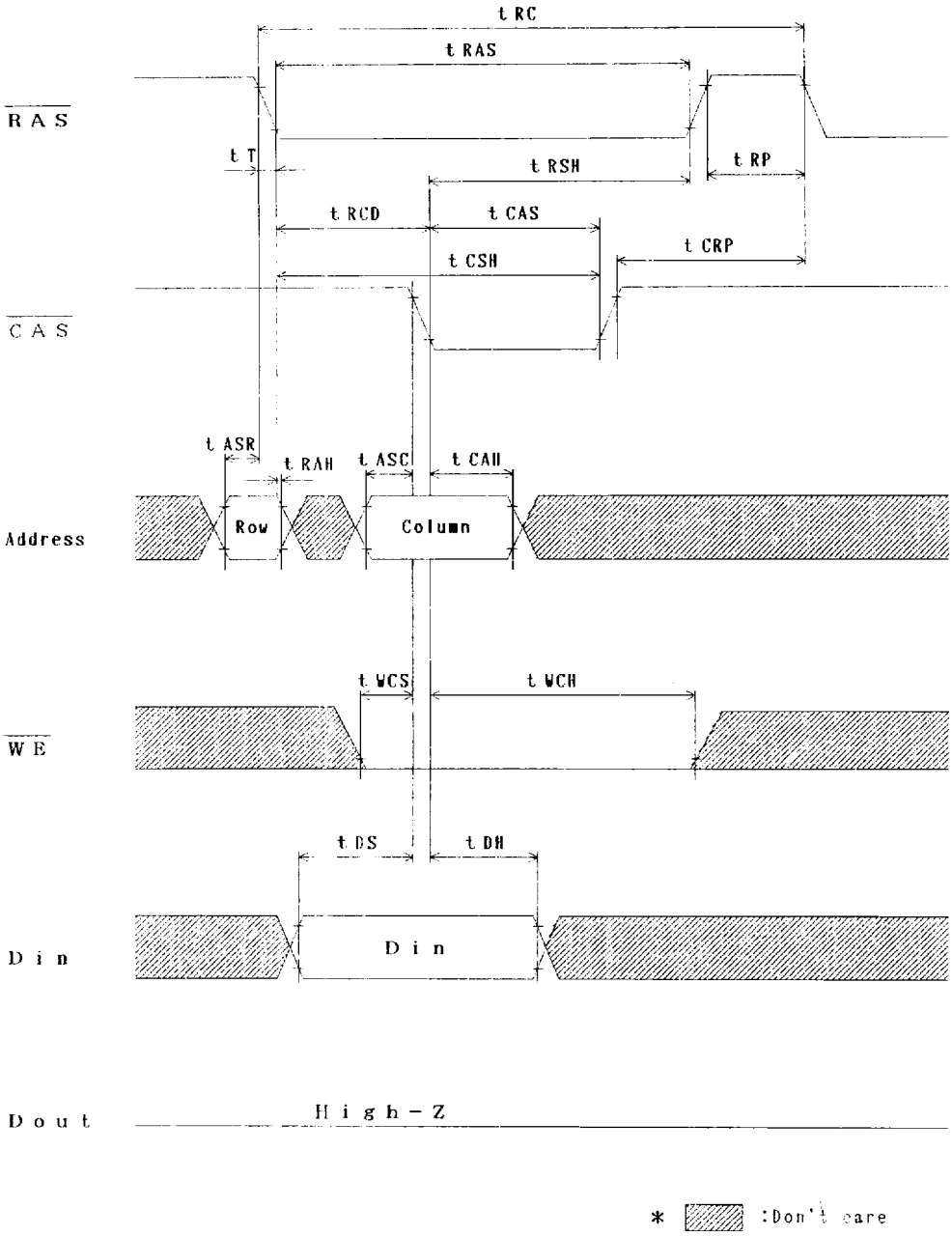
Notes on AC Electrical Characteristics

1. t_T = 5 ns for AC measurement.
2. $t_{RCD} \leq t_{RDC}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
   When t_{RCD} or t_{RAD} is larger than the recommended value in this table, t_{RAC} exceeds the specified value.
3. Measurement with a load circuit equivalent to 2 TTL + 100 pF.
4. When $t_{RCD} \geq t_{RCD}$ (MAX) and $t_{RAD} \leq t_{RAD}$ (MAX), apply this value.
5. When $t_{RCD} \leq t_{RCD}$ (MAX) and $t_{RAD} \geq t_{RAD}$ (MAX), apply this value.
6. t_{OFF} (MAX) is defined by time for the case where the output reaches the open status and the output voltage level cannot be referenced.
7. V_{IH} (MIN) and V_{IL} (MAX) are measurement timing reference levels of input signals. The transition time is the fall time from V_{IH} to V_{IL} or the reverse rise time.
8. When t_{RCD} is larger than RCD (MAX), the access time is defined as t_{CAC}.
9. When t_{RAD} is larger than t_{RAD} (MAX), the access time is defined by t_{AA}.
10. When $t_{WCS} \geq t_{WCS}$ (MIN), this cycle becomes an early write cycle. The data pins are in the input status during this cycle. When $t_{WCS} < t_{WVS}$ (MIN), this cycle does not become a write cycle and the data pins are in the output status, so that indefinite data is output.
11. These parameters are applied to the leading edge of $\overline{CAS}$ in the early write cycle.
12. t_{RASC} is defined by the $\overline{RAS}$ pulse width of the fast page mode cycle.
13. The access time is defined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. Wait for 100 μs or more after the power supply is turned on, and add 8 or more initial cycles. Add ordinary $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle as the initial cycle.
    When using an internal refresh counter, the initial cycle is limited to the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
15. One of t_{RCH} and t_{RRH} should be satisfied.
16. This parameter value is applied to only decentralized refresh.
    For centralized refresh, the value becomes 64 ms.

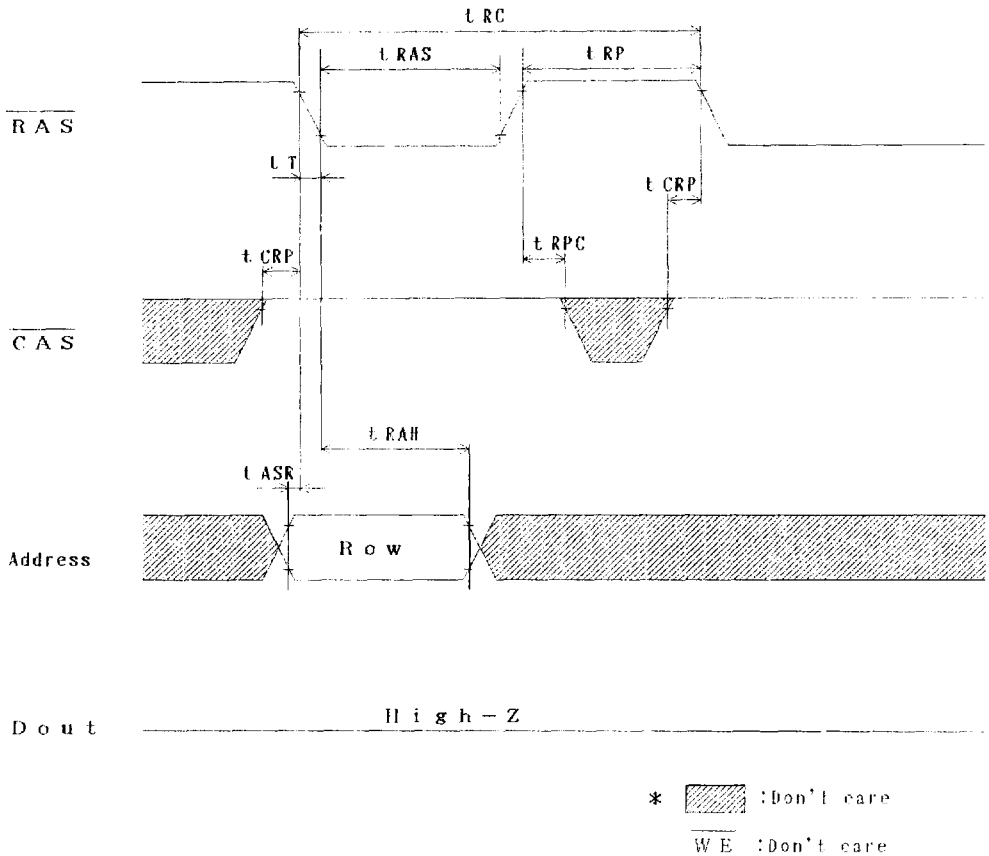
Timing Chart Read Cycle



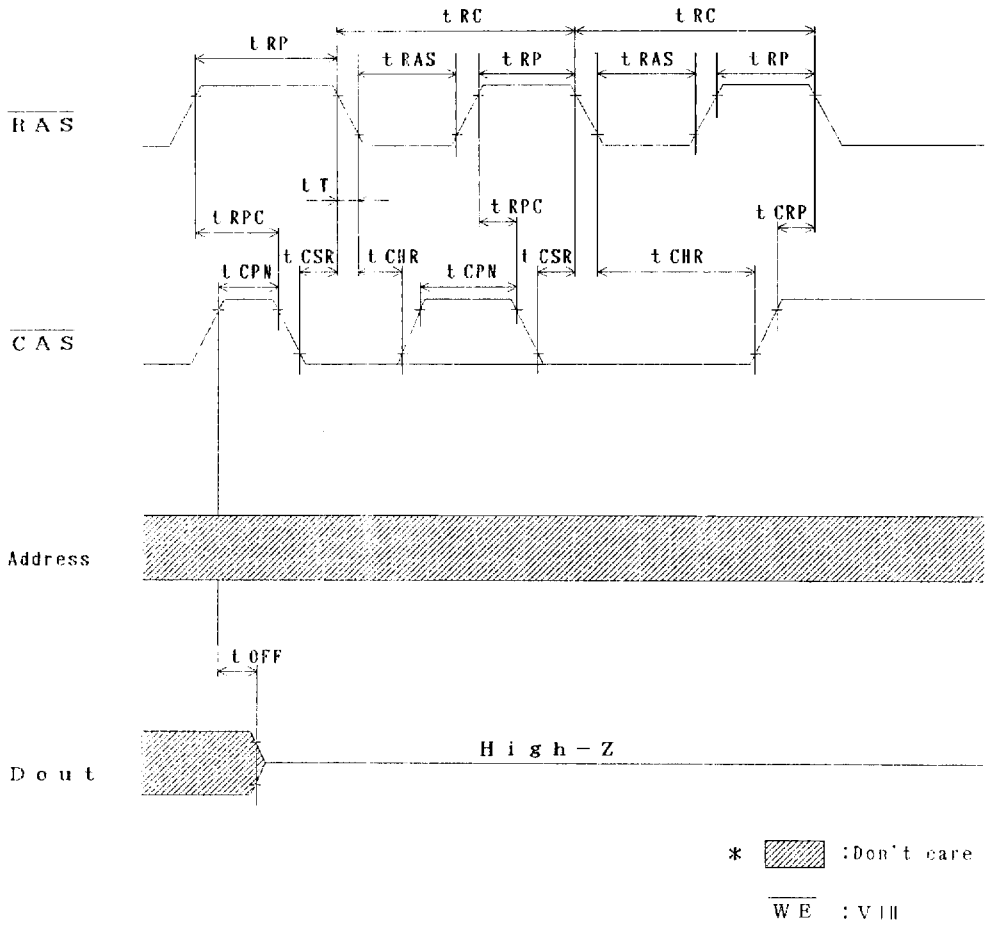
Early Write Cycle



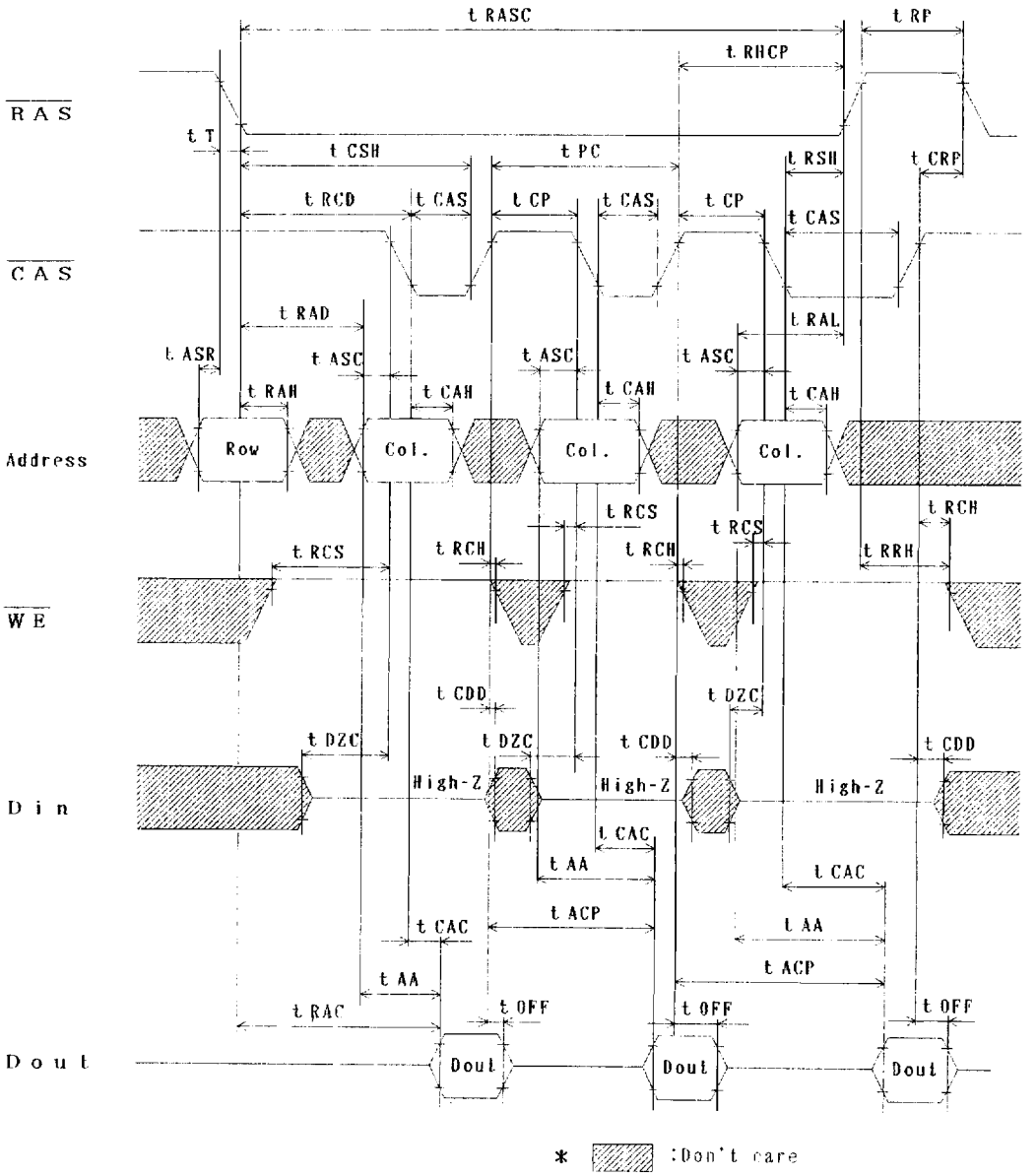
Refresh Cycle, $\overline{RAS}$-only Refresh Cycle



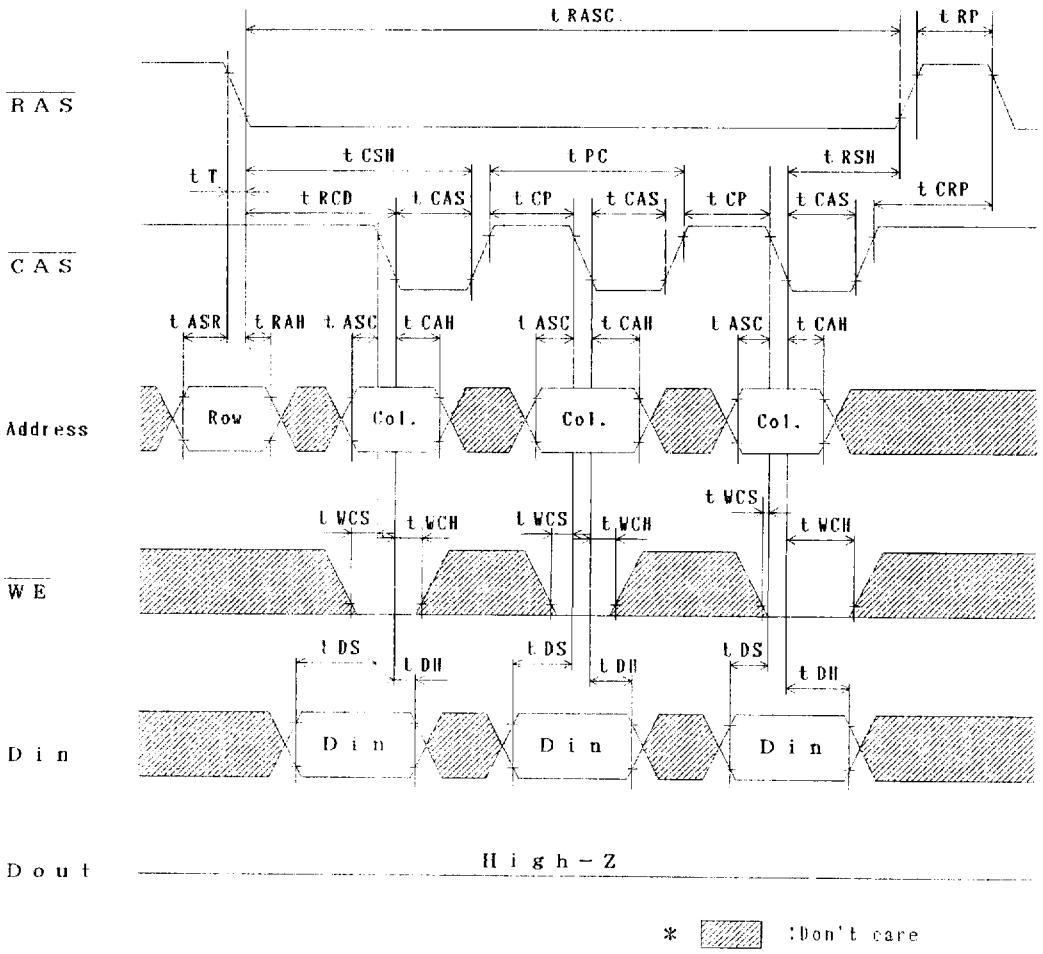
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle



Fast Page Mode Cycle, Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle



PD PIN ASSIGNMENT

PIN-Name	Connection	Contents
PD1	GND	Device Data • • • • • 1 M × 4 Parity • • • • 1 M × 1
PD2	NC	
PD3	GND	Address Data • • • • • Row/Column=10/10 Parity • • • • Row/Column=10/10
PD4	GND	
PD5	GND	Number of banks • • • 2
PD6	NC	*Access time (t_{RAC}) 80 ns
PD7	GND	
PD8	NC	Slow refresh

Remarks : The access time is also applicable to 70 ns and 100 ns.

5. PIN ASSIGNMENT

Pin No.	Name	Function	Pin No.	Name	Function
1	GND	Ground	45	GND	Ground
2	DQ0	Data 0	46	DQ18	Data 18
3	DQ1	Data 1	47	DQ19	Data 19
4	DQ2	Data 2	48	DQ20	Data 20
5	DQ3	Data 3	49	DQ21	Data 21
6	DQ4	Data 4	50	DQ22	Data 22
7	DQ5	Data 5	51	DQ23	Data 23
8	DQ6	Data 6	52	DQ24	Data 24
9	Vcc	Power supply (5V)	53	DQ25	Data 25
10	DQ7	Data 7	54	DQ26	Data 26
11	NC	No connect	55	NC	No connect
12	DQ8	Data 8	56	GND	Ground
13	A0	Address 0	57	A1	Address 1
14	A2	Address 2	58	A3	Address 3
15	Vcc	Power supply (5V)	59	A5	Address 5
16	A4	Address 4	60	A7	Address 7
17	NC	No connect	61	A9	Address 9
18	A6	Address 6	62	NC	No connect
19	A8	Address 8	63	GND	Ground
20	NC	No connect	64	NC	No connect
21	NC	No connect	65	$\overline{RAS1}$	Row address strobe 1
22	$\overline{RAS0}$	Row address strobe 0	66	$\overline{CAS2}$	Column address strobe 2
23	$\overline{CAS0}$	Column address strobe 0	67	GND	Ground
24	$\overline{CAS1}$	Column address strobe 1	68	$\overline{CAS3}$	Column address strobe 3
25	NC	No connect	69	$\overline{RAS3}$	Row address strobe 3
26	$\overline{RAS2}$	Row address strobe 2	70	$\overline{WE}$	Write enable
27	Vcc	Power supply (5V)	71	PD1	Presence detect 1
28	PD2	Presence detect 2	72	PD3	Presence detect 3
29	PD4	Presence detect 4	73	GND	Ground
30	PD6	Presence detect 6	74	PD5	Presence detect 5
31	NC	No connect	75	PD7	Presence detect 7
32	NC	No connect	76	PD8	Presence detect 8
33	DQ17	Data 17	77	NC	No connect
34	DQ9	Data 9	78	NC	No connect
35	NC	No connect	79	DQ35	Data 35
36	DQ10	Data 10	80	DQ27	Data 27
37	Vcc	Power supply(5V)	81	DQ28	Data 28
38	DQ11	Data 11	82	DQ29	Data 29
39	DQ12	Data 12	83	DQ30	Data 30
40	DQ13	Data 13	84	DQ31	Data 31
41	DQ14	Data 14	85	DQ32	Data 32
42	DQ15	Data 15	86	DQ33	Data 33
43	DQ16	Data 16	87	DQ34	Data 34
44	GND	Ground	88	GND	Ground

6. Block Diagram