

MN5515

High-Speed Color Conversion LSI

■ Overview

The MN5515 is a high-speed color conversion processor capable of free conversion among various full-color formats.

It offers a low-cost solution to reproducing colors from various sources in multimedia environments.

Note: This product is manufactured under license from Electronics for Imaging, Inc., holders of US Patent 4,837,722.

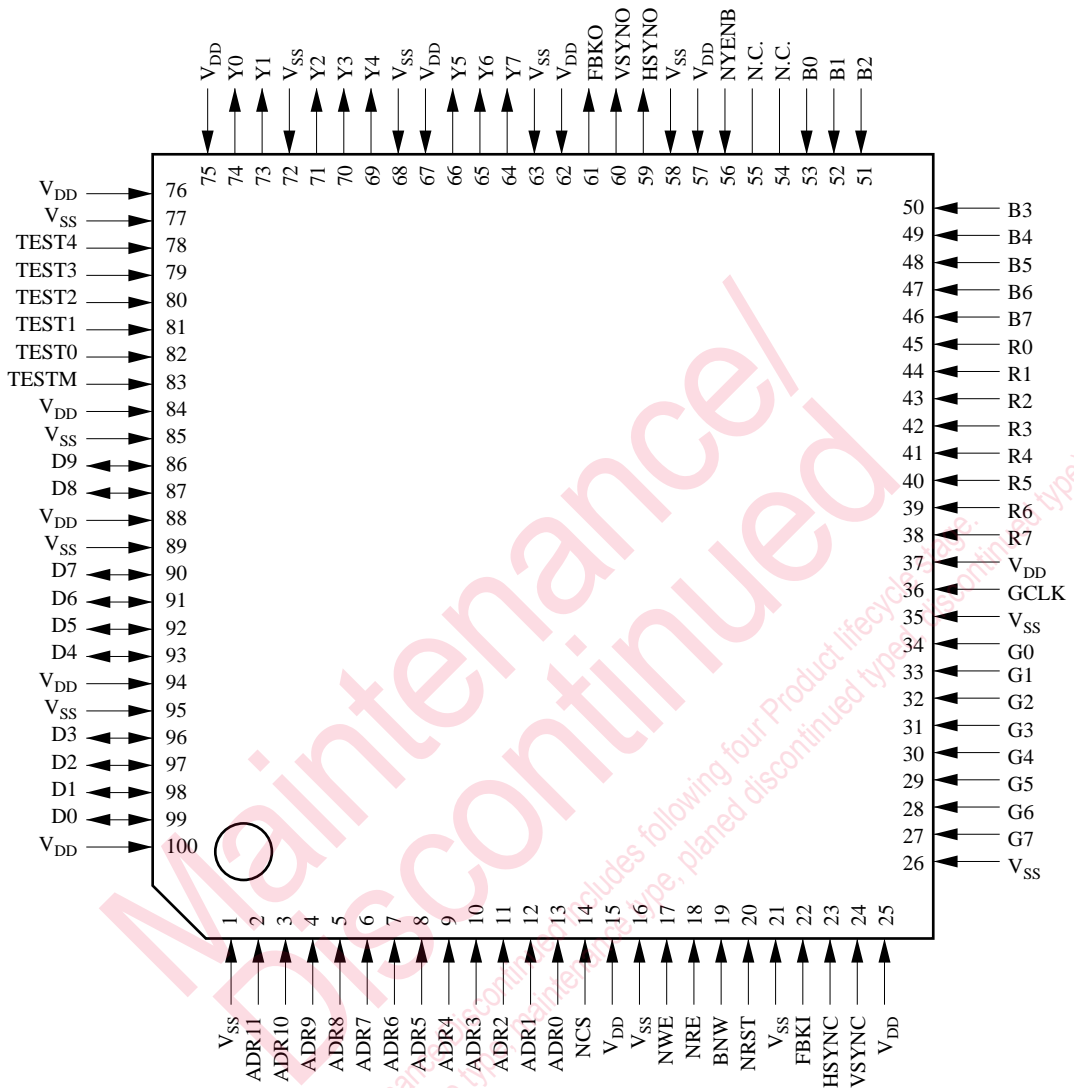
■ Features

- Conformable to ICC standard model
- Real-time conversion of full-color signals using prism interpolation method
- Greater precision in reproducing black with new slant prism interpolation method
- An appropriate management for the system is available by only setting the three-dimensional look-up table in RAM that attaches to the host interface.
- Maximum processing speed (t_{\min}): 62.5 ns/pixel
- Maximum operating frequency (f_{\max}): 16 MHz
- Data width for pixel input: 8 bits \times 3 channels
- Data width for pixel output: 8 bits \times 1 channel
- Host interface bus width: 8 or 10 bits (Switchable at any time during operation)
- Number of memories of 3D-LUT: $9 \times 9 \times 9 = 729$
- Color conversion look-up table output data width (signed): 10 bits
- Choice of built-in prism or slant prism interpolation function by a register
- Auxiliary delay line: 1 bit (10 t pipeline delay)
- Pipeline delay: 10 t (t: 1 GCLK)

■ Applications

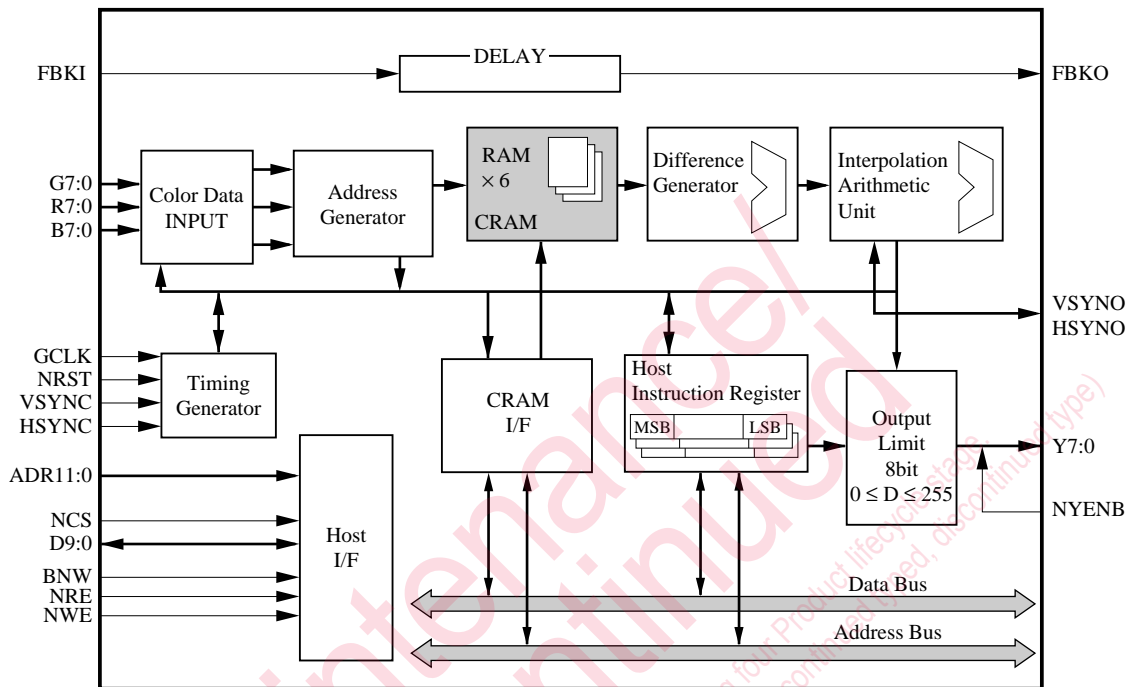
- Faithful color reproduction with color scanners, color printers, color copiers, color facsimile machines, and other office electronics equipment
- Color adjustment for television cameras, displays, and other imaging equipment
- High-speed accelerator in color conversion for computer graphics, computer-aided design, and workstation applications
- Differentiating parts by color on automated production lines

■ Pin Assignment



(TOP VIEW)
QFP100-P-1818

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Type	I/O	Number	Level	Logic	Function description	Remarks
14	NCS	Control signals	I	1	T	L	Chip select	
18	NRE		I	1	T	L	Read enable	
17	NWE		I	1	T	L	Write enable	
2 to 13	ADR11 to 0		I	12	T	H	Address bus	
86, 87, 90 to 93, 96 to 99	D9 to 0		I/O	10	T	H	Bidirectional data bus	
20	NRST		I	1	T	L	System reset	
19	BNW		I	1	T		Byte/word select	H/L: Byte/word
56	NYENB		I	1	T	L	Image output enable	
36	GCLK	Image I/O signals	I	1	T	H	Pixel clock	
27 to 34	G7 to 0		I	8	T	H	Pixel input (G)	
38 to 45	R7 to 0		I	8	T	H	Pixel input (R)	
46 to 53	B7 to 0		I	8	T	H	Pixel input (B)	
64 to 66, 69 to 71, 73, 74	Y7 to 0		O	8	T	H	Color conversion output data	
24	VSYNC		I	1	T	L	Vertical synchronization signal	
23	HSYNC		I	1	T	L	Horizontal synchronization signal	
60	VSYNO		O	1	T	L	Vertical delay synchronization signal	VSYNC output
59	HSYNO		O	1	T	L	Horizontal delay synchronization signal	HSYNC output
22	FBKI		I	1	T		Auxiliary input signal	
61	FBKO	O	1	T		Auxiliary output signal		
78 to 82	TEST4 to 0	Miscellaneous	I	5	T		Test signal	Connect these to ground
83	TESTM		I	1	C		Test signal	Connect this to ground
15, 25, 37, 57, 62, 67, 75, 76, 84, 88, 94, 100	V _{DD}	Power supply	I				+5V	Connect all pins.
1, 16, 21, 26, 35, 58, 63, 68, 72, 77, 85, 89, 95	V _{SS}		I				0V	Connect all pins.

T: TTL

C: CMOS

H: High

L: Low

■ Functional Description

● Color conversion algorithm

This color conversion LSI converts colors using a three-dimensional look-up table and three-dimensional interpolation.

The three-dimensional look-up table holds output values at representative pixel-input. The number of representative output points in the operating mode is shown in the following table.

Number of Representative Points in Three-Dimensional Look-Up Table

	Prism Interpolation	Slant Prism Interpolation
333 mode	$9 \times 9 \times 9 = 729$	$9 \times 9 \times 9 = 729$ (MN5515 configuration)
		$11 \times 11 \times 9 = 1089$ (if lattice points extrapolation does not used)

For slant prism interpolation, the MN5515 uses the same 729 points that it uses for prism interpolation so as to support lattice point extrapolation. It derives its output image data with three-dimensional interpolation based on the data for the six lattice points by prism or slant prism interpolation method that depends on the input image data.

1. Prism interpolation method

Figure 1 illustrates the procedure that the color conversion LSI applies to produce prism interpolation.

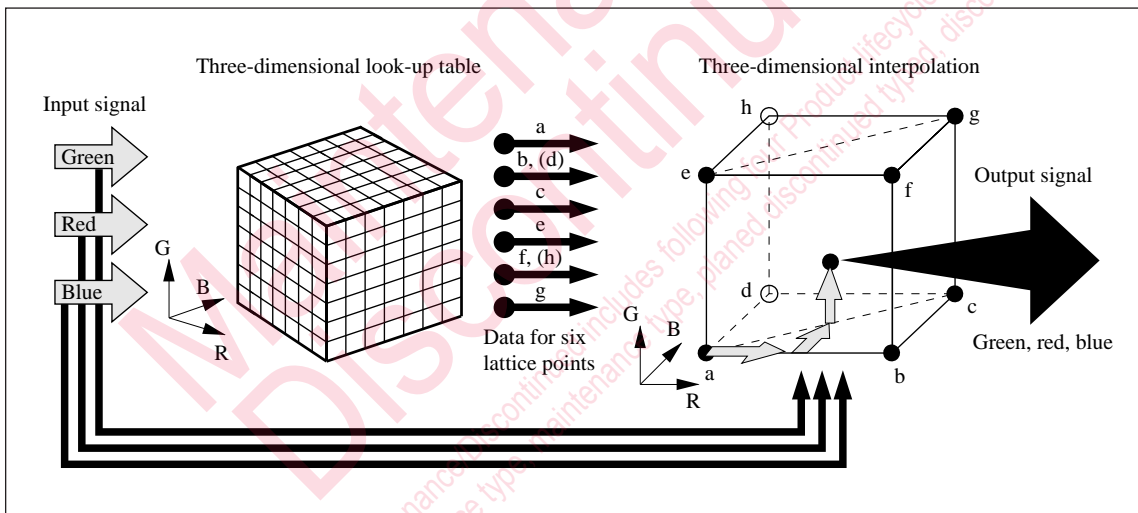


Figure 1 Principle of Operation for Color Conversion LSI

Figure 2 illustrates the prism interpolation algorithm itself. Point o represents the position of the input data in the coordinate space; points a, b, c, e, f, and g, the six lattice points specified by the upper bits in the data; D(a), D(b), D(c), D(e), D(f), and D(g), the data values for these lattice points. The line mn is the perpendicular joining the two parallel prism faces and passing through point o. The output data D(o) is derived from the following linear interpolation calculation with weighting coefficients based on these 6 data and the lower bits of the input data.

If $RL \geq BL$

$$D(o) = D(m) + (D(n) - D(m))GL/L \quad (\text{Note: } L \text{ is a unit distance between lattice points})$$

where,

$$D(m) = D(a) + (D(b) - D(a))RL/L + (D(c) - D(b))BL/L$$

$$D(n) = D(e) + (D(f) - D(e))RL/L + (D(g) - D(f))BL/L$$

If $RL < BL$

$$D(o) = D(m) + (D(n) - D(m))GL/L$$

where,

$$D(m) = D(a) + (D(c) - D(d))RL/L + (D(d) - D(a))BL/L$$

$$D(n) = D(e) + (D(g) - D(h))RL/L + (D(h) - D(e))BL/L$$

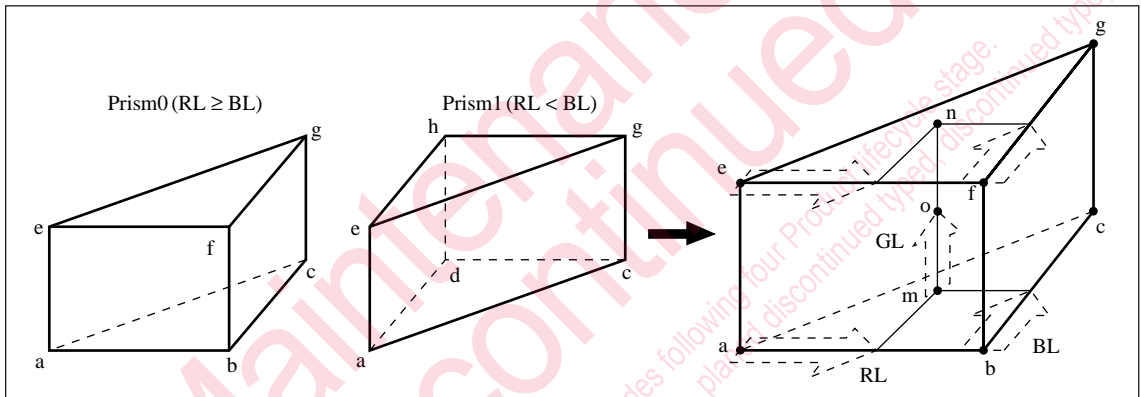


Figure 2 Prism Interpolation Algorithm

2. Slant prism interpolation method

Figure 3 illustrates the procedure that the color conversion LSI applies to produce slant prism interpolation.

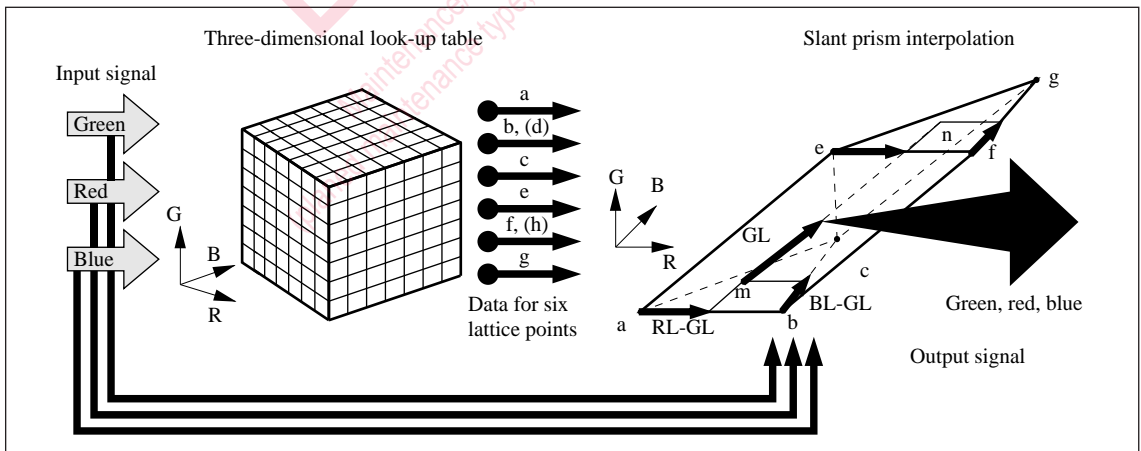


Figure 3 Principle of Color Conversion LSI Operation

Figure 4 illustrates the slant prism interpolation algorithm itself. Point o represents the position of the input data in the coordinate space; points a, b, c, e, f, and g, the six lattice points specified by the upper bits in the data; D(a), D(b), D(c), D(e), D(f), and D(g), the output values for these lattice points. The line mn is parallel to the slant-prism axis (a-e) and passing through point o. The output data D(o) is derived from the following linear interpolation calculation with weighting coefficients based on these 6 data and the lower bits of the input data.

If $(RL - GL) \geq (BL - GL)$

$$D(o) = D(m) + (D(n) - D(m))GL/L \quad (\text{Note: } L \text{ is the lattice spacing})$$

where,

$$D(m) = D(a) + (D(b) - D(a))(RL - GL)/L + (D(c) - D(b))(BL - GL)/L$$

$$D(n) = D(e) + (D(f) - D(e))(RL - GL)/L + (D(g) - D(f))(BL - GL)/L$$

If $(RL - GL) < (BL - GL)$

$$D(o) = D(m) + (D(n) - D(m))GL/L$$

where,

$$D(m) = D(a) + (D(c) - D(d))(RL - GL)/L + (D(d) - D(a))(BL - GL)/L$$

$$D(n) = D(e) + (D(g) - D(h))(RL - GL)/L + (D(h) - D(e))(BL - GL)/L$$

If $(RL - GL)$, $(BL - GL)$ in the above derivation is negative, anticipated origin correction automatically ensures that they are positive by adding L: $(RL - GL) + L$, $(BL - GL) + L$.

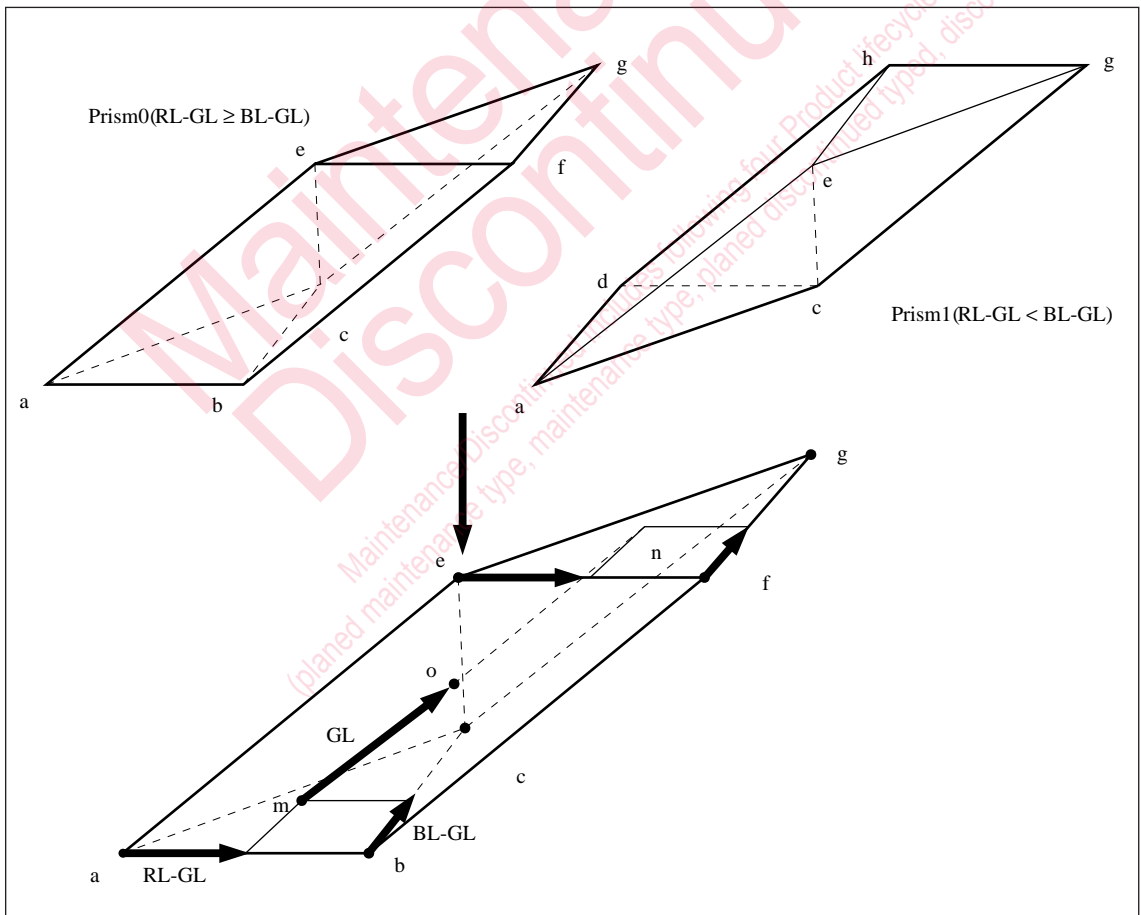


Figure 4 Slant Prism Interpolation Algorithm

3. Interpolation precision

The MN5515 uses signed integer arithmetic for all internal processing. The entries in the color conversion table are signed 10-bit integers (-512 to 511); the weighting coefficients for interpolation, unsigned 5-bit integers (0 to 31). To minimize rounding errors during internal processing and reduce arithmetic errors in the output, the LSI uses enhanced bit for internal arithmetic.

The following table gives the error, δ , between the output value and the calculated value for the each modes of the MN5515.

Error, δ , between Output Value and Calculated Value for Color Conversion LSI

	Output Magnification of 1	Output Magnification of 1/2	Output Magnification of 1/4
Half compression mode	$-1\text{LSB} \leq \delta \leq 0$	$-1\text{LSB} \leq \delta \leq 0$	$-1\text{LSB} \leq \delta \leq 0$
Standard mode	$-1\text{LSB} \leq \delta \leq 0$	$-1\text{LSB} \leq \delta \leq 0$	$-1\text{LSB} \leq \delta \leq 0$

4. Internal structure of three-dimensional look-up table

The three-dimensional look-up table is stored in six RAM chips (CRAM: M0 to M5). The following formulas derive CRAM number, M_i , and byte address, A_i , from the three-dimensional look-up table indices, X_i , Y_i , and Z_i .

$$M_i = (X_i + Y_i) \% 3 + (Z_i \% 2) \times 3$$

$$A_i = \{X_i / 3 + Y_i \times C1 + (Z_i / 2) \times C2\} \times 2$$

Note: The $X_i / 3$ indicate integer division discarding any remainder.

The percent signs indicate the modulo operator. C1 gives the maximum number of lattice points along the x-axis in groups of three because the memory is distributed among three RAM chips along the x-axis. C2 is the maximum value, in groups of three, for coordinate pairs for a single x-y plane.

This indexing scheme maps the R input to the x-axis, the B input to the y-axis, and the G input to the z-axis. Write the lattice point data to the CRAM chips in the following order: x-axis data, y-axis data, and z-axis data. The following table gives the values for C1 and C2.

	C1	C2
333 mode	3	27(3 × 9)

The same three-dimensional look-up table data are used for both the prism and slant prism algorithms.

■ Absolute Maximum Ratings

$V_{SS}=0V$

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to +7.0	V
Input pin voltage	V_I	-0.3 to $V_{DD} + 0.3$	V
Output pin voltage	V_O	-0.3 to $V_{DD} + 0.3$	V
Output current *1	I_{OL}	+12	mA
Output current *1	I_{OH}	-12	mA
Power dissipation	P_D	500	mW
Operating temperature	T_{opr}	-40 to +70	°C
Storage temperature	T_{stg}	-55 to +150	°C

Note*1: For pins with output current capacities other than the standard values, see the peak output current in Electrical Characteristics below.

Note: The above ratings represent the maximum values that may be applied without damaging the chip, not the limits for guaranteed operation.

■ Recommended Operating Conditions

$V_{SS}=0V$

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		4.75	5.0	5.25	V
Rise time	t_r		0		150	ns
Fall time	t_f		0		150	ns
Ambient temperature	T_a		0		70	°C

■ Input/Output Capacitance

Item	Symbol	Conditions	min	typ	max	Unit
Input pins	C_{IN}	$V_{DD}=V_I=0V$ $f=1MHz, T_a=25°C$		7	15	pF
Output pins	C_{OUT}			7	15	pF
I/O pins	C_{IO}				7	15

■ Electrical Characteristics

$V_{DD}=4.75$ to $5.25V$, $V_{SS}=0.00V$, $f_{TEST}=16MHz$, $T_a=0$ to $70^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent supply current	I_{DDs}	V_I (pull-up) = open V_I (pull-down) = open Other input pins and I/O pins in the high-impedance state are all simultaneously connected to either the V_{SS} or V_{DD} level.			620	μA
Operating supply current	I_{DDO}	$V_I=V_{DD}$ or V_{SS} $f=16.0MHz$ $V_{DD}=5.0V$ Outputs open		40.0	80.0	mA

CMOS level input, with pull-down resistor: TESTM

"H" level input voltage	V_{IH2}		$V_{DD} \times 0.7$		V_{DD}	V
"L" level input voltage	V_{IL2}		0		$V_{DD} \times 0.3$	V
Pull-down resistance	R_{PD1}	$V_I=V_{DD}$ $V_{DD}=5.0V$	12	30	75	Ω
Input leakage current	I_{LIPD}	$V_I=V_{SS}$			± 20	μA

TTL level input: B0 to B7, G0 to G7, R0 to R7, ADR0 to ADR11, BNW, NCS, NRE, NWE, GCLK, TEST3, TEST4, HSYNC, NYENB, VSYNC

"H" level input voltage	V_{IH1}		2.0		V_{DD}	V
"L" level input voltage	V_{IL1}		0		0.8	V
Input leakage current	I_{LI}	$V_I=V_{DD}$ or V_{SS}			± 10	μA

TTL level (Schmitt) input, with pull-up resistor: NRST

Input threshold voltage	V_{tHL}	$V_{DD}=4.75$ to $5.25V$		1.8	2.4	V
	V_{tLH}		0.4	1.0		
Hysteresis width	ΔV_{t}	$V_{DD}=5.0V$	0.4	0.8		V
Pull-up resistance	R_{PU1}	$V_I=0.0V$ $V_{DD}=5.0V$	12	30	75	k Ω
Input leakage current	I_{LIPU}	$V_I=V_{DD}$			± 20	μA

TTL level input, with pull-up resistor: FBKI

"H" level input voltage	V_{IH1}		2.0		V_{DD}	V
"L" level input voltage	V_{IL1}		0		0.8	V
Pull-up resistance	R_{PU1}	$V_I=0.0V$ $V_{DD}=5.0V$	12	30	75	k Ω
Input leakage current	I_{LIPU}	$V_I=V_{DD}$			± 20	μA

■ Electrical Characteristics (continued)

$V_{DD}=4.75$ to $5.25V$, $V_{SS}=0.00V$, $f_{TEST}=16MHz$, $T_a=0$ to $70^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
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TTL level input, with pull-down resistor: TEST0 to TEST2

"H" level input voltage	V_{IHL}		2.0		V_{DD}	V
"L" level input voltage	V_{IL1}		0		0.8	V
Pull-down resistance	R_{PD1}	$V_I=V_{DD}$ $V_{DD}=5.0V$	12	30	75	$k\Omega$
Input leakage current	I_{LIPD}	$V_I=V_{SS}$			± 20	μA

Push-pull outputs: FBKO, HSYNCO, VSYNCO

"H" level output voltage	V_{OH}	$I_O=-4.0mA$ $V_I=V_{DD}$ or V_{SS}	$V_{DD}-0.6$			V
"L" level output voltage	V_{OL}	$I_O=12.0mA$ $V_I=V_{DD}$ or V_{SS}			0.4	V
Peak output current	I_{OH} (Peak)	Maximum permissible rating (not guaranteed operating value)	-12			mA
Peak output current	I_{OL} (Peak)	Maximum permissible rating (not guaranteed operating value)			36	mA

Tristate outputs: Y0 to Y7

"H" level output voltage	V_{OH}	$I_O=-4.0mA$ $V_I=V_{DD}$ or V_{SS}	$V_{DD}-0.6$			V
"L" level output voltage	V_{OL}	$I_O=12.0mA$ $V_I=V_{DD}$ or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_O =high-impedance state $V_I=V_{DD}$ or V_{SS} $V_O=V_{DD}$ or V_{SS}			± 10	μA
Peak output current	I_{OH} (Peak)	Maximum permissible rating (not guaranteed operating value)	-12			mA
Peak output current	I_{OL} (Peak)	Maximum permissible rating (not guaranteed operating value)			36	mA

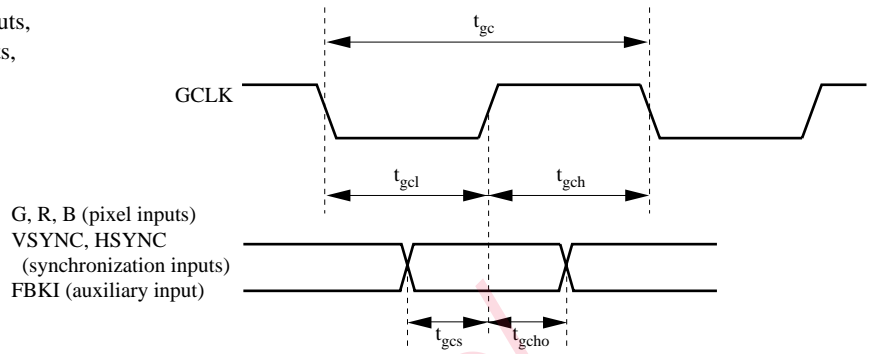
TTL level I/O: D0 to D9

"H" level input voltage	V_{IH1}		2.0		V_{DD}	V
"L" level input voltage	V_{IL1}		0		0.8	V
"H" level output voltage	V_{OH}	$I_O=-2.0mA$ $V_I=V_{DD}$ or V_{SS}	$V_{DD}-0.6$			V
"L" level output voltage	V_{OL}	$I_O=4.0mA$ $V_I=V_{DD}$ or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_O =high-impedance state $V_I=V_{DD}$ or V_{SS} $V_O=V_{DD}$ or V_{SS}			± 10	μA
Peak output current	I_{OH} (Peak)	Maximum permissible rating (not guaranteed operating value)	-6			mA
Peak output current	I_{OL} (Peak)	Maximum permissible rating (not guaranteed operating value)			12	mA

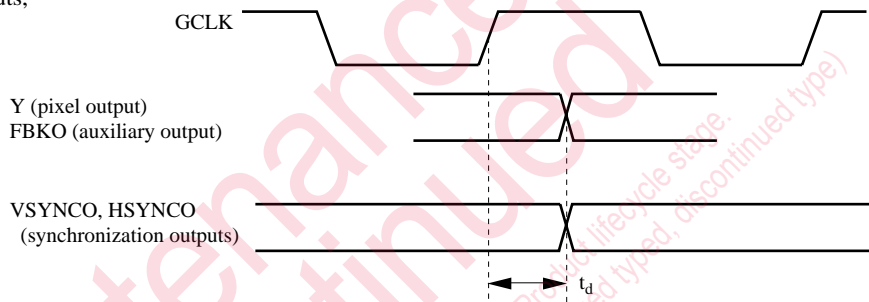
■ Timing Specifications

Conditions: $T_a=0$ to 70°C , $V_{DD}=5\text{V}\pm 5\%$, $V_{\text{ith}}=1.3\text{V}$, $V_{\text{OTH}}=1.3\text{V}$, Output load = 75pF

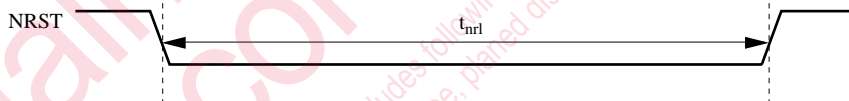
- (1) Pixel clock, pixel inputs, synchronization inputs, auxiliary input



- (2) Pixel clock, pixel outputs, synchronization outputs, auxiliary output



- (3) Reset

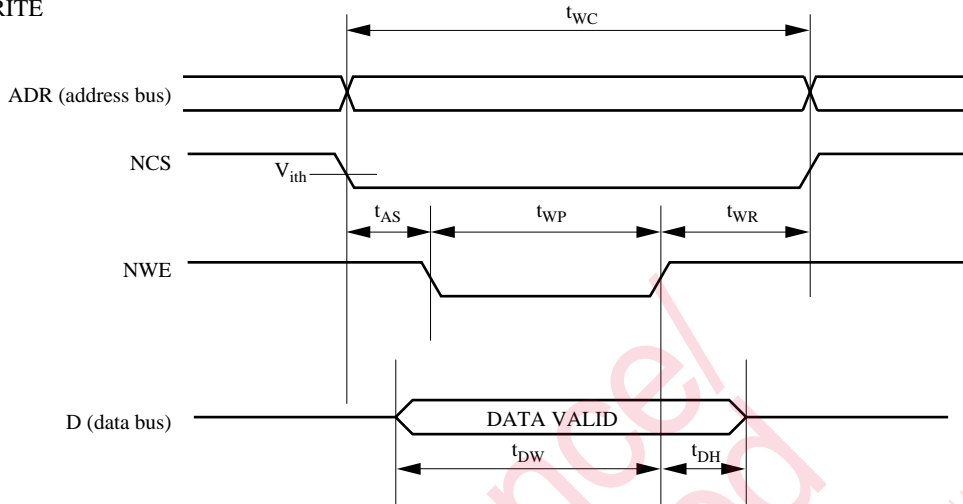


Item	Symbol	Timing specifications (ns)		
		min	typ	max
GCLK clock frequency	t_{gc}	62.5		
GCLK "H" interval	t_{gch}	30		
GCLK "L" interval	t_{gcl}	30		
GCLK setup time	t_{gcs}	10		
GCLK hold time	t_{gcho}	5		
Output delay time	t_d	5		50
NRSTL interval	t_{nrl}	25		

■ Timing Specifications (continued)

Conditions: $T_a=0$ to 70°C , $V_{DD}=5\text{V}\pm 5\%$, $V_{\text{ith}}=1.3\text{V}$, $V_{\text{Oth}}=1.3\text{V}$, Output load = 75pF

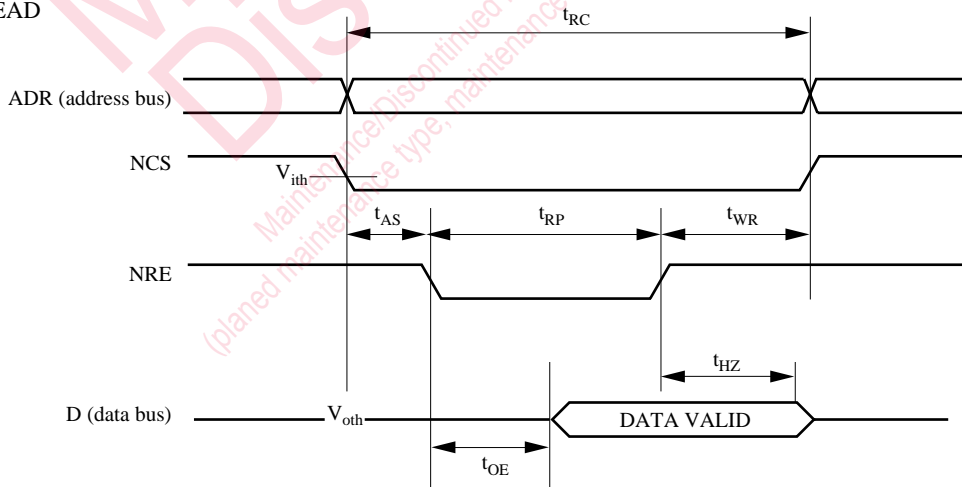
(4) WRITE



Item	Symbol	Timing specifications (ns)		
		min	typ	max
Write cycle time	t_{WC}	45		
Address setup time	t_{AS}	9		
Write pulse width	t_{WP}	18		
Address hold time	t_{WR}	9		
Input data setup time	t_{DW}	18		
Input data hold time	t_{DH}	8		

The write operation proceeds when both NCS and NWE are asserted.

(5) READ



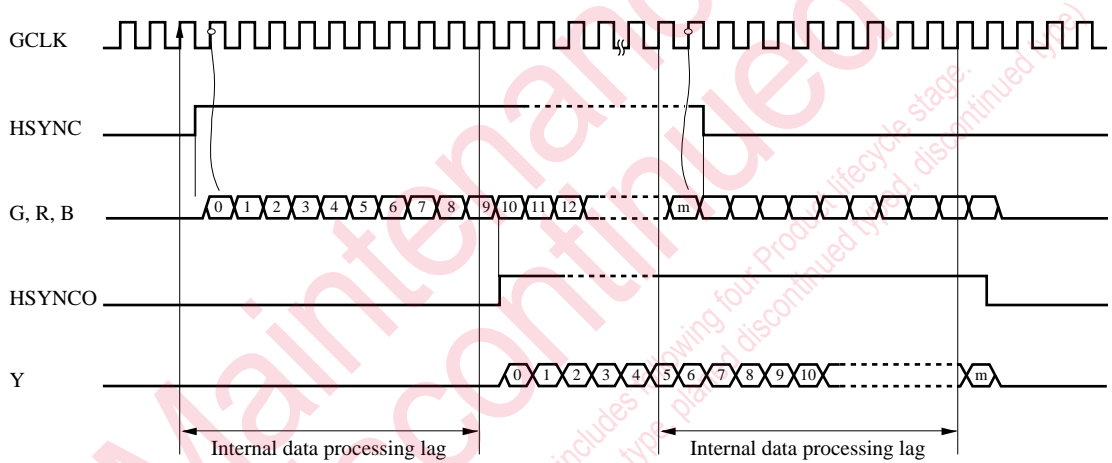
■ Timing Specifications (continued)

Conditions: $T_a=0$ to 70°C , $V_{DD}=5\text{V}\pm 5\%$, $V_{\text{ith}}=1.3\text{V}$, $V_{\text{OTH}}=1.3\text{V}$, Output load = 75pF

Item	Symbol	Timing specifications (ns)		
		min	typ	max
Read cycle time	t_{RC}	68		
NRE access time	t_{OE}	8		40
Address setup time	t_{AS}	20		
Read pulse width	t_{RP}	40		
Address hold time	t_{WR}	8		
Output data hold time	t_{HZ}	5		35

The read operation proceeds when both NCS and NRE are asserted.

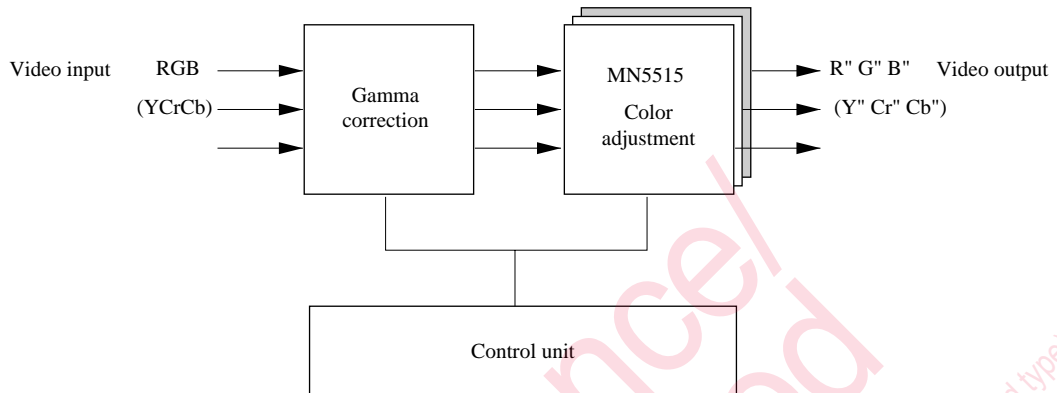
(6) Pixel data timing chart (GCLK, HSYNC, G, R, B, Y, HSYNCO)



■ Application Block Diagrams

Digital Video Equipment

● Color corrector

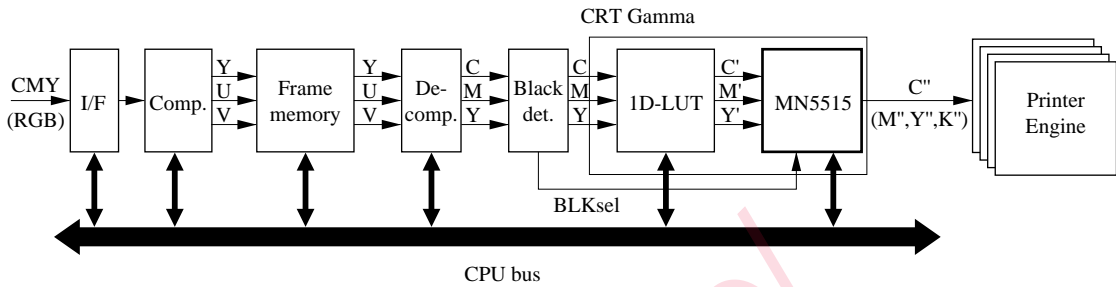


Key functions:

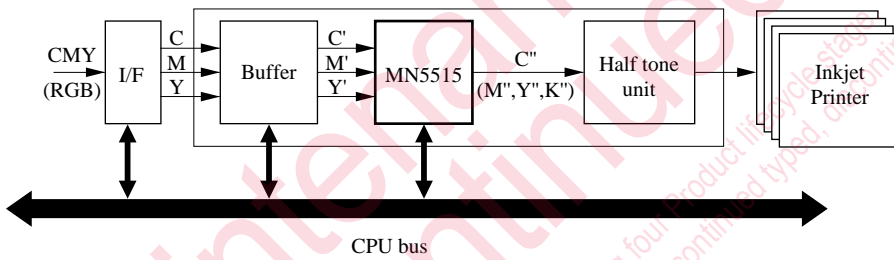
- Adjusting Cr and Cb
- Color masking: FV conversion
- White balance: Color temperature conversion

Color Printers and Scanners

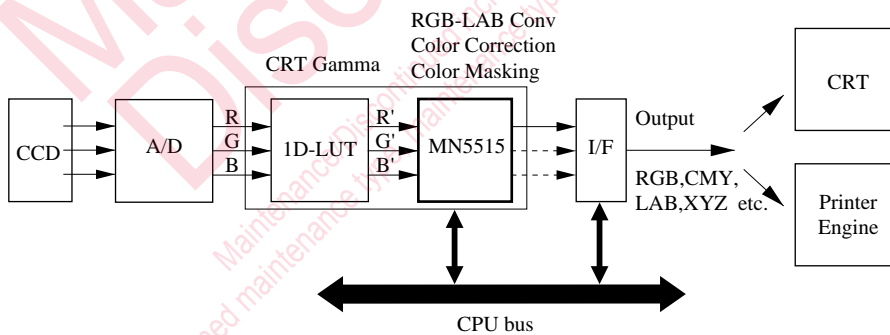
● Laser printer



● Ink jet printer



● Color scanner

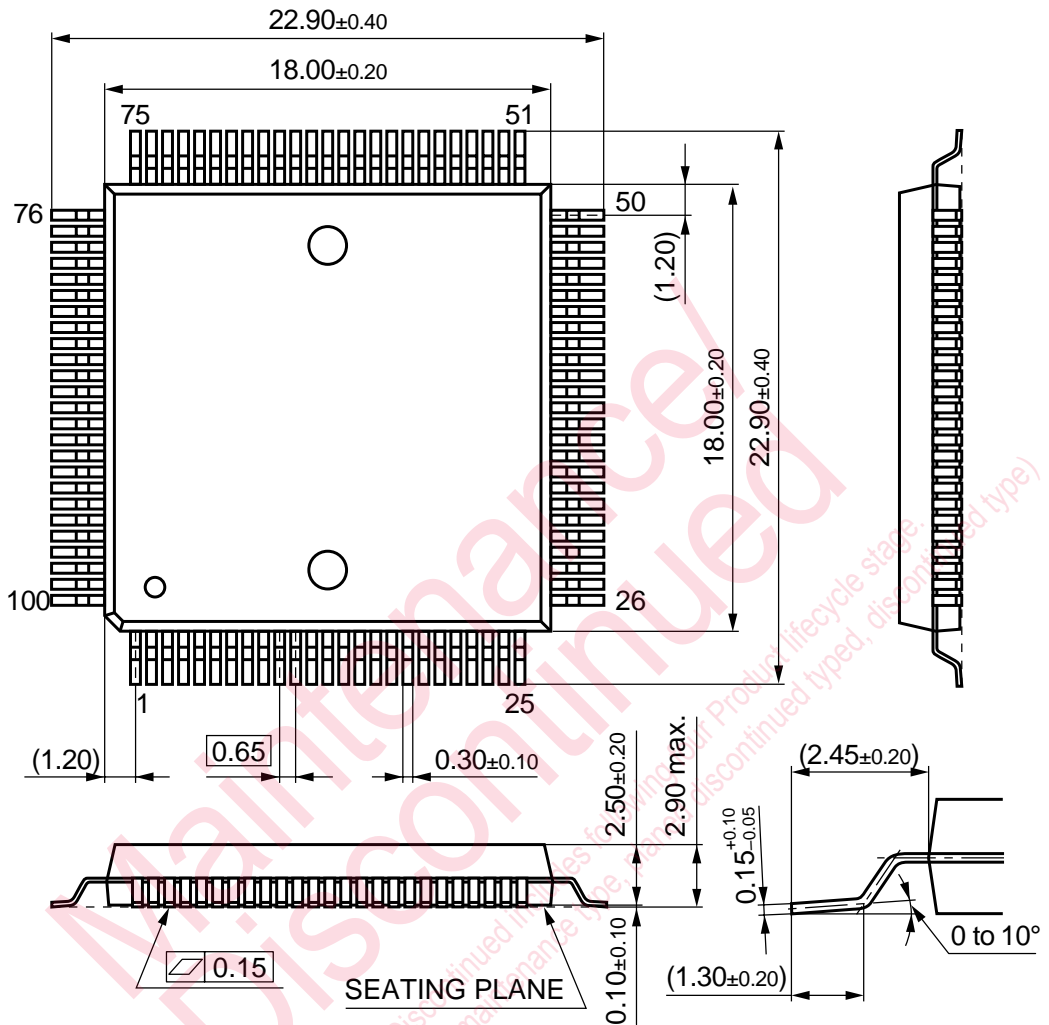


Key functions:

- Adjusting color saturation and color hue
- Color management to maintain consistency between original image, printer, and CRT display
- Color-space conversion between RGB, CMY, XYZ, LAB, etc.

■ Package Dimensions (Unit: mm)

QFP100-P-1818



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