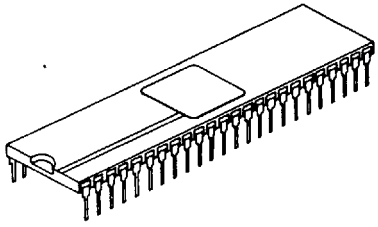
TS 68230

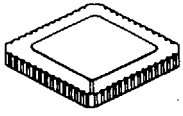
HMOS HIGH DENSITY N-CHANNEL SILICON-GATE PARALLEL INTERFACE / TIMER

DESCRIPTION

The TS 68230 parallel interface/timer (PI/T) provides versatile double buffered parallel interfaces and a system oriented timer for TS 68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether each port pin is on input or output. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or auto-vectored interrupts, and also provide a DMA request pin for connection to a direct memory access controller (DMAC) or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.



C suffix
DIL 48
Ceramic Side Brazed package



E suffix
LCCC 52
Leadless Ceramic Chip Carrier

See the Ordering Information at the end of the data sheet.

MAIN FEATURES

- TS 68000 bus compatible.
- Port modes include :
  - Bit I/O,
  - Unidirectional 8-bit and 16-bit,
  - Bidirectional 8-bit and 16-bit,
- Programmable handshaking options.
- 24-bit programmable timer modes.
- Five separate interrupt modes.
- Separate port and timer interrupt service requests.
- Registers are read/write and directly addressable.
- Registers are addressed for MOVEP (move peripheral) and DMAC compatibility.
- V_{CC} = 5 V_{DC} ±5 %.

SCREENING / QUALITY

This part is manufactured in full compliance with :

- DESC/SMD 5962-93170.
- MIL-STD-883, class B.
- TCS standard.

SUMMARY

A - GENERAL DESCRIPTION

1 - INTRODUCTION

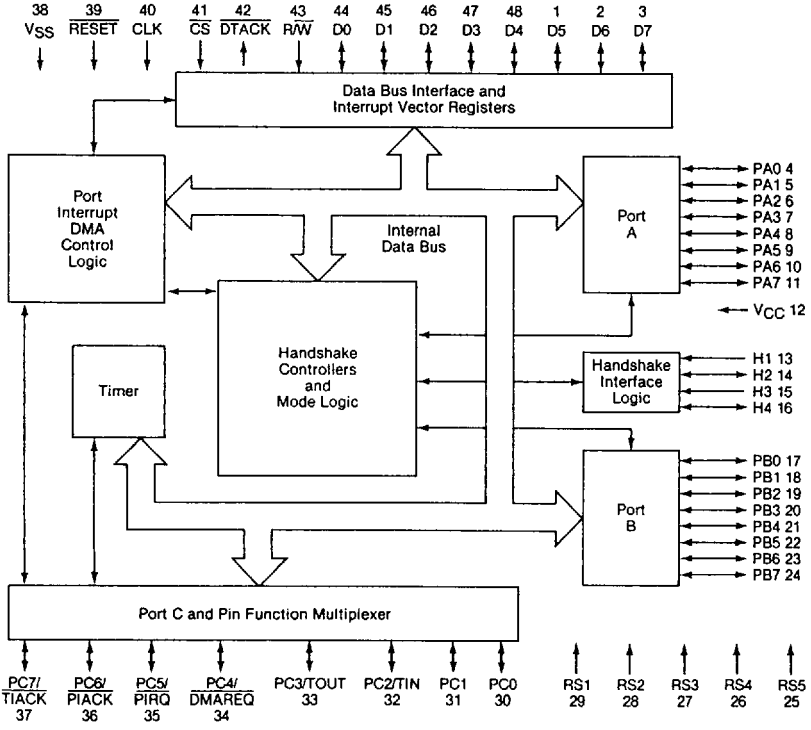


Figure 1 : TS 68230 block diagram.

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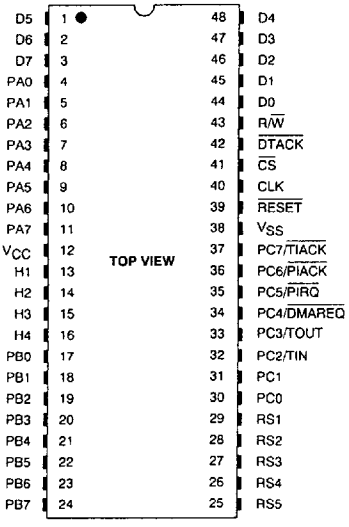
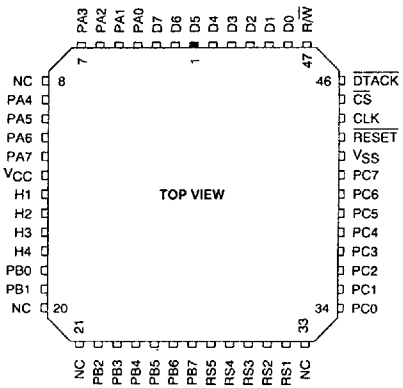
2 · PIN ASSIGNMENTS



DIL 48



LCCC 52

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the peripheral TS 68230 processes in HMOS technology and class B in compliance with the MIL-STD-883.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-PRF-38535, appendix A : general specification for microcircuits.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be as shown in § A.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-STD-1835.

3.2.3 - Package

The microcircuits are packaged in a hermetically sealed ceramic package which is conformed to case outlines of MIL-STD-1835.

- 48-lead DIP case outline : D-14
- 52-Terminal SQ.LCC case outline : C-6

The precise case outlines are described in § 8 of this document.

3.3 - Electrical requirements

3.3.1 - Absolute maximum ratings

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	+7.0	V
V_I	Input voltage		−0.3	+7.0	V
P_d	Power dissipation	T_{case} = −55°C		800	mW
		T_{case} = +125°C		500	mW
T_c	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{lead}	Lead temperature	Max. 5 sec. soldering		+270	°C

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3.3.2 - Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal.

Symbol	Parameter	Model	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_{IL}	Low level input voltage (except input H1, H2, H3, H4)		0	0.8	V
V_{IL}	Low level input H1, H2, H3, H4		0	0.5	V
V_{IH}	High level input voltage		2.0	5.25	V
T_{case}	Operating temperature		−55	+125	°C
R_L	Value of output load resistance		see Note		Ω
C_L	Output loading capacitance			see Note	pF
$t_{r(c)}$	Clock rise time (see Figure 2)			10	ns
$t_{f(c)}$	Clock fall time (see Figure 2)			10	ns
f_c	Clock frequency (see Figure 2)	TS 68230-8	2	8	MHz
		TS 68230-10	2	10	
t_{cyc}	Cycle time (see Figure 2)	TS 68230-8	125	500	ns
		TS 68230-10	100	500	
$t_{w(cL)}$	Clock pulse width low (see Figure 2)	TS 68230-8	55	250	ns
		TS 68230-10	45	250	
$t_{w(cH)}$	Clock pulse width high (see Figure 2)	TS 68230-8	55	250	ns
		TS 68230-10	45	250	

Note : Load network number 1 and 2 as specified in (Figure 5.2.2) gives the maximum loading of the relevant output.

3.3.3 · Electrical performance conditions

The electrical performance characteristics are specified in Tables 1 and 2 and are applied over full operating temperature range unless otherwise specified (see § 10).

3.4 · Mechanical and environmental

The microcircuits shall meet all mechanical and environmental requirements of MIL-STD-883 for class B devices.

3.5 · Marking

The documents where are defined the marking are identified in the reference documents (3) to (8).

Each microcircuit are legible and permanently marked with the following informations as minimum :

3.5.1 · Thomson logo
3.5.2 · Manufacturer's part number
3.5.3 · class B identification
3.5.4 · Date-code of inspection lot
3.5.5 · ESD identifier if available
3.5.6 · Country of manufacturing

3.6 · Thermal characteristics

Symbol	Parameter	Value	Unit
$\theta_{J\text{-}C}$	Thermal resistance junction to case DIL 48	10	°K/W
$\theta_{J\text{-}C}$	Thermal resistance junction to case LCC 52	6	°K/W
$\theta_{J\text{-}A}$	Thermal resistance junction to ambient DIL 48	45	°K/W
$\theta_{J\text{-}A}$	Thermal resistance junction to ambient LCC 52	50	°K/W

4 · QUALITY CONFORMANCE INSPECTION

4.1 · MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883.

Group A & B inspection are performed on each inspection lot or as specified in method 5005 of MIL-STD-883.

Group C & D are performed on a periodic basis in accordance with MIL-M-38510.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 1 : Static electrical characteristics for all electrical variants.
- Table 2A : Dynamic electrical characteristics for 68230-8 (8 MHz).
- Table 2B : Dynamic electrical characteristics for 68230-10 (10 MHz).

For static characteristics (Table 1), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to § 5.2 / 5.3 / 5.6.5 of this specification (Tables 2A and 2B).

Indication of «min» or «max» in the column «Test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.3 here above.

5.2 · Test conditions specific to the device

5.2.1 · Loading network

The applicable loading network shall be as defined in column «Test conditions» of Tables 2A and 2B, refering to the loading network number as shown in figure below.

Load NBR	Figure	R1	R2	C1	Output application
B	5.2.2.1	750	19 k	82 pF	D0-D7
T	5.2.2.2	1.62 k	24.3 k		PC0, PC1, PC2, PC4, PC6, PC7
S	5.2.2.3	1.62 k	16.2 k		PA0-PA7, H2, H4, PB0-PB7
U	5.2.2.4	475			PC5, PC3
E	5.2.2.5	750		82 pF	$\overline{\text{DTACK}}$

5.2.2 · Figures

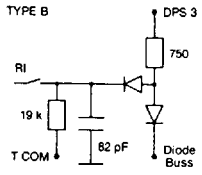

Figure 5.2.2.1

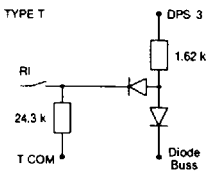

Figure 5.2.2.2

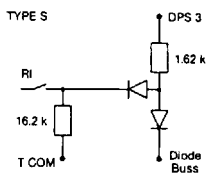

Figure 5.2.2.3

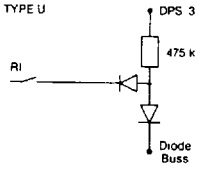

Figure 5.2.2.4

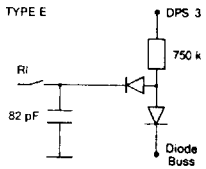

Figure 5.2.2.5

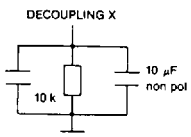

Figure 5.2.2.6

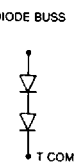

Figure 5.2.2.7

5.3 - Time definition

5.3.1 - Read and write cycle timings

1 - See 1.4 Bus Interface Operation for exception.

2 - This specification only applies if the PI/T had completed all operations initiated by previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted if $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

3 - Assuming the RS1-RS5 to data valid time has also expired.

4 - This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.

5 - Synchronized means that the input signal has been by the PI/T on the appropriate adge of the clock (rising edge for H1 (H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

6 - This limit applies to the frequency of the signal at TIN compared to the fraquency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90 % of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100 % of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an "AND" function of the clock and a control signal.

7 - CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.

5.3.2 - Peripheral input timings

1 - This specification assures recognition of the asserted edge to H1 (H3).

2 - This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

3 - The maximum value is caused by a peripheral access (H1) (H3) asserted and bus access (CS asserted) occuring at the same time.

4 - Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1 (H3) and falling edge for CS). (Refer to the 1.4 Bus Interface Operation for the exception concerning CS).

5 - If the setup time on the rising edge of the clock is not met, H1 (H3) may not be recognized until the next rising of the clock.

5.3.3 - Peripheral output timings

1 - This specification assures recognition of the asserted edge to H1 (H3).

2 - This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).

3 - The maximum value is caused by a peripheral access (H1) (H3) asserted and bus access ($\overline{CS}$ asserted) occuring at the same time.

4 - Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1 (H3) and falling edge for $\overline{CS}$). (Refer to the 1.4 Bus Interface Operation for the exception concerning $\overline{CS}$).

5 - If the setup time on the rising edge of the clock is not met, H1 (H3) may not be recognized until the next rising of the clock.

5.4 - Static characteristics for all covered models

Table 1

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
1	I_{CC}	Supply current	41	V_{CC} = 5.25 V	all		133	mA
2	V_{OL}	Low level output PC3/TOUT, PC5/$\overline{PIRQ}$	37	I_{OL} = 8.8 mA V_{CC} = 4.75 V	all		0.5	V
3	V_{OL}	Low level output voltage D0/D7, $\overline{DTACK}$	37	I_{OL} = 5.3 mA V_{CC} = 4.75 V	all		0.5	V
4	V_{OL}	Low level output voltage PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	37	I_{OL} = 2.4 mA V_{CC} = 4.75 V	all		0.5	V
5	V_{OH}	High level output D0-D7, $\overline{DTACK}$	37	I_{OH} = −400 µA V_{CC} = 4.75 V	all	2.4		V
6	V_{OH}	High level output voltage H2, H4, PB0-PB7, PA0-PA7	37	I_{OH} = −150 µA V_{CC} = 4.75 V	all	2.4		V
7	V_{OH}	High level output voltage PC0-PC7	37	V_{OH} = −100 µA V_{CC} = 4.75 V	all	2.4		V
8	I_{IH}	High level input current H1, H3, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$ 1) Other inputs at 0 2) Other inputs at 1		V_{IN} = 5.25 V	all		10	µA
9	I_{IL}	Low level input current H1, H3, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$ 1) Other inputs at 0 2) Other inputs at 1		V_{IN} = 0 V	all	−10		µA
10	I_{LO}	Power off leakage			all	−10	+10	µA
11	I_{OZH1}	Tristate input high leakage $\overline{DTACK}$, PC0-PC7, D0-D7		V_{IH} = 2.4 V V_{CC} = 5.25 V	all	−20	+20	µA
12	I_{OZH2}	Tristate input high leakage H2, H4, PA0-PA7, PB0-PB7		V_{IH} = 2.4 V V_{CC} = 5.25 V	all	−0.1	+0.1	mA
13	I_{OZL1}	Tristate input low leakage $\overline{DTACK}$, PC0-PC7, D0-D7		V_{IH} = 0.4 V V_{CC} = 5.25 V	all	−20	+20	µA
14	I_{OZL2}	Tristate input low leakage H2, H4, PA0-PA7, PB0-PB7		V_{IH} = 0.4 V V_{CC} = 5.25 V	all	−0.1	+0.1	mA
15	V_{IH}	High level input voltage (all inputs)			all	2.0	V_{CC} +0.3	V
16	V_{IL}	Low level input voltage (all inputs except H1, H2, H3, H4)			all	−0.3	0.8	V
16A	V_{IL}	Low level input voltage (inputs H1, H2, H3, H4)			all	−0.3	0.5	V
97	C_{IN}	Input capacitance (all inputs)	method 11	Reverse voltage = 0 V f = 1.0 MHz	25°C		25	pF
					min		NA	
			IEC 748-2		max		NA	
98	C_{OUT}	Input capacitance (all inputs)	method 11	Reverse voltage = 0 V f = 1.0 MHz	25°C		25	pF
					min		NA	
			IEC 748-2		max		NA	
99	V_{ESD}	Internal protection Transient energy rating	See 5.3	See 5.3	25°C	−500	+500	V
					min	NA	NA	
				5 cycles	max	NA	NA	

* IEC measurement method number unless otherwise stated.

5.5 - Dynamic (switching) characteristics - TS 68230-8

5.5.1 - Read and write cycle timings - TS 68230-8

Table 2A

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
17	t_{su} (TRVSL)	R/$\overline{W}$, RS1-RS5 valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 1	See 5.6.5 (a) to (c) f_C = 8 MHz	0		ns
18	t_h (TSRI)	$\overline{CS}$ low to R/$\overline{W}$ and RS1-RS5 invalid (Note 1)	Fig. 3, 4 Ref. 2	See test 17	100		ns
19	t_{su} (TSLCL)	$\overline{CS}$ low to CLK low (Note 2)	Fig. 3, 4 Ref. 2	See test 17	30		ns
20	t_{phl} t_{plh} (TSLDV)	$\overline{CS}$ low to data out valid (Note 3)	Fig. 3, 4 Ref. 4	See test 17 Load B		75	ns
21	t_{phl} t_{plh} (TRLDV)	RS1-RS5 valid to data out valid	Fig. 3, 4 Ref. 5	See test 17 Load B		140	ns
22	t_{phl} (TCLDL)	CLK low to $\overline{DTACK}$ low (read-write cycle time)	Fig. 3, 4 Ref. 6	See test 17 Load E	0	70	ns
23	t_h (TDTLSH)	$\overline{DTACK}$ low to $\overline{CS}$ high (Note 4)	Fig. 3, 4 Ref. 7	See test 17	0		ns
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 3, 4 Ref. 9	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 3, 4 Ref. 9	See test 17 Load B		50	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high	Fig. 3, 4 Ref. 10	See test 17 Load E	0	50	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high (to $\overline{DTACK}$ high Z)	Fig. 3, 4 Ref. 11	See test 17 Load E	0	100	ns
28	t_{su} (TDVSL)	Data in valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 12	See test 17	0		ns
29	t_h (TSLDI)	$\overline{CS}$ low to data in invalid	Fig. 3, 4 Ref. 13	See test 17 Load B	100		ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 3, 4 Ref. 13	See test 17 Load T		3	CLK. per
32	t_{phl} (TSSCLDMA)	Synchronized $\overline{CS}$ to CLK low on which $\overline{DMAREQ}$ is asserted (Note 5)	Fig. 3, 4 Ref. 32	See test 17 Load T	3	3	CLK. per
33	t_{phl} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 35	See test 17 Load T	0	120	ns
34	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 36	See test 17 Load T	0	120	ns
35	t_{phl} (TSHCLPIA)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is asserted	Fig. 3, 4 Ref. 37	See test 17 Load U	3	3	CLK. per
36	t_{phl} (TSHCLPIZ)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is high Z (Note 5)	Fig. 3, 4 Ref. 38	See test 17 Load U	3	3	CLK. per
37	t_{plz} t_{phl} (TCLPLZ)	CLK low to $\overline{PIRQ}$ low or high-Z	Fig. 3, 4 Ref. 39	See test 17 Load U	0	250	ns

5.5.1 · Read and write cycle timings · TS 68230-8 (Continued)

Table 2A

$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
38	t_{cy} (TINPN)	TIN frequency (external CLK) prescaler used (Note 6)	Fig. 3, 4 Ref. 40	See test 17	0	1	f clk (HZ) (Note 7)
39	t_{cy} (TINPN)	TIN frequency (external CLK) prescaler not used	Fig. 3, 4 Ref. 41	See test 17	0	1/8	f clk (HZ) (Note 7)
40	t_w (TIWEC)	TIN pulse width high or low (external CLK)	Fig. 3, 4 Ref. 42	See test 17	55		ns
41	t_w (TIWRH)	TIN pulse width low (RUN/ halt control)	Fig. 3, 4 Ref. 43	See test 17	1		CLK. per
42	t_{plh} t_{plz} (TCTHZ)	CLK low to tout high, low or H-Z	Fig. 3, 4 Ref. 44	See test 17 Load U	0	250	ns
43	t_{phl} (SHSL)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ low	Fig. 3, 4 Ref. 45	See test 17 Load T	50		ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.1.

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5.5.2 · Peripheral input timings · TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
44	t_{su} (TDVHA)	Port input data valid to H1 (H3) asserted	Fig. 5 Ref. 14	See test 17	100		ns
45	t_h (THADI)	H1 (H3) asserted to port data invalid	Fig. 5 Ref. 15	See test 17 Load B	20		ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 5 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 5 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 5 Ref. 18	See test 17 Load S		150	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 5 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Note 3, 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 5 Ref. 23	See test 17 Load T		3	CLK. per
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17	50		ns

5.5.2 · Peripheral input timings · TS 68230-8 (Continued)

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
54	t_{plh} (TSHCLHA)	Synchronized H1 (H3) to CLK low on which H2 (H4) asserted (Note 3, 4)	Fig. 5 Ref. 33	See test 17 Load S		4.5	ns
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 5 Ref. 35	See test 17 Load T	0	120	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 5 Ref. 36	See test 17 Load T	0	120	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.2.

5.5.3 · Peripheral output timings · TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 6 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 6 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 6 Ref. 18	See test 17 Load S		150	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 6 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 6 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 6 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Note 3, 4)	Fig. 6 Ref. 22	See test 17 Load t	2.5	3.5	ns
30	t_{plh} (TCDMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 6 Ref. 23	See test 17 Load T	2.5	3	CLK. per
55	t_{plh} t_{phl} (TCLPOD)	CLK low to port output data valid (Modes 0 or 1)	Fig. 6 Ref. 24	See test 17 Load B		150	ns
56	t_{phl} t_{plh} (TSHDI)	Synchronized H1 (H3) to port output data invalid (Note 3, 4) (Mode 0 and 1)	Fig. 6 Ref. 25	See test 17 Load B	1.5	2.5	CLK per.
57	t_{phl} t_{plh} (THNDV)	H1 negated to port output data valid (Mode 2 and 3)	Fig. 6 Ref. 26	See test 17 Load B		70	ns
58	t_{phz} t_{plz} (THADZ)	H1 asserted to port output data high-Z (Mode 2 and 3)	Fig. 6 Ref. 27	See test 17 Load B		70	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 6 Ref. 30	See test 17 Load T	50		ns
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 6 Ref. 35	See test 17 Load T	0	120	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 6 Ref. 36	See test 17 Load T	0	120	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.3.

5.5.4 · IACK timings - TS 68230-8

Table 2A

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 7 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSDHZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 7 Ref. 9	See test 17 Load B		50	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 10	See test 17 Load E		50	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 11	See test 17 Load E		100	ns
59	t_{plh} t_{phl} (TCLDVIAC)	CLK low to data output valid interrupt acknowledge	Fig. 7 Ref. 29	See test 17 Load B		120	ns
60	t_{su} (TILCL)	$\overline{PIACK}$ to $\overline{TIACK}$ low to CLK low	Fig. 7 Ref. 31	See test 17	50		ns
61	t_{phl} (TCLDLIAC)	CLK low to $\overline{DTACK}$ low interrupt acknowledge	Fig. 7 Ref. 34	See test 17 Load E		100	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

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5.6 · Dynamic (switching) characteristics - TS 68230-10

5.6.1 · Read and write cycle timings - TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
17	t_{su} (TRVSL)	R/$\overline{W}$, RS1-RS5 valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 1	See 5.6.5 (a) to (c) f_C = 8 MHz	0		ns
18	t_h (TSRI)	$\overline{CS}$ low to R/$\overline{W}$ and RS1-RS5 invalid (Note 1)	Fig. 3, 4 Ref. 2	See test 17	65		ns
19	t_{su} (TSLCL)	$\overline{CS}$ low to CLK low (Note 2)	Fig. 3, 4 Ref. 3	See test 17	20		ns
20	t_{phl} t_{plh} (TSLDV)	$\overline{CS}$ low to data out valid (Note 3)	Fig. 3, 4 Ref. 4	See test 17 Load B		60	ns
21	t_{phl} t_{plh} (TRLDV)	RS1-RS5 valid to data out valid	Fig. 3, 4 Ref. 5	See test 17 Load B		105	ns
22	t_{phl} (TCLDL)	CLK low to $\overline{DTACK}$ low (read-write cycle time)	Fig. 3, 4 Ref. 6	See test 17 Load E	0	60	ns
23	t_h (TDTLSH)	$\overline{DTACK}$ low to $\overline{CS}$ high (Note 4)	Fig. 3, 4 Ref. 7	See test 17	0		ns
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 3, 4 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 3, 4 Ref. 9	See test 17 Load B		45	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high	Fig. 3, 4 Ref. 10	See test 17 Load E		45	ns

5.6.1 - Read and write cycle timings - TS 68230-10 (Continued)

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 3, 4 Ref. 11	See test 17 Load E		55	ns
28	t_{su} (TDVSL)	Data in valid to $\overline{CS}$ low	Fig. 3, 4 Ref. 12	See test 17	0		ns
29	t_{h} (TSLDI)	$\overline{CS}$ low to data in invalid	Fig. 3, 4 Ref. 13	See test 17 Load B	65		ns
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 3, 4 Ref. 23	See test 17 Load T	2.5	3	CLK. per
31	t_{su} (TRDDTL)	Read data valid to $\overline{DTACK}$ low	Fig. 3, 4 Ref. 28	See test 17 Load E	0		ns
32	t_{phl} (TSSCLDMA)	Synchronized $\overline{CS}$ to CLK low on which $\overline{DMAREQ}$ is asserted (Note 5)	Fig. 3, 4 Ref. 32	See test 17 Load T	3	3	CLK. per
33	t_{phl} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 35	See test 17 Load T	0	100	ns
34	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ low	Fig. 3, 4 Ref. 36	See test 17 Load T	0	100	ns
35	t_{phl} (TSHCLPIA)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is asserted	Fig. 3, 4 Ref. 37	See test 17 Load U	3	3	CLK. per
36	t_{phl} (TSHCLPIZ)	Synchronized H1 (H3) to CLK low on which $\overline{PIRQ}$ is high Z (Note 5)	Fig. 3, 4 Ref. 38	See test 17 Load U	3	3	CLK. per
37	t_{plz} t_{phl} (TCLPLZ)	CLK low to $\overline{PIRQ}$ low or high-Z	Fig. 3, 4 Ref. 39	See test 17 Load U	0	225	ns
38	t_{cy} (TINPU)	TIN frequency (external CLK) prescaler used (Note 6)	Fig. 3, 4 Ref. 40	See test 17	0	1	f clk (HZ) (Note 7)
39	t_{cy} (TINPU)	TIN frequency (external CLK) prescaler not used	Fig. 3, 4 Ref. 41	See test 17	0	1/8	f clk (HZ) (Note 7)
40	t_{w} (TIWEC)	TIN pulse width high or low (external CLK)	Fig. 3, 4 Ref. 42	See test 17	45		ns
41	t_{w} (TIWRH)	TIN pulse width low (RUN/ halt control)	Fig. 3, 4 Ref. 43	See test 17	1		CLK. per
42	t_{plh} t_{plz} (TCTHZ)	CLK low to tout high, low or H-Z	Fig. 3, 4 Ref. 44	See test 17 Load U	0	225	ns
43	t_{phl} (SHSL)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ low	Fig. 3, 4 Ref. 45	See test 17 Load T	30		ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.1.

5.6.2 · Peripheral input timings · TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
30	t_{phl} (TCDAMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 5 Ref. 23	See test 17 Load T	2.5	3	CLK. per
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 5 Ref. 35	See test 17 Load T	0	100	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 5 Ref. 36	See test 17 Load T	0	100	ns
44	t_{su} (TDVHA)	Port input data valid to H1 (H3) asserted	Fig. 5 Ref. 14	See test 17	60		
45	t_h (THADI)	H1 (H3) asserted to port data invalid	Fig. 5 Ref. 15	See test 17 Load B	20		ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 5 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 5 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 5 Ref. 18	See test 17 Load S		120	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 5 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Notes 3 and 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17	40		ns
54	t_{plh} (TSHCLHA)	Synchronized H1 (H3) to CLK low on which H2 (H4) asserted (Notes 3 and 4)	Fig. 5 Ref. 33	See test 17 Load S	3.5	4.5	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.2.

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5.6.3 · Peripheral output timings - TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
30	t_{phl} (TCDMA-CDMN)	CLK low on which $\overline{DMAREQ}$ is asserted to CLK low on which $\overline{DMAREQ}$ is negated	Fig. 6 Ref. 23	See test 17 Load T	2.5	3	CLK. per
34	t_{plh} (TCLDML)	CLK low to $\overline{DMAREQ}$ low	Fig. 6 Ref. 35	See test 17 Load T	0	100	ns
35	t_{plh} (TCLDMH)	CLK low to $\overline{DMAREQ}$ high	Fig. 6 Ref. 36	See test 17 Load T	0	100	ns
46	t_w (THWA)	Handshake input H2 (H4) pulse width asserted	Fig. 6 Ref. 16	See test 17	40		ns
47	t_w (THWN)	Handshake input H2 (H4) pulse width negated	Fig. 6 Ref. 17	See test 17	40		ns
48	t_{plh} (THAHN)	H1 (H3) asserted to H2 (H4) negated	Fig. 6 Ref. 18	See test 17 Load S		120	ns
49	t_{phl} (TCLHA)	CLK low to H2 (H4) asserted	Fig. 6 Ref. 19	See test 17 Load S		100	ns
50	t_{phl} (THAHA)	H1 (H3) asserted to H2 (H4) asserted (Note 1)	Fig. 5 Ref. 20	See test 17 Load S	0		ns
51	t_{plh} (TCLHN)	CLK low to H2 (H4) pulse negated (Note 2)	Fig. 5 Ref. 21	See test 17 Load S		125	ns
52	t_{plh} (TSHCL-DMA)	Synchronized H1 (H3) to CLK low on which $\overline{DMAREQ}$ is asserted (Notes 3 and 4)	Fig. 5 Ref. 22	See test 17 Load T	2.5	3.5	ns
53	t_{su} (THACH)	H1 (H3) asserted to CLK high (Note 5)	Fig. 5 Ref. 30	See test 17 Load T	40		ns
55	t_{plh} t_{phl} (TCLPOD)	CLK low to port output data valid (Modes 0 or 1)	Fig. 5 Ref. 24	See test 17 Load B		120	ns
56	t_{phl} t_{plh} (TSHDI)	Synchronized H1 (H3) to port output data invalid (Notes 3 and 4) (Mode 0 and 1)	Fig. 5 Ref. 25	See test 17 Load B	1.5	2.5	CLK per.
57	t_{phl} t_{plh} (THNDV)	H1 negated to port output data valid (Mode 2 and 3)	Fig. 5 Ref. 26	See test 17 Load B		60	ns
58	t_{phz} t_{plz} (THADZ)	H1 asserted to port output data high-Z (Mode 2 and 3)	Fig. 5 Ref. 27	See test 17 Load B	0	70	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

Notes : See § 5.3.3.

5.6.4 - IACK timings - TS 68230-10

Table 2B

Test Nbr	Symbol	Parameter	Ref Nbr (*)	Test Conditions	Limits		Unit
					Min	Max	
24	t_{plh} t_{phl} (TSHDI)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to data out invalid	Fig. 7 Ref. 8	See test 17 Load B	0		ns
25	t_{plz} t_{phz} (TSHDZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to D0-D7 high Z	Fig. 7 Ref. 9	See test 17 Load B		45	ns
26	t_{plh} (TSHDH)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 10	See test 17 Load E		45	ns
27	t_{phz} (TSHDTZ)	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ high to $\overline{DTACK}$ high Z	Fig. 7 Ref. 11	See test 17 Load E		55	ns
59	t_{plh} t_{phl} (TCLDVIAC)	CLK low to data output valid interrupt acknowledge cycle	Fig. 7 Ref. 29	See test 17 Load B		105	ns
60	t_{su} (TILCL)	$\overline{PIACK}$ to $\overline{TIACK}$ low to CLK low	Fig. 7 Ref. 31	See test 17	40		ns
61	t_{phl} (TCLDLIAC)	CLK low to $\overline{DTACK}$ low interrupt acknowledge cycle	Fig. 7 Ref. 34	See test 17 Load E		100	ns

* Measurement method see § 5.2 / 5.3 / 5.6.5.

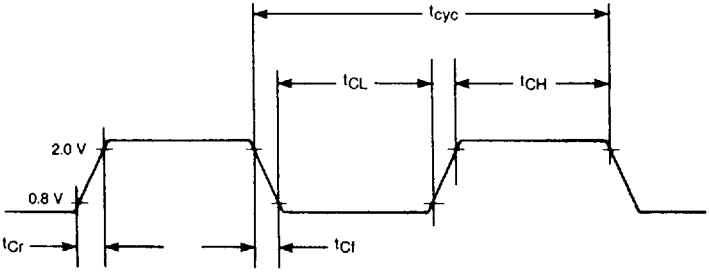

Figure 2 : Clock input timing diagram.

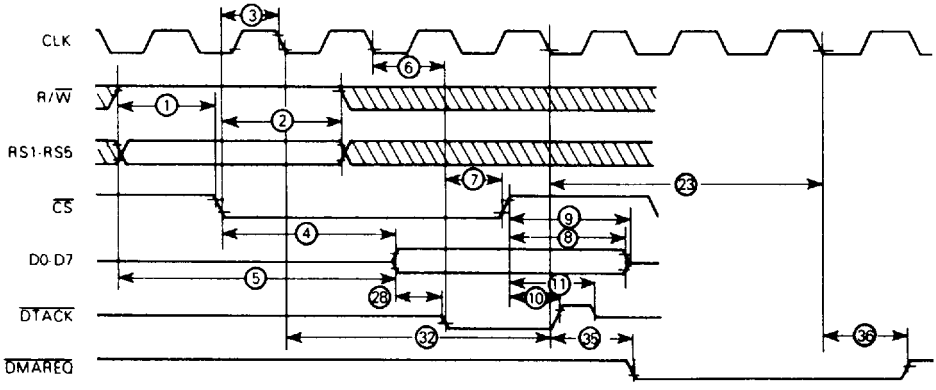

Figure 3 : Read cycle timing diagram.

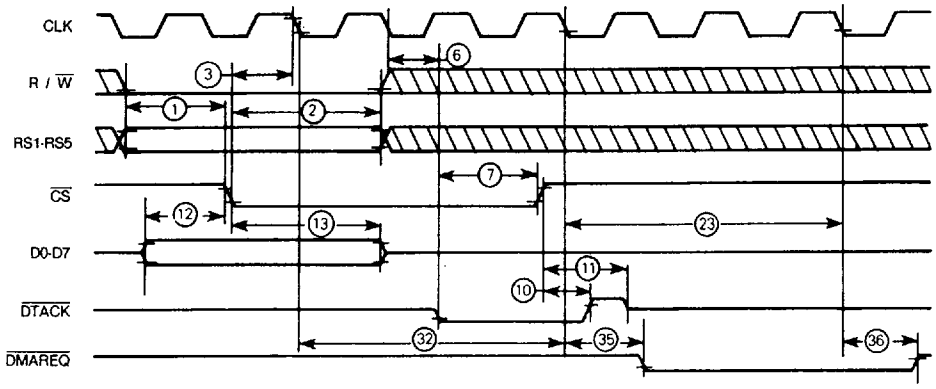

Figure 4 : Write cycle timing diagram.

Note : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

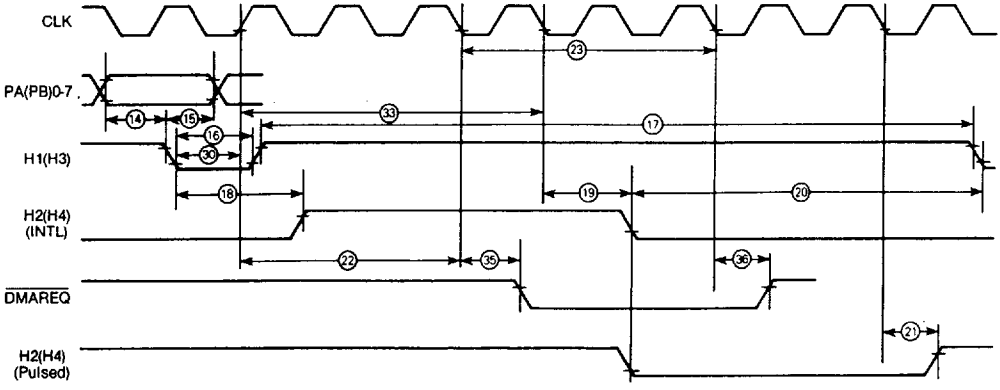

Figure 5 : Peripheral input timing diagram.

Note 1 : Timing diagram shows H1, H2, H3 and H4 asserted low.
Note 2 : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

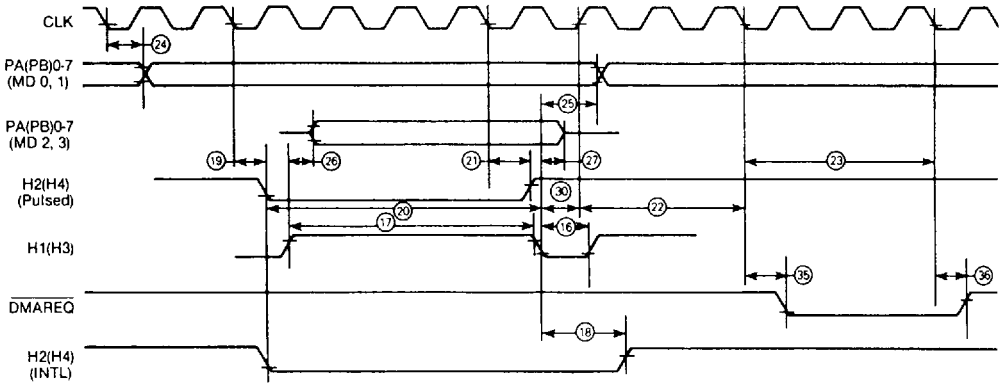

Figure 6 : Peripheral output timing diagram.

Note 1 : Timing diagram shows H1, H2, H3 and H4 asserted low.
Note 2 : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

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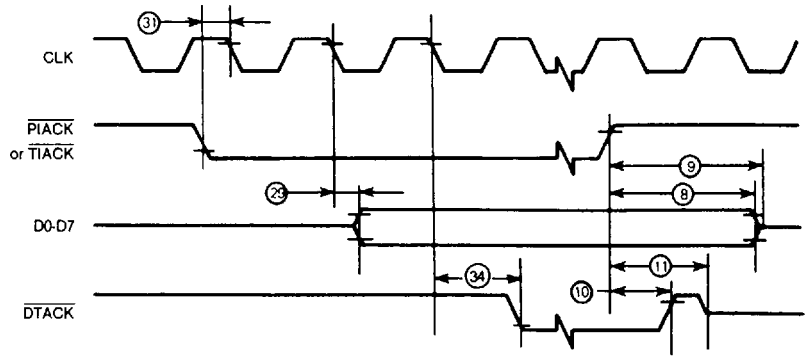


Figure 7 : IACK timing diagram.

Note : Timing requirements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.

5.6.5 · Input and output signals for dynamic measurements

a) Input pulse characteristcs

Where input pulse generator is loaded by a 90 Ω resistor, the input pulse characteristics shall be as shown in figure 8.

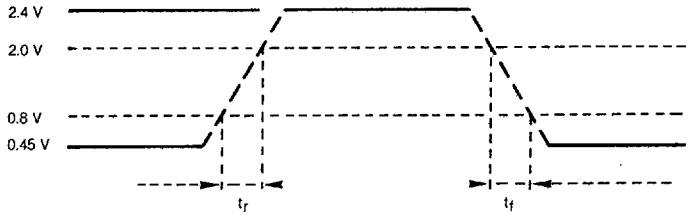


Figure 8 : Input pulse characteristics.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurements shall be :

$$V_{IL} = 0.8\ V$$
$$V_{IH} = 2.0\ V$$

c) Time measurement output voltage reference for time valid state output

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in figure 9.

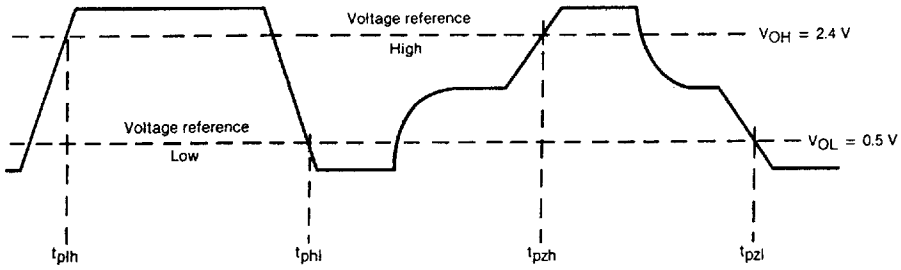


Figure 9 : Ouput voltage references.

6 · PREPARATION FOR DELIVERY

6.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

6.2 · Certificate of compliance

TCS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

7 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools, and operator.

c) Do not handle devices by the leads.

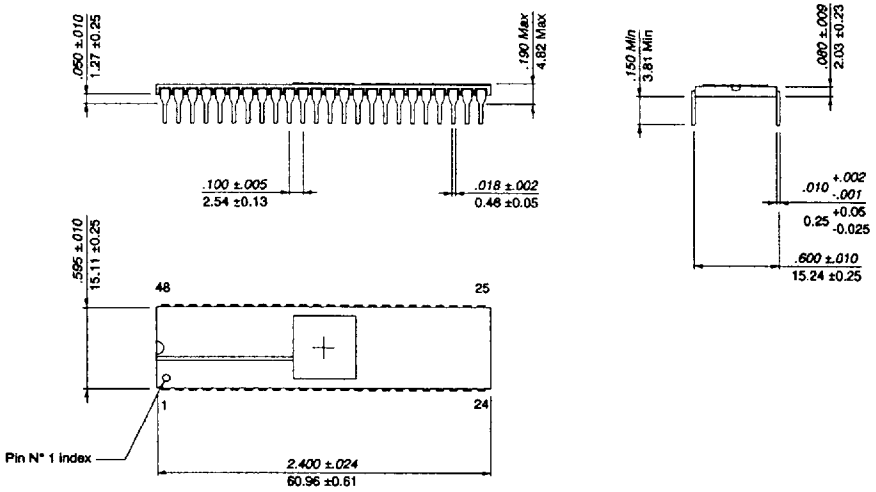
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

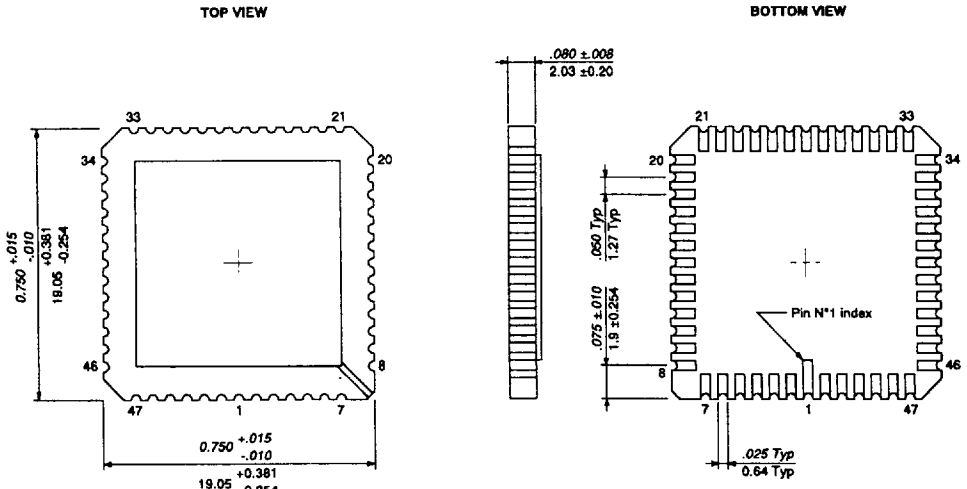
f) Maintain relative humidity above 50 percent, if practical.

8 - PACKAGE MECHANICAL DATA

8.1 - 48 pins - Ceramic Side Brazed package



8.2 - 52 pins - Leadless Ceramic Chip Carrier



9 - TERMINAL CONNECTIONS

9.1 - Ceramic DIL

See § A.2.

9.2 - LCCC

See § A.2.

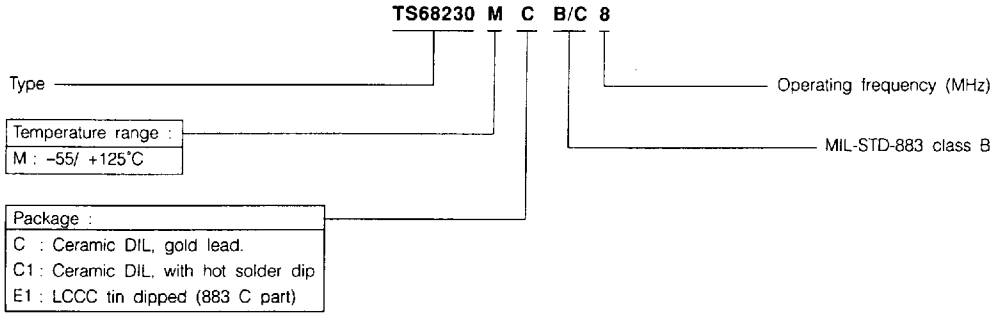
9.3 - Terminal designation of the device

The function, category and relevant symbol of each terminal of the device are given in the following table :

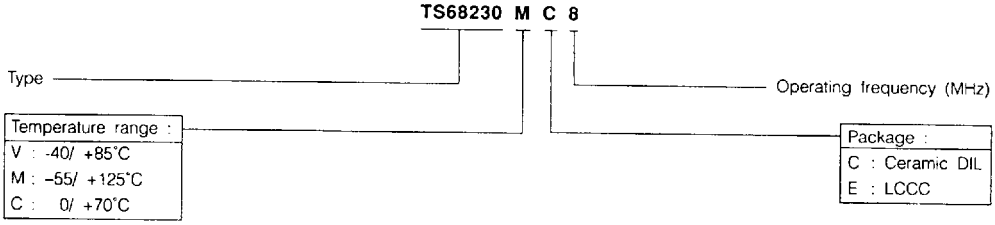
Symbol	Function	Category
V_{CC}	Power supply	Supply
V_{SS}	Power supply	Terminals
D0-D7	Bidirectionnal data bus	Bi-directionnal
RS1-RS5	Register select	Input
R/$\overline{W}$	Read / Write	Input
$\overline{CS}$	Chip select	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
$\overline{RESET}$	Reset	Input
CLK	Clock	Input
PA0-PA7 PB0-PB7	Port A and Port B	Input / Output
H1-H3	Handshake Pins	Input
H2-H4	Handshake Pins	Input or Output
PC0-PC7	Port C	Input or Output

10 - ORDERING INFORMATION

10.1 - MIL-STD-883



10.2 · Standard product



10.3 · DESC

Refer to 5962-93170.

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