



## Security & Chip Card ICs

### SLE 66C166P/PE

8/16-Bit Security Controller

with enhanced instruction set for large memories

in 0.22  $\mu\text{m}$  CMOS Technology

98-Kbytes ROM, 4352 bytes RAM, 16-Kbytes EEPROM

Dual Key Triple DES

Preliminary

Short Product Information 04.03

**This document contains preliminary information on a new product under development.  
Details are subject to change without notice.**

**Revision History: Current Version 04.03**

Previous Releases: 03.03

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## 8/16-Bit Security Controller with enhanced instruction set for large memories in 0.22µm CMOS Technology 98-Kbyte ROM, 4352 Bytes RAM, 16-Kbyte EEPROM, Dual Key Triple DES Accelerator

### Features

- 8/16-bit microcomputer in 0.22 µm CMOS technology 
  - Instruction set opcode compatible with standard SAB 8051 processor 
  - **Downward compatibility to existing SLE66CxxxP products for existing masks without using the new features**
  -  ● **Addressable memory up to 16 Mbyte**
  -  ● **Additional enhanced instructions for direct physical memory access of >64kByte**
    - Typically saves up to 90% code space and increases execution speed up to 80%.
  - Dedicated, non-standard architecture with **execution time 6 times faster** than standard SAB 8051 processor at same external clock. (Up to **18 times faster** using internal frequency PLL x 3 compared to external clock).
  -  ● **98 Kbytes User ROM** for application programs
  -  ● **16 Kbytes MicroSlim-EEPROM** for increased memory requirements in mobile applications
  - **4 Kbytes XRAM**, 256 bytes internal RAM
  -  ● **Enhanced Memory Management and Protection Unit (MMU)** with application and user defined segments
  - **Dual Key Triple DES (DDES)**
  - CC EAL5+ certification according to BSI-PP-0002 planned
  - True Random Number Generator with Firmware test function 
  - CRC Module
  - 16-bit Interrupt Module 
  - Code executions during E<sup>2</sup>-programming for faster personalization
  - EEPROM programming voltage generated on chip
  - **Internal Clock** with up to 33 MHz: Programmable internal frequency (PLL x1, x2, x3, x4 and free running mode(s)).
  - **Adjustable internal frequency according to available power or required performance**
    - Increased internal clock frequency for maximum performance
    - Internal frequency is automatically adjusted to guarantee a given limited power consumption
  - Two 16-bit Autoreload Timer
  - Power saving sleep mode
  - **Ext. Clock freq. 1 up to 7.5 MHz**
  - **UART for handling serial interface** in accordance with ISO/IEC 7816 part 3 **supporting transmission protocols T=1 and T=0**
  - Supply voltage range: 1.8 V, 3.0 V, 5.0 V
  - Support of current consumption limits by GSM / UICC applications
    - < 10 mA @ 5.5 V
    - < 6 mA @ 3.3 V
    - < 4 mA @ 1.98 V
  - Operating Temperature range: -25 to +85°C
  - Storing temperature range: -40° to +125°C
  - ESD protection larger than 6 kV (HBM)
- MicroSlim-EEPROM**
- Typical Erase + Write time ≤ 2.9 ms
  - Enhanced ECC module controlled by OS
  - Reading and programming byte by byte
  - Flash-like erasing of E<sup>2</sup>-segments up to 2 kB
  - Flexible page mode for 1 to 64 bytes write/erase operation
  - 32 bytes security area (OTP)
  - Fast personalization mode ≤ 1.0 ms
  - Minimum of 500.000 write/erase cycles @ 25°C per page. Maximum of 16.500.000 write/erase cycles per sector
  - Typical data retention of 10 years @ 25°C


**Memory Management and Protection Unit**

-  ● Addressable memory of up to 16 Mbyte
- Separates OS (system mode) and application (user mode)
- System routines called by interrupts
- OS can restrict access to peripherals in application mode
- Variable application orientated segments defined and controlled by OS
- Code execution from XRAM possible
-  ● Enhanced multi-application support by descriptors for system / application mode.

**Security Features**

- Enhanced sensor concept:
  - Low and high voltage sensors
  - Frequency sensors and filters
  - Light Sensor
  - Glitch Sensors
  - Temperature Sensor
  - Life Test Function for Sensors (UMSLC)
- Bus confusion
- Security reset detection
- Current control oscillator (ICO)

**Memory Security**

-  ● Sparkling SFR encryption for DDES and ACE, CRC module and RNG
- 32 bytes security PROM, hardware protected for batch-, wafer-, die-individual security data. Unique chip identification number for each chip
- Additional memory for customer-defined security FabKey on request
- MED – memory encryption/decryption device for XRAM, ROM and EEPROM
- Security optimized layout and layout scrambling
- Fast IRAM erase
- Enhanced Error correction unit (ECU)

**Testmode**

- Irreversible Lock - Out of test-mode

**Anti Snooping**

- Automatic randomization smoothing of power profile
- Effective HW-countermeasures against SEMA/DEMA, SPA/DPA, DFA and Timing-Attacks
- Non standard dedicated Smart Card CPU – Core
- Active Shield with automatic and user controlled attack detection
- Hardware countermeasures controlled by True Random Number Generator

**Targeted Certifications**

- CC EAL5+
- VISA
- MULTOS
- Mastercard

**Support**

- HW-& SW-Tools (Emulator, ROM Monitor, Card Emulator, Simulator, Softmasking)
- Application notes

**Supported Standards**

- ISO/IEC 7816
- EMV 2000
- GSM 11.11, 11.12, 11.18
- ETSI TS 102 221

**Document References**

- Confidential Data Book SLE 66CxxxPE
- Qualification report
- Chip delivery specification for wafer with chip-layout (die size, orientation,...)
- Module specification containing description of package, etc.
- Qualification report module

**Development Tools Overview**

- Short Product Information Software Development Kit SDK CC
- Short Product Information Card Emulator CE66P
- Short Product Information ROM Monitor RM66P
- Short Product Information Emulator ET66P Hitex or ET66P KSC
- Short Product Information Smart Mask Package

**Performance DDES- Accelerator (typical values, based on internal test results)**

Operation	Data Block Length	Encryption Time for an 8-Byte Block incl. Data Transfer <span style="float: right;">New</span>		
		5 MHz	15 MHz	33 MHz*
56-bit Single DES Encryption	64 bit	23 $\mu$ s	8 $\mu$ s	3.5 $\mu$ s
112-bit Triple DES Encryption	64 bit	35 $\mu$ s	12 $\mu$ s	5.3 $\mu$ s

\* preliminary values

**Ordering Information**

Type	Remark	Package <sup>1</sup>	Voltage Range	Temperature Range	Frequency Range (int. clock frequency)	Frequency Range (ext. clock frequency)
SLE 66C166PE C	Enhanced feature set	Die (sawn, unsawn)	1.8 V; 3.0 V; 5.0 V	- 25°C to + 70°C	Up to 33 MHz	1 MHz - 5 MHz
SLE 66C166PE M5		M5.1	3.0 V; 5.0 V	- 25°C to + 85°C		1 MHz - 7.5 MHz
SLE 66C166P C	Mask compatibility to existing SLE 66P products	Die (sawn, unsawn)	1.8 V; 3.0 V; 5.0 V	- 25°C to + 70°C	Up to 15 MHz	1 MHz - 5 MHz
SLE 66C166P M5		M5.1	3.0 V; 5.0 V	- 25°C to + 85°C		1 MHz - 7.5 MHz

For ordering information please refer to the databook and contact your sales representative.

**Production sites for SLE 66C166P/PE:**

- Dresden (Germany), UMC (Taiwan), Altis (France).

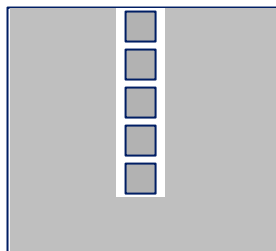
**Packaging Information:**

- New, innovative Pad design:
  - Suitable for wire bonding and future Flip-Chip technology
  - Interoperability between all new derivatives of the 66PE family


**Inline Pads**

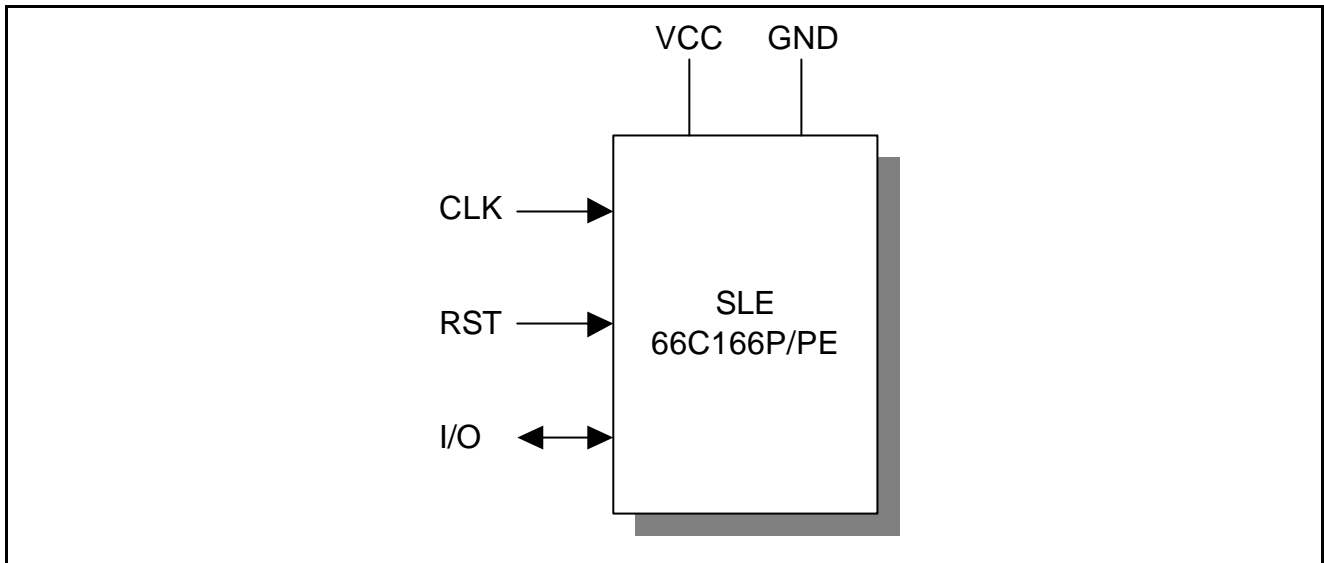
Pad size: 90 x 90  $\mu$ m

Pad Pitch: 280  $\mu$ m



<sup>1</sup> available as wire-bonded module (M5) for embedding in plastic cards or as die (C) for customer packaging

**Pin Configuration**



**Figure 1: Pin Configuration**

**Pin Definitions and Functions**

Symbol	Function
VCC	Operating voltage
RST	Reset input
CLK	Processor clock input
GND	Ground
I/O	Bi-directional data port

## General Description

The SLE66C166P/PE is a member of the improved 66PE-series of Infineon Technologies. This high performance security controller is manufactured in advanced 0.22 µm CMOS technology. It is downward compatible to existing 66P controller derivatives. The well known ECO2000 8/16 bit CPU provides the high efficiency of the SAB 8051 instruction set extended by additional powerful instructions together with enhanced performance, memory sizes and security features compared to existing 66P derivatives.

**Performance:** The internal clock frequency can be adjusted to a level up to 33 MHz either as a multiple of 1,2,3,4 to the external frequency or independent of the clock rate of the terminal with the help of the internal clock. It is adjustable according to either available power requirements or required performance:

- Increased internal clock frequency for maximum performance, e.g. for high performance with max. frequency in payment applications.
- Automatically adjusted frequency for a max. given power consumption, e.g. by GSM or UMTS requirements.



**Memory:** The SLE66C166P/PE offers 98 Kbytes of User-ROM, 256 byte internal RAM, 4096 byte XRAM and 16 Kbytes MicroSlim-EEPROM, to fulfill the increased requirements of GSM and UMTS applications. The large ROM size allows to place applications in the ROM-mask and to keep the E<sup>2</sup>PROM free for customer data. In addition it saves mask development costs, as one mask may be used for different customer projects. 16kByte of EEPROM thus allows to include include SIM Application Toolkit, Wireless Application Protocol (WAP), WML-Browser and JavaCard API implementations into the NVM.

The enhanced Memory Management and Protection Unit allows a secure separation of the operating system and different applications. It allows to separate the memories in application orientated segments, which can be controlled by the OS. Furthermore, the MMU makes a secure downloading of applications possible even after personalization of a card. These new features suit the requirements of the next generation of multi application operating systems.

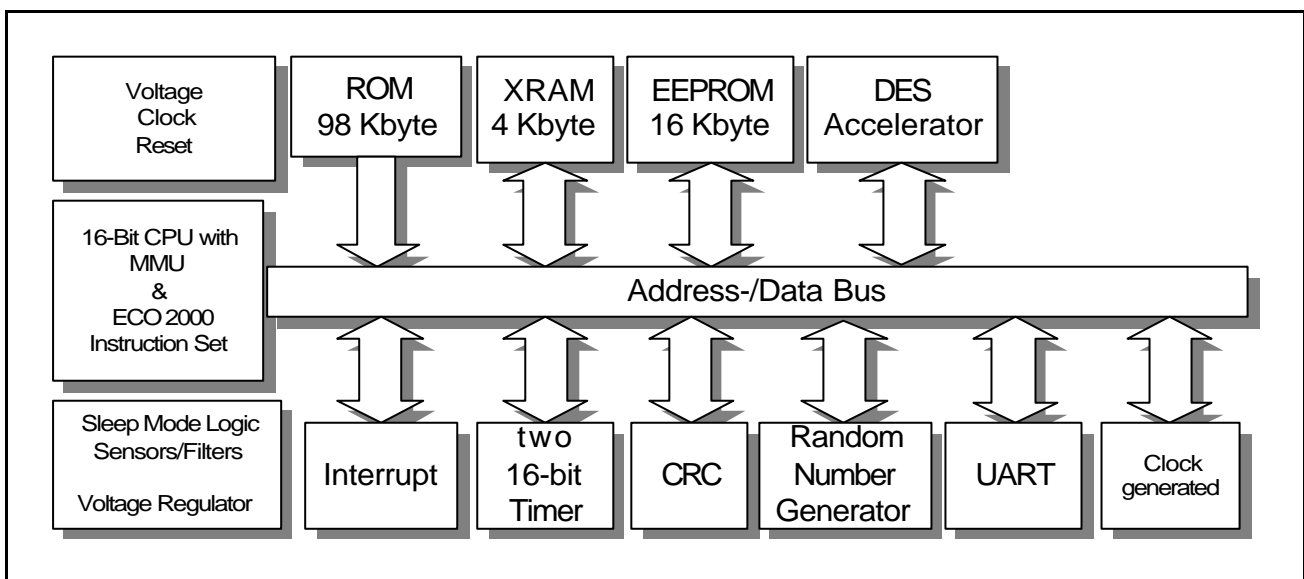


Figure 2: Block Diagram SLE 66C166P/PE

The new platform is designed to address up to 16Mbyte. However this feature is only available upon request and will clearly require a change in the existing tool environment.

In addition, new instructions have been implemented in the design for an efficient direct access of physical memory >64KByte up to 16 MByte.

**Security features:**

Since the very beginning, security is an integrated part of Infineons product development, as proved by various certificates (ITSEC, CC, Proton, VISA, ZKA, Mondex). The so called **“integral security concept”** for the 66P series ensures:

- A secret storage of any confidential code, data and keys
- Protection against side channel attacks such as: Simple Power Analysis (SPA) , Differential Power Analysis (DPA),
- Protection against Differential Fault Analysis (DFA), Electromagnetic Emanation Attack (EMA) and other possible HW or SW attacks

**Peripherals:** The CRC module allows the easy generation of checksums according to ISO/IEC 3309 (16-Bit-CRC). To minimize the overall power consumption, the chip card controller IC offers a sleep mode. The UART supports the half-duplex transmission protocols T=0 and T=1 according to ISO/IEC 7816-3. All relevant transmission parameters can be adjusted by software, as e.g. the clock division factor, direct/inverse convention and the number of stop bits. Additionally, the I/O port can be driven by communication routines realized in software.

The HW-DES module supports symmetric crypto algorithms according to the Data Encryption Standard in the Electronic Code Book Mode.

The random number generator (RNG) is able to supply the CPU with true random numbers on all conditions.

The advanced sensor concept includes various sensors for any kind of attacks scenarios and even more important a “Life Test ” for sensors.

As an important feature, the chip provides an on-chip security, which fulfills the strong security requirements of a Common Criteria evaluation at an EAL5+ level.

In conclusion, the SLE 66C166P/PE fulfills all the requirements of today's chip card applications, such as payment, GSM, Pay TV, security access, identification and digital signatures. In addition it offers a powerful platform for multi application cards based on Multos, Java or WinSC and supports the migration to enhanced GSM (incl. WAP), GPRS and UMTS value added services.

The SLE66C166P/PE integrates outstanding memory sizes, additional peripherals in combination with enhanced performance and optimized power consumption on a minimized die size.