FAIRCHILD
A Schlumberger Company

F100124
Hex TTL-to-ECL Translator

F100K ECL Product

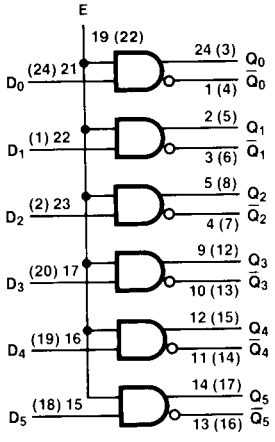
Description

The F100124 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable input (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated. All inputs have 50K Ω pull-down resistors.

When the circuit is used in the differential mode, the F100124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

Pin Names	Description	TTL Unit Load (U.L.) HIGH/LOW
D_0–D_5	Data Inputs	0.5/1.0
E	Enable Input	3.0/6.0
Q_0–Q_5	Data Outputs	—
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs	—

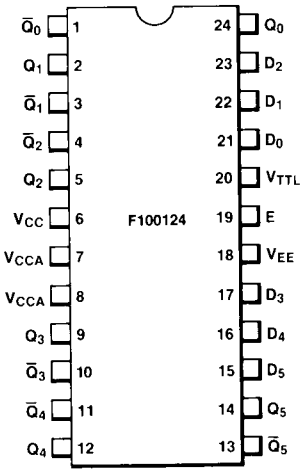
Logic Symbol



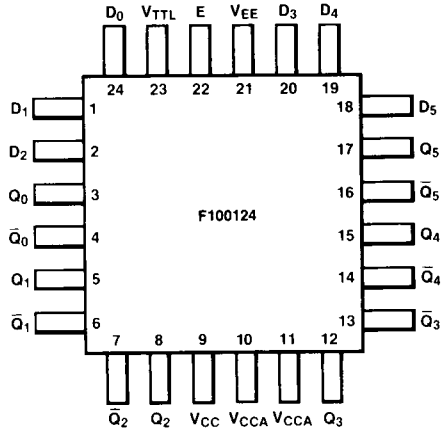
V_{CC} = Pin 6 (9)
V_{CCA} = Pins 7 (10), 8 (11)
V_{EE} = Pin 18 (21)
V_{TTL} = Pin 20 (23)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Absolute Maximum Ratings* Above which the useful life may be impaired

V_{TTL} Pin Potential to Ground Pin	+6.0 V to −0.5 V
Input Voltage (dc)	−0.5 V to V_{TTL}

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs
V_{CD}	Input Clamp Diode Voltage	−1.5			V	I_{IN} = −10 mA
I_{IH}	Input HIGH Current Data Enable			20 120	μA	V_{IN} = +2.4 V, All Other Inputs V_{IN} = GND
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	V_{IN} = +5.5 V, All Other Inputs = GND
I_{IL}	Input LOW Current Data Enable	 −1.6 −9.6			mA	V_{IN} = +0.4 V, All Other Inputs V_{IN} = GND
I_{EE}	V_{EE} Power Supply Current	−140	−96	−52	mA	All Inputs V_{IN} = +4.0 V
I_{TTL}	V_{TTL} Power Supply Current		44	75	mA	All Inputs V_{IN} = GND

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V

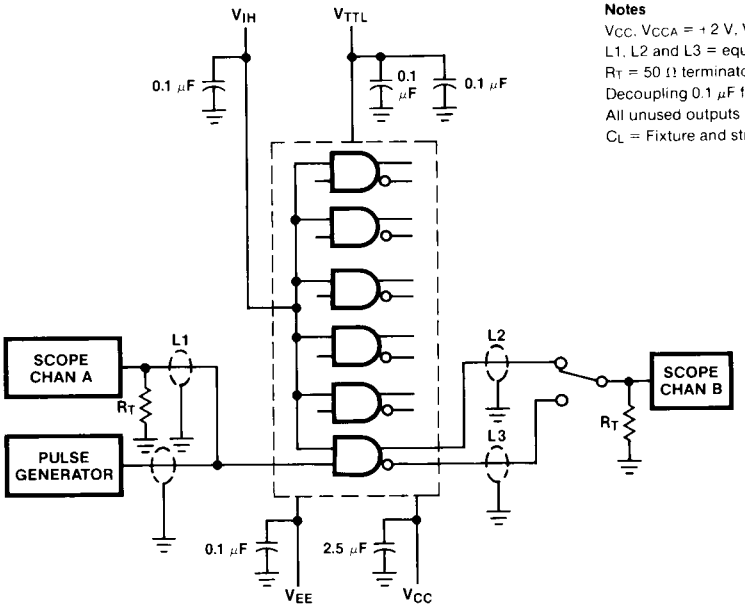
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

*See Family Characteristics for other absolute maximum ratings and dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V, V_{TTL} = +7.0 V, V_{IH} = +6.0 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times