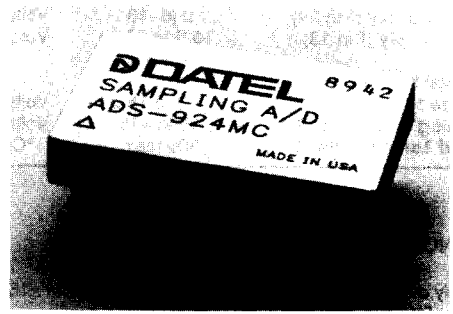
ADS-924

14-Bit, 300 KHz, Low-Power Sampling A/D Converter

FEATURES

- **14-Bit resolution**
- **Internal Sample/Hold**
- **300 KHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 1.4 Watts**
- **Three-state output buffers**

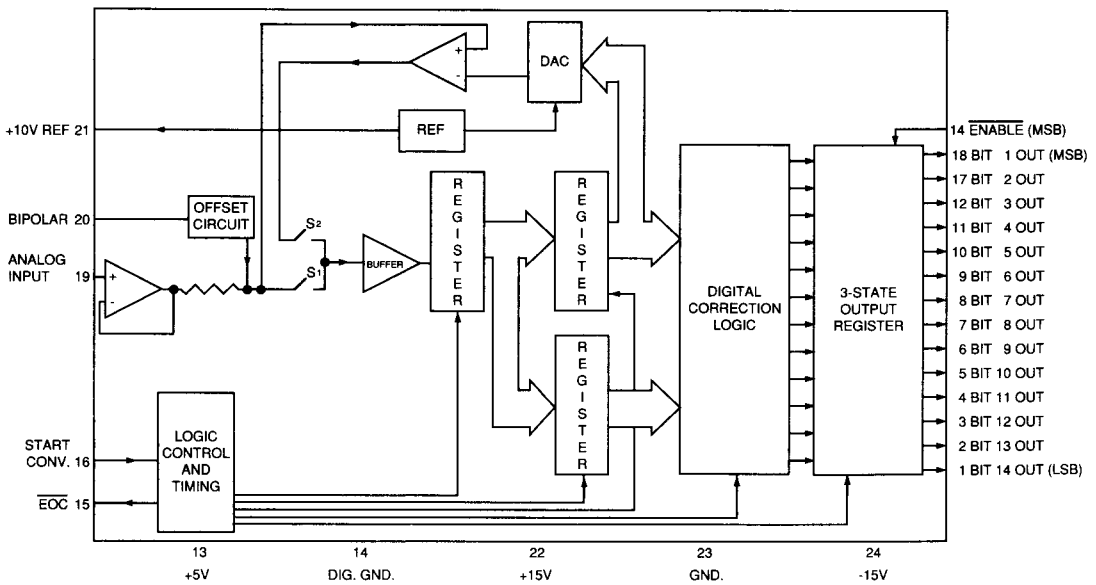


GENERAL DESCRIPTION

DATEL's ADS-924 is a 14-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 300 KHz is achieved while only dissipating 1.4 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 OUT (LSB)	13	+5V
2	BIT 13 OUT	14	$\overline{\text{ENABLE}}$
3	BIT 12 OUT	15	$\overline{\text{EOC}}$
4	BIT 11 OUT	16	START CONVERT
5	BIT 10 OUT	17	BIT 2 OUT
6	BIT 9 OUT	18	BIT 1 (MSB)
7	BIT 8 OUT	19	ANALOG INPUT
8	BIT 7 OUT	20	BIPOLAR
9	BIT 6 OUT	21	+10V REF
10	BIT 5 OUT	22	+15V
11	BIT 4 OUT	23	GROUND
12	BIT 3 OUT	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14, 16)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-924	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	5.0	15.0	–	M Ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Integral Non-Linearity				
+25 °C (see Tech Notes)	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±3	LSB
Differential Non-Linearity				
+25 °C	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±2.5	LSB
Full Scale Absolute Accuracy				
+25 °C	–	±0.037	±0.074	%FSR
0 °C to +70 °C	–	±0.074	±0.13	%FSR
-55 °C to +125 °C	–	±0.12	±0.2	%FSR
Unipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR
Bipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR
Bipolar Offset Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR
Gain Error, +25 °C (See Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR

OUTPUTS	MIN.	TYP.	MAX.	UNITS
No Missing Codes				
(14 Bits)	at +25 °C			
(13 Bits)	over 0 to 70 °C temp. range			
(12 Bits)	over -55 to +125 °C temp. range			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	14 Bits			
Output Coding	Straight binary/offset binary			
DYNAMIC PERFORMANCE				
Conversion Time				
+25 °C	300	–	–	KHz
0 °C to +70 °C	300	–	–	KHz
-55 °C to +125 °C	300	–	–	KHz
Total Harmonic Distortion				
DC to 100 KHz at Vin<2.5V p-p				
+25 °C	-72	-76	–	dB
-55 °C to +125 °C	-70	-72	–	dB
DC to 40 KHz at Vin = 10V p-p				
+25 °C	-72	-76	–	dB
-55 °C to +125 °C	-70	-72	–	dB
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty	–	±100	–	pSec.
S/H Acquisition Time to 0.006% (10V step)				
+25 °C	–	–	1.2	µSec.
0 °C to +70 °C	–	–	1.35	µSec.
-55 °C to +125 °C	–	–	1.5	µSec.
(Sinusoidal Input)	–	–	700	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.5	+5.0	+5.5	Volts dc
Power Supply Current				
+15V dc Supply	–	+41	+49	mA
-15V dc Supply	–	-46	-53	mA
+5V dc Supply*	–	+66	+75	mA
Power Dissipation	–	1.4	1.8	Watts
Power Supply Rejection	–	–	0.01	%FSR/%
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

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TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-924 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.
2. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).
3. The ADS-924 exhibits up to 2.0 LSB's of peak-to-peak noise. Digital signal processing (DSP) applications will average this noise.
4. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 14) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 14) to a logic "1" (high).

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

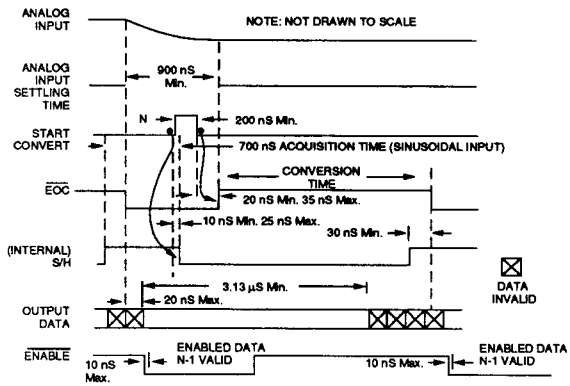


Figure 2. ADS-924 Timing Diagram

Table 2. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to Pin 21
0 to +10V dc	Pin 19	Pin 20 to Ground

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+300µV dc	+9.9991V dc
±5V dc	+300µV dc	+4.9991V dc

Table 4. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	1.65	4.99	K Ohms
0 to +2.5V, ±1.25V	715	4990	K Ohms

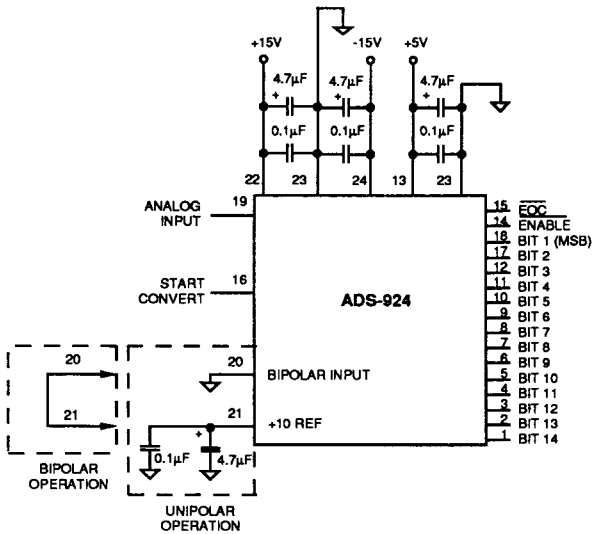


Figure 3. Typical Input Connections for the ADS-924

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 5.

Table 6. Output Coding

		STRAIGHT BIN. COMP. BINARY				
INPUT RANGE	**UNIPOLAR**	**OUTPUT CODING**				**BIPOLAR**	**INPUT**
0 to +10V	**SCALE**	**MSB**	**LSB**	**MSB**	**LSB**	**SCALE**	**RANGES**
+9.99939V	+FS -1 LSB	1111	1111 1111	0000	0000 0000	+FS -1 LSB	+4.99939V
+8.7500V	7/8 FS	1110	0000 0000	0001	1111 1111	+3/4 FS	+3.7500V
+7.5000V	3/4 FS	1100	0000 0000	0011	1111 1111	+1/2 FS	+2.5000V
+5.0000V	1/2 FS	1000	0000 0000	0111	1111 1111	0	0.0000V
+2.5000V	1/4 FS	0100	0000 0000	1011	1111 1111	-1/2 FS	-2.5000V
+1.2500V	1/8 FS	0010	0000 0000	1101	1111 1111	-3/4 FS	-3.7500V
+0.0003V	1 LSB	0000	0000 0001	1111	1111 1110	-FS + 1 LSB	-4.99939V
0.0000V	0	0000	0000 0000	1111	1111 1111	-FS	-5.0000V
		OFF. BINARY		COMP. OFF. BIN.			

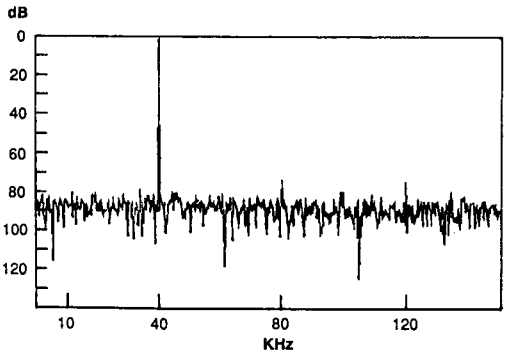
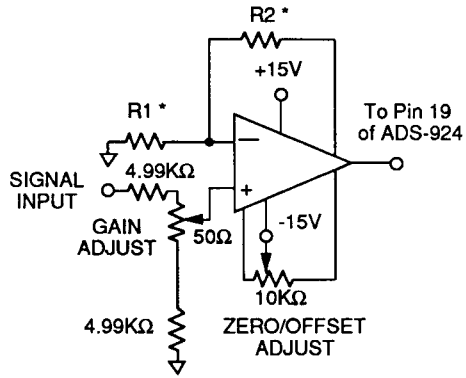


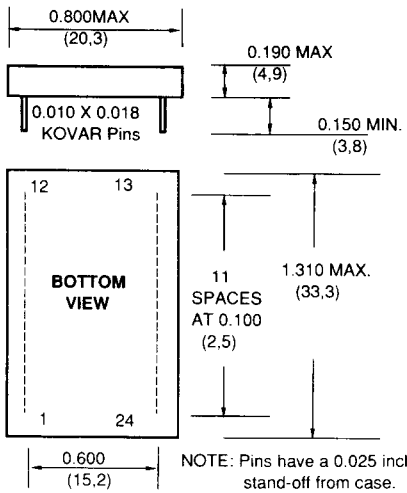
Figure 5. FFT Analysis of ADS-924



* See Table 4 for R1 and R2 values.

Figure 4. Optional Calibration Circuit

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-924MC	0 °C to +70 °C	Hermetic
ADS-924MM	-55 °C to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883B versions, contact DATEL.

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