KS54HCTLS/KS74HCTLS 679/680

T-45-17

12-Bit Address Comparators

Preliminary Specifications

FEATURES

- '679: 12-bit to 4-bit comparator with enable
- '680: 12-bit to 4-bit comparator with latch
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

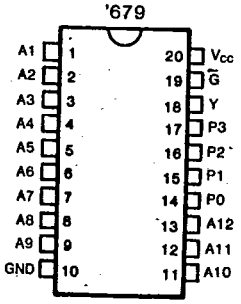
The '679 and '680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

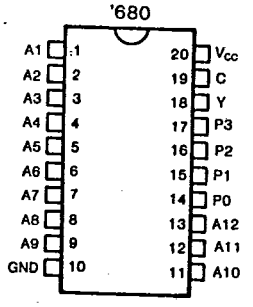
The '679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The '680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS





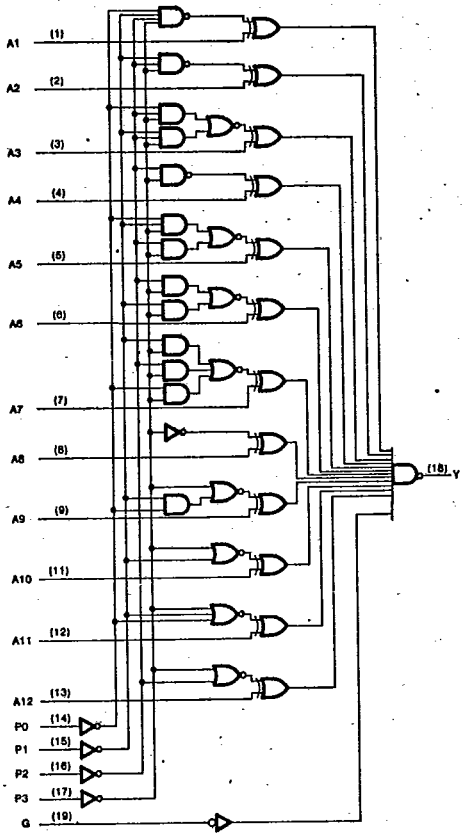
KS54HCTLS / KS74HCTLS 679/680

12-Bit Address Comparators

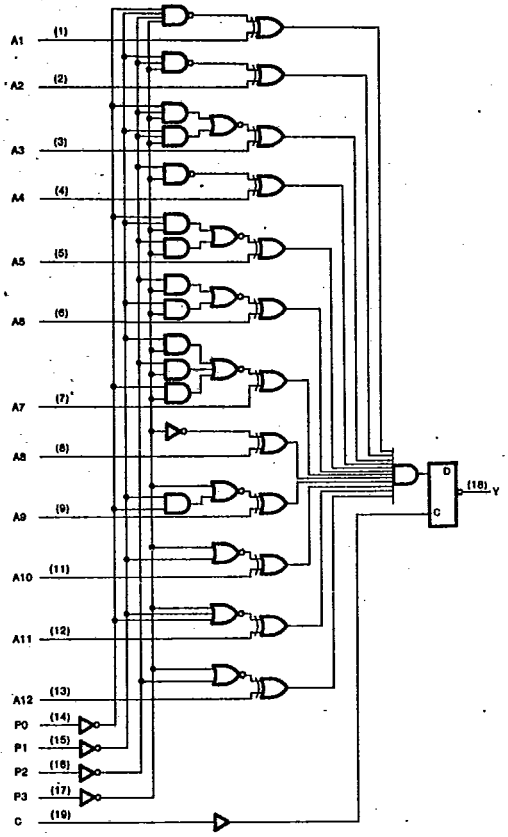
T-45-17

LOGIC DIAGRAMS

'679



'680



5

KS54HCTLS/KS74HCTLS 679/680

12-Bit Address Comparators

FUNCTION TABLE

'679	'680	INPUTS COMMON TO '679 AND '680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'679: Any combination																H
	L	'680: Any combination																Latched

* These three rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for all combinations in which P=12, 13 and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P≥9 to P=9 ... 11/13 ... 15, P≥10 to P=10/11/14/15, and P≥11 to P=11/15.

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) ..... ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) .... ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) ..... ±70 mA
Continuous Current Through
V_{CC} or GND pins ..... ±250 mA
Storage Temperature Range, T_{stg} ... −65°C to +150°C
Power Dissipation Per Package, P_d† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} .. 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

KS54HCTLS KS74HCTLS 679/680

12-Bit Address Comparators

T-45-17

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA I_O=−6mA	V_{CC} 4.2	V_{CC} −0.1 3.98	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA I_O=12mA I_O=24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS679

Characteristic	Symbol	Conditions†	T_a=25°C V_{CC}=5.0V		KS74HCTLS T_a=−40°C to +85°C V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C V_{CC}=5.0V± 10%	Unit
			Typ		Guaranteed Limits		
Maximum Propagation Delay, Any P to Y	t_{PLH}	C_L=50pF	24	32	40	48	ns
		C_L=150pF	27	35	45	54	
	t_{PHL}	C_L=50pF	27	32	40	48	
		C_L=150pF	30	35	45	54	
Maximum Propagation Delay, Any A to Y	t_{PLH}	C_L=50pF	21	28	35	42	ns
		C_L=150pF	24	31	40	48	
	t_{PHL}	C_L=50pF	21	28	35	42	
		C_L=150pF	24	31	40	48	
Maximum Propagation Delay, G to Y	t_{PLH}	C_L=50pF	18	24	30	36	ns
		C_L=150pF	21	27	35	42	
	t_{PHL}	C_L=50pF	18	24	30	36	
		C_L=150pF	21	27	35	42	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D \doteq C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

KS54HCTLS KS74HCTLS 679/680

12-Bit Address Comparators

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS680

Characteristic	Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay, Any P to Y	t_{PLH}	$C_L = 50pF$	27	36	45	54	ns
		$C_L = 150pF$	30	39	50	60	
	t_{PHL}	$C_L = 50pF$	27	32	40	48	
		$C_L = 150pF$	30	35	45	64	
Maximum Propagation Delay, Any A to Y	t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		$C_L = 150pF$	27	35	45	64	
	t_{PHL}	$C_L = 50pF$	24	32	40	48	
		$C_L = 150pF$	27	35	45	64	
Maximum Propagation Delay, C to Y	t_{PLH}	$C_L = 50pF$	19	26	32	38	ns
		$C_L = 150pF$	22	29	37	44	
	t_{PHL}	$C_L = 50pF$	19	26	32	38	
		$C_L = 150pF$	22	29	37	44	
Maximum Input Capacitance	C_{IN}		5				pF
Power Dissipation Capacitance*	C_{PD}						pF

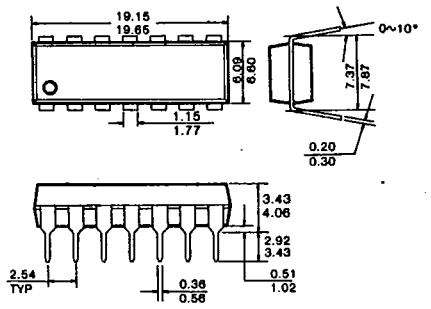
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

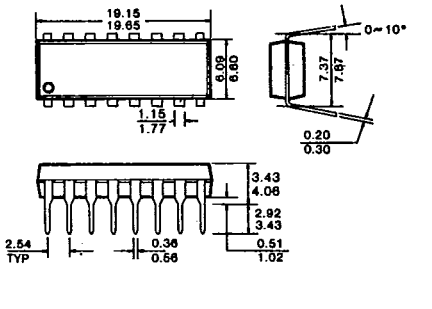
T-90-20

1. PLASTIC PACKAGES

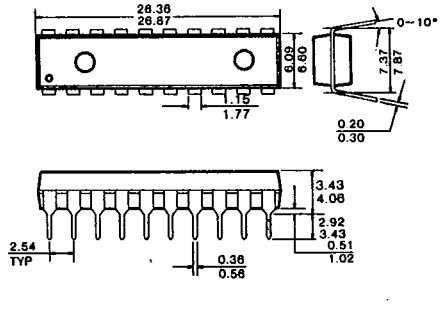
14-Pin Plastic DIP **Units: mm**



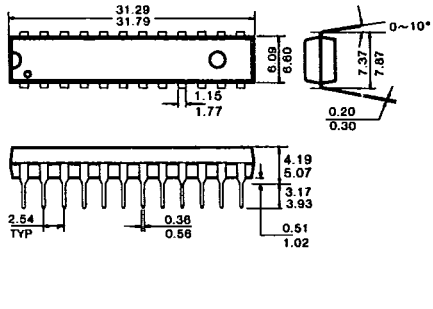
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



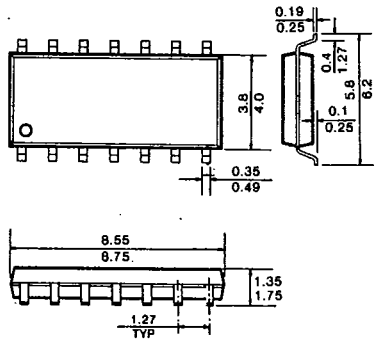
7

PACKAGE DIMENSIONS

T-90-20

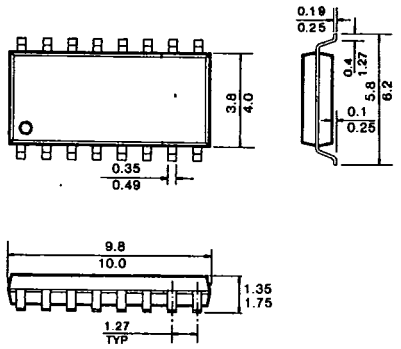
14-Pin SOP

Unit: mm



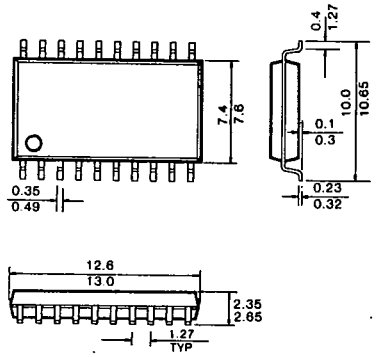
16-Pin SOP

Unit: mm



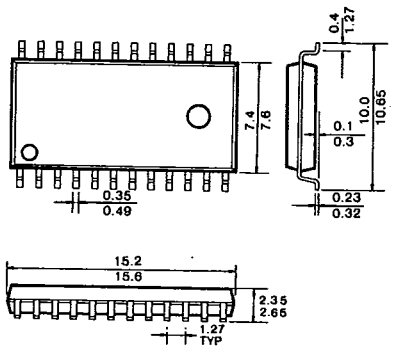
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

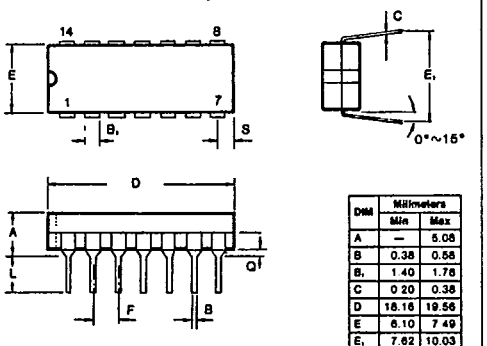


PACKAGE DIMENSIONS

T-90-20

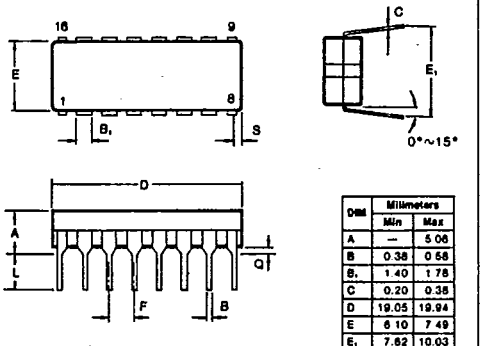
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



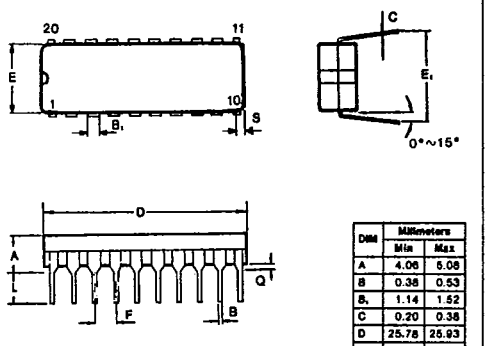
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



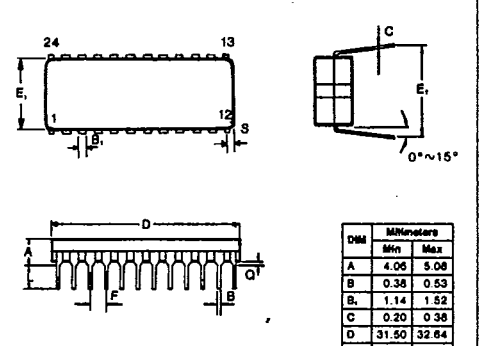
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

7