Signetics

74AC/ACT11579

8-Bit Binary Up/Down Counter w/ Common I/O Pins; Synchronous and Asynchronous Reset; 3-State

Objective Specification

ACL Products

FEATURES

- **Multiplexed 3-State I/O ports for bus-oriented applications**
- **Built-in cascading carry capability**
- **Glitchless Terminal Count output**
- **Fully synchronous operation**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master Reset and Synchronous Reset**
- **Output capability: ±24mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11579 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The AC/ACT11579 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applica-

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to I/O_n	C_L = 50pF		6.2	7.8	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	230	210	pF
			Disabled	40	40	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_O	Output capacitance	V_{IO} = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	V_{IO} = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP to I/O_n	C_L = 50pF		160	150	MHz

Note:

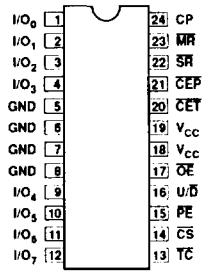
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

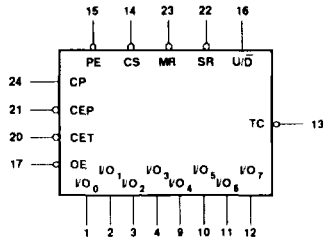
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11579N 74ACT11579N
24-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11579D 74ACT11579D

PIN CONFIGURATION

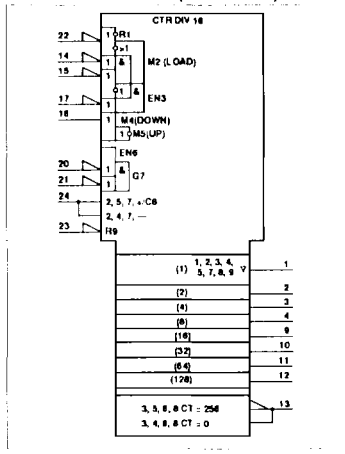
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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tions. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock.

The AC/ACT11579 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other. This mode of operation eliminates the output spikes normally associated with ripple counters. A buffered clock input triggers all flip-flops on the Low-to-High transition. Flip-flop contents appear on the I/O lines only when $\overline{OE}$ and $\overline{CS}$ are Low and $\overline{PE}$ is High.

Both synchronous and asynchronous master resets are provided. All flip-flops are reset whenever $\overline{MR}$ is Low. If $\overline{MR}$ is High and $\overline{SR}$ is Low, all flip-flops are reset on the next Low-to-High transition of the clock.

The counter is fully programmable; that is, the flip-flops may be preset to either level. Presetting is synchronous with the clock and takes precedence over other functions when $\overline{MR}$ and $\overline{SR}$ are High. Both $\overline{PE}$ and $\overline{CS}$ must be Low to preset the counter.

The direction of counting is controlled by the U/$\overline{D}$ input; a High will cause the count to increase, a low will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional components. Instrumental in accomplishing this are tow Count Enable inputs ($\overline{CET}$ and $\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both count enable inputs must be low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High or Low level portion of the Q_0 output depending on the state of U/$\overline{D}$. This will occur when the counter is at zero when counting down or 15 when counting up.

The Terminal Count ($\overline{TC}$) output is normally High and goes Low when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode, provided that $\overline{CET}$ is Low. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ signal is derived by decoding the D-input signals of the counter flip-flops and using this decoded signal as the D-input driving the $\overline{TC}$ output. Use of this configuration gives a $\overline{TC}$ output which is free of decoding spikes. The possibility exists that on pwer-up that the $\overline{TC}$ output may not give a true indication of the state of the counter (i.e., $\overline{TC}$ may be Low while the counter is not at terminal count or High when it is at terminal count.) Should this occur, $\overline{TC}$ will always go to a correct state on the first Low-to-High transition of the clock.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{PE}$	Parallel enable input
16	U/$\overline{D}$	Up-Down count control input
23	$\overline{MR}$	Master reset input (active-Low)
22	$\overline{SR}$	Synchronous reset input (active-Low)
21	$\overline{CEP}$	Count enable parallel input (active-Low)
20	$\overline{CET}$	Count enable trickle input (active-Low)
14	$\overline{CS}$	Chip select input (active-Low)
17	$\overline{OE}$	Output enable input (active-Low)
24	CP	Clock input
13	$\overline{TC}$	Terminal count output (active-Low)
1, 2, 3, 4, 9, 10, 11, 12	I/O_0 -I/O_7	Data inputs/outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	FUNCTION
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in Hi Z (PE disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in Hi Z
X	X	L	H	X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage levle
L = Low voltage levels
X = Don't Care
U = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never both be at the Low voltage level at the same time

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11579			74ACT11579			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±225	mA
	DC ground current		±225	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11579				74ACT11579				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		±5.0		±0.5		±5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.