Document No.	
ECN No.	
Date of Issue	June 18, 1990
Status	Preliminary Specification
ECL Products	

100255

Quint ECL–TTL Translating Transceiver

FEATURES

- **Typical propagation delay from ECL input to TTL output: 3.2ns**
- **Typical propagation delay from TTL input to ECL output: 1.6ns**
- **Typical ECL supply current ($-I_{EE}$): 105mA**
- **Typical TTL supply current (I_{TTL}): 76mA**
- **ECL output has three–state capability**
- **ECL output drives 25 Ohm loads**

DESCRIPTION

The 100255 is a five–bit, inverting, translating transceiver. It allows the exchange of data between a 100K ECL bus and a TTL bus. The A data lines are bidirectional with 100K ECL compatibility and three–state capability. The B data lines are bidirectional with TTL compatibility and three–state capability. The control lines require 100K ECL input levels.

The Direction Control, DIR, selects the data flow path (A_n to B_n or B_n to A_n). A Low on the Chip Enable, CE, puts both the A_n and the B_n lines into a high impedance state. Each A_n output can drive a load as low as 25 Ohms (i.e. a 50 Ohm bus terminated at each end with 50 Ohms to –2.0V).

The GND_1 line is associated with all the TTL circuitry, the ECL internal logic, and the ECL reference generator. GND_2 services the ECL outputs.

Power may be applied to the V_{EE} and V_{TTL} pins in any order.

All unused inputs can be left open due to integrated pull–down resistors.

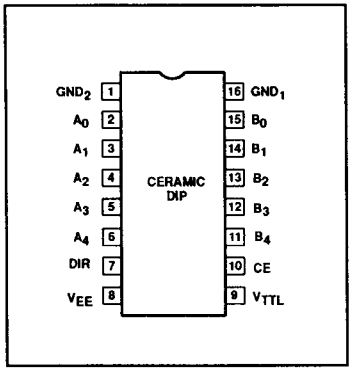
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Ceramic DIP (300 mils wide)	100255F

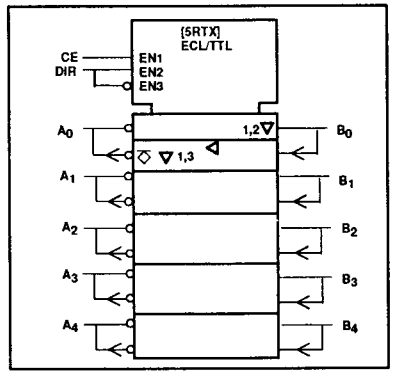
PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_4$	Bidirectional data lines (100K ECL compatible)
$B_0 - B_4$	Bidirectional data lines (TTL compatible)
DIR	Direction control input (100K ECL compatible)
CE	Chip enable input (100K ECL compatible)

PIN CONFIGURATION



IEC/IEEE SYMBOL



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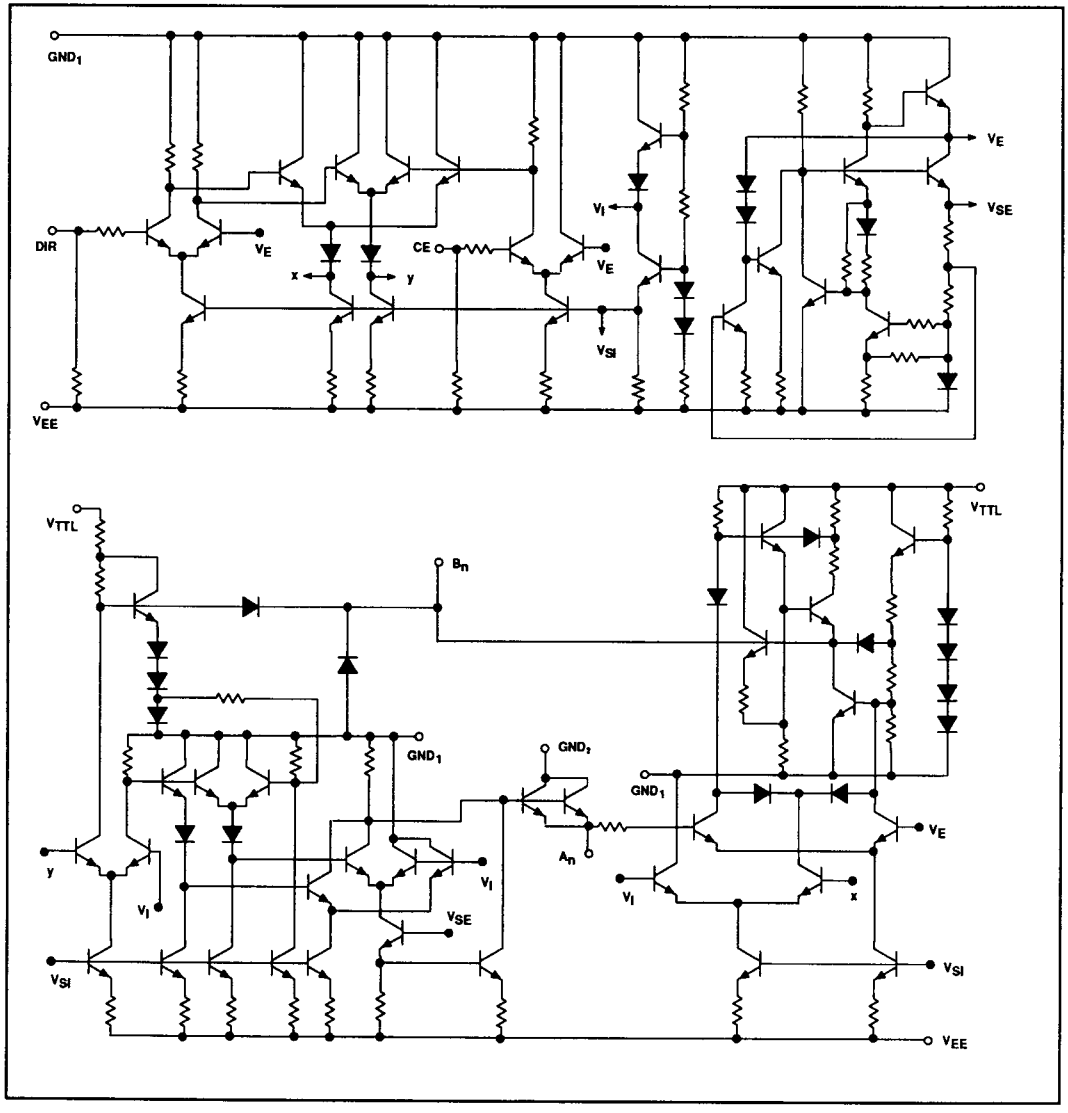
SIMPLIFIED SCHEMATIC



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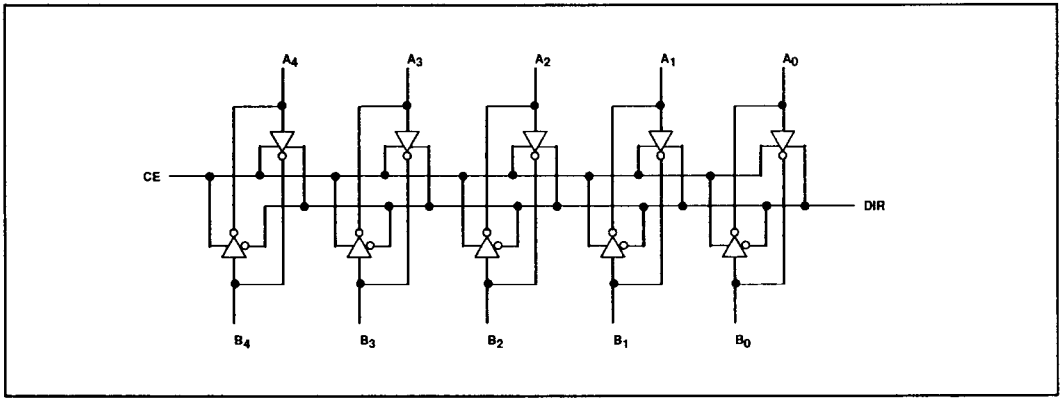
LOGIC DIAGRAM



NOTE:
Pins B_0 through B_4 are compatible with TTL. Pins CE, DIR, and A_0 through A_4 are compatible with 100K ECL.

FUNCTION TABLE

CONTROL		DATA		OPERATING MODE
CE	DIR	A_n	B_n	
L	X	Z	Z	A_n and B_n in high impedance state
H H	H H	L H	H L	Data flows from A_n to B_n (ECL–to–TTL translation)
H H	L L	L H	H L	Data flows from B_n to A_n (TTL–to–ECL translation)

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance state

ABSOLUTE MAXIMUM RATINGS FOR ECL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, T_A =0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	ECL supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–100	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

ABSOLUTE MAXIMUM RATINGS FOR TTL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{TTL}	TTL supply voltage range	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to V_{TTL}	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to B_n in High state	–0.5 to V_{TTL}	V
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS FOR ECL–COMPATIBLE LINES

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
GND_1, GND_2	Circuit ground		0	0	0	V
V_{EE}	ECL supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	ECL supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC OPERATING CONDITIONS FOR TTL–COMPATIBLE LINES

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS NOM.	LIMITS MAX.	UNIT
V_{TTL}	TTL supply voltage	+4.5	+5.0	+5.5	V
V_{IH}	High level input voltage	+2.0			V
V_{IL}	Low level input voltage			+0.8	V
$-I_{OH}$	High level output current			2	mA
I_{OL}	Low level output current			20	mA
T_A	Operating ambient temperature range	0	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS FOR ECL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, V_{EE} = –4.8V to –4.2V, V_{TTL} = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		DIR at V_{ILMIN}. CE at V_{IHMAX}. A_n loaded with 25Ω to –2.0V ± 0.010V.	B_n at 0.4V.	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			B_n at 0.8V.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			B_n at 2.0V.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			B_n at 2.4V.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current[5]	DIR, CE	One control input under test at V_{IHMAX}, other control input at V_{ILMIN}. A_n and B_n are open.					350	µA
		A_n	One A_n under test at V_{IHMAX}, all other A_n at V_{ILMIN}. CE and DIR at V_{IHMAX}.					350	µA
I_{IL}	Low level input current for DIR and CE		One control input under test at V_{ILMIN}, other control input at V_{IHMAX}. A_n and B_n are open.			+0.5			µA
I_{OZ}	Off–state output current[6]		One A_n under test at –2.1V, all other A_n open. B_n, CE and DIR at V_{ILMIN}.			–50		50	µA
$-I_{EE}$	ECL supply current		CE at V_{IHMAX}.			60	105	150	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for extended V_{EE} range. For more information, see Chapter 10, sexction 4.
5. For bidirectional lines, this parameter includes output leakage current.
6. This parameter includes input reverse leakage current.

DC ELECTRICAL CHARACTERISTICS FOR TTL–COMPATIBLE LINES

$GND_1 = GND_2$ = ground, V_{EE} = –4.8V to –4.2V, V_{TTL} = 4.5V to 5.5V, T_A = 0°C to +85°C unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS			UNIT
			MIN.	TYP.	MAX.	
V_{OH}	High level output voltage	A_n at V_{ILMAX}, DIR and CE at V_{IHMAX}, I_{OH} = –2.0mA.	2.4			V
V_{OL}	Low level output voltage	A_n at V_{IHMIN}, DIR and CE at V_{IHMAX}, I_{OL} = +20mA.		0.35	0.50	V
V_{IK}	Input clamp voltage	Apply –18mA to B_n under test with other B_n open. CE at V_{ILMIN}.	–1.2	–0.73		V
I_I	Input current at maximum input voltage[4]	B_n under test at +5.5V, other B_n at ground. CE at V_{ILMIN}. V_{TTL} at +5.5V.			1.0	mV
I_{IH}	High level input current[4]	B_n under test at +2.4V, other B_n at ground. CE at V_{IHMAX}. DIR at V_{ILMIN}.			40	µA
$-I_{IL}$	Low level input current[4]	B_n under test at +0.4V, other B_n at +2.4V. CE at V_{IHMAX}. DIR at V_{ILMIN}.			1.6	mA
I_{OZH}	Off–state output current, High level voltage applied[5]	B_n at +2.4V. A_n at V_{ILMAX}. CE at V_{ILMIN}. DIR at V_{IHMAX}.			40	µA
$-I_{OZL}$	Off–state output current, Low level voltage applied[5]	B_n at +0.4V. A_n at V_{IHMIN}. CE at V_{ILMIN}. DIR at V_{IHMAX}.			40	µA
$-I_{OS}$	Short circuit output current[6]	A_n at V_{ILMIN}. One B_n under test at ground. V_{TTL} at +5.5V. DIR and CE at V_{IHMAX}.	40		130	mA
I_{TTLH}	TTL supply current with outputs High	All A_n at V_{ILMIN}. V_{TTL} at +5.5V. All B_n open. DIR and CE at V_{IHMAX}.	25	35	44	mA
I_{TTLL}	TTL supply current with outputs Low	All A_n at V_{IHMAX}. V_{TTL} at +5.5V. All B_n open. CE and DIR at V_{IHMAX}.	19	35	44	mA
I_{TTLZ}	TTL supply current with outputs in the high impedance state	V_{TTL} at +5.5V. All B_n open. CE at V_{ILMIN}.	25	44	48	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply volage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. This parameter includes output leakage current.
5. This parameter includes input reverse leakage current.
6. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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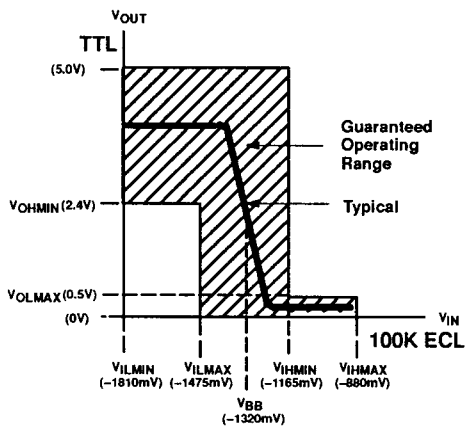
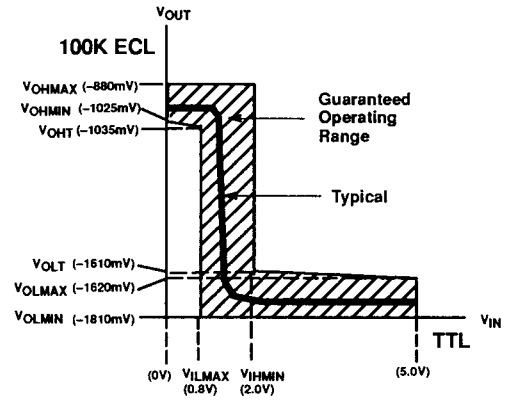
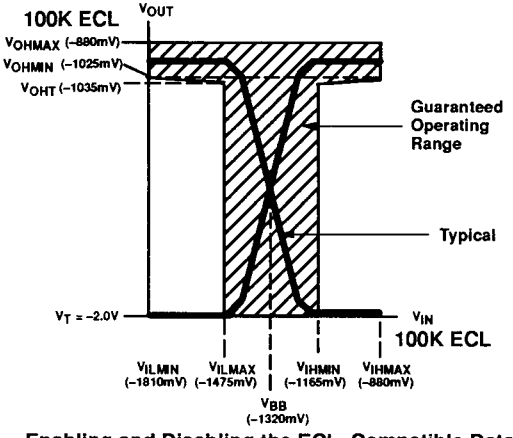
TRANSFER CHARACTERISTICS



ECL–to–TTL Translation[1]



TTL–to–ECL Translation[2]



Enabling and Disabling the ECL–Compatible Data Lines[3]

NOTES:
1. V_{IN} is applied to A_n and V_{OUT} is measured at B_n.
2. V_{IN} is applied to B_n and V_{OUT} is measured at A_n.
3. V_{IN} is applied to DIR or CE and V_{OUT} is measured at A_n.

AC ELECTRICAL CHARACTERISTICS FOR TTL–TO–ECL DATA FLOW

Ceramic DIP $GND_1 = GND_2$ = ground, V_{EE} = –5.7V to –4.2V, V_{TTL} = 4.5V to 5.5V.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	1.00 1.00	4.00 4.00	1.00 1.00	4.00 4.00	1.00 1.00	4.00 4.00	ns ns
t_{PZH}	Output enable time CE, DIR to A_n	Waveform 2	4.00	8.00	4.00	8.00	4.00	8.00	ns ns
t_{PHZ}	Output disable time CE, DIR to A_n	Waveform 2	1.50	4.00	1.50	4.00	1.50	4.00	ns ns
t_{TLH} t_{THL}	Transition time for A_n	Waveform 1	1.00 1.00	2.50 2.50	1.00 1.00	2.50 2.50	1.00 1.00	2.50 2.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

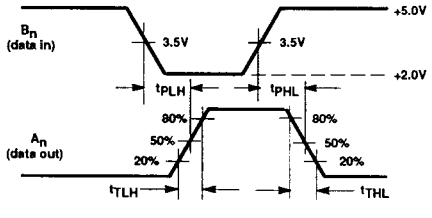
AC ELECTRICAL CHARACTERISTICS FOR ECL–TO–TTL DATA FLOW

Ceramic DIP $GND_1 = GND_2$ = ground, V_{EE} = –5.7V to –4.2V, V_{TTL} = 4.5V to 5.5V.

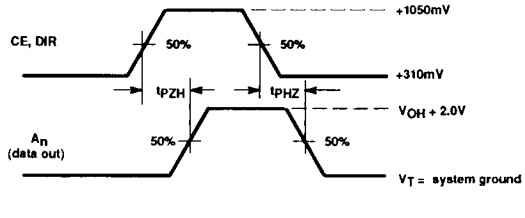
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 3		4.50 4.50		4.50 4.50		4.50 4.50	ns ns
t_{PZH} t_{PZL}	Output enable time CE, DIR to B_n	Waveform 4		7.00 7.00		7.00 7.00		7.00 7.00	ns ns
t_{PHZ} t_{PLZ}	Output disable time CE, DIR to B_n	Waveform 4		3.00 3.00		3.00 3.00		3.00 3.00	ns ns
t_{TLH} t_{THL}	Transition time for B_n	Waveform 3	1.00 1.00	3.50 3.50	1.00 1.00	3.50 3.50	1.00 1.00	3.50 3.50	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS FOR TTL–TO–ECL DATA FLOW



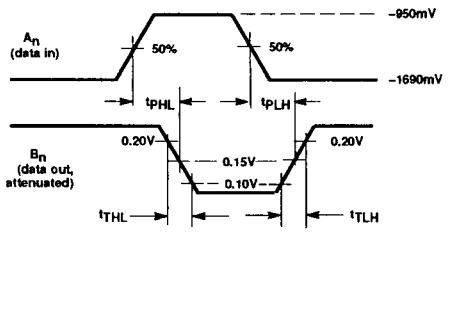
Waveform 1. Propagation Delays and Transition Times



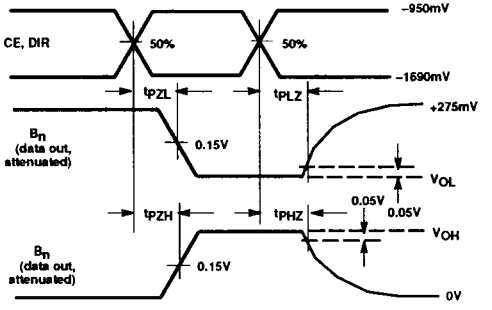
Waveform 2. Output Enable and Disable Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

AC WAVEFORMS FOR ECL–TO–TTL DATA FLOW

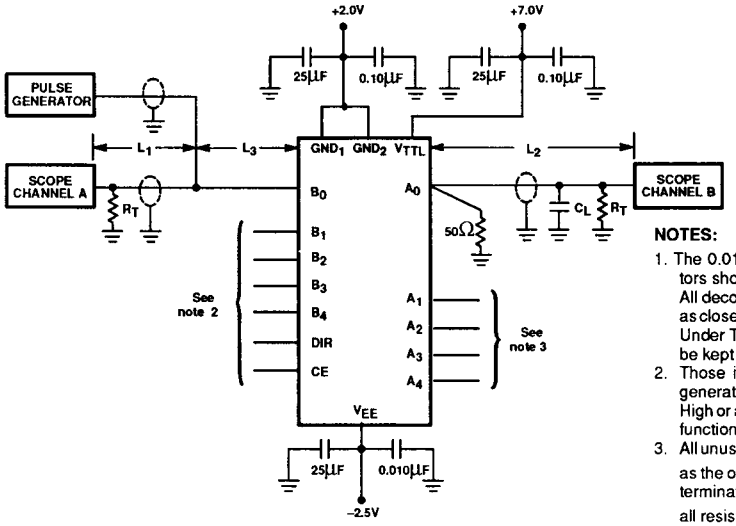


Waveform 3. Propagation Delays and Transition Times



Waveform 4. Output Enable and Disable Times

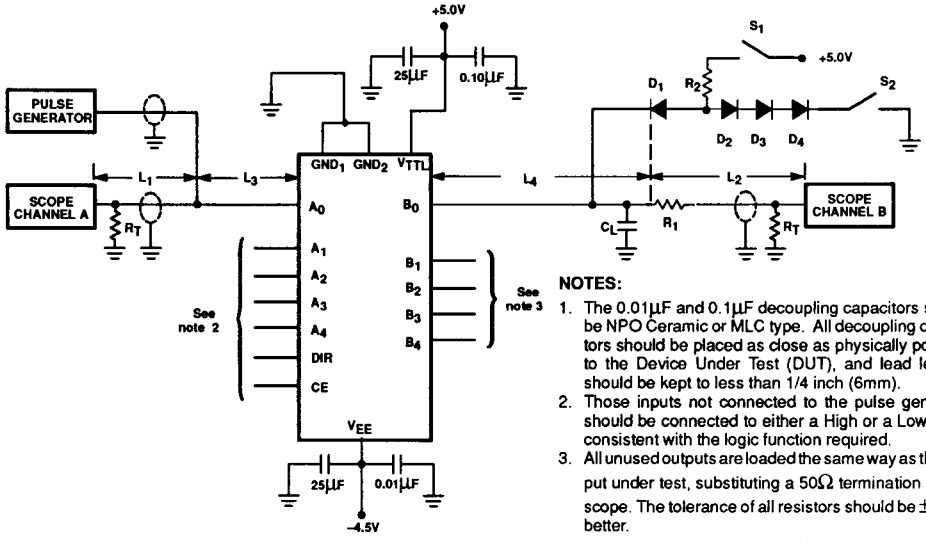
AC TEST CIRCUIT FOR TTL–TO–ECL DATA FLOW



NOTES:

1. The 0.01µF and 0.1µF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm).
5. R_T = 50Ω termination internal to scope.
6. Fixture and stray capacitance (not including scope cable capacitance) = $C_L \leq 3pF$.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. All power and signal voltages shifted up 2.0V for AC bench test purposes.

AC TEST CIRCUIT FOR ECL–TO–TTL DATA FLOW



SWITCH POSITION

TEST	SWITCH S_1	SWITCH S_2
t_{PLH}, t_{PHL}	closed	closed
t_{PLZ}, t_{PZL}	closed	open
t_{PHZ}, t_{PZH}	open	open

NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ±1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 =450Ω. R_2 =280Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 25pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).
8. When the output under test is in the high impedance state, the voltage at scope channel B will be at ground potential with S_1 and S_2 open and at 0.275V with S_1 closed and S_2 open.
9. D_1 through D_4 are high frequency (low capacitance) switching diodes.

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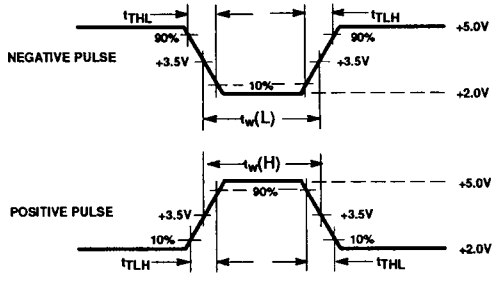
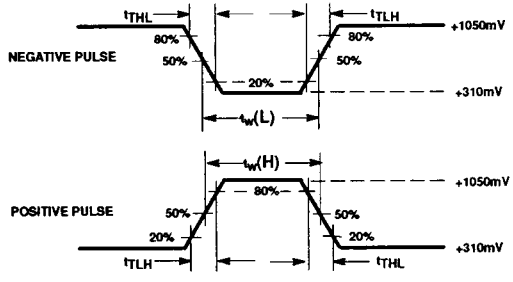
INPUT PULSE DEFINITION FOR TTL–TO–ECL DATA FLOW



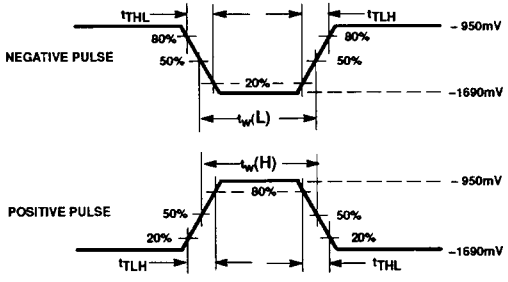


INPUT PULSE REQUIREMENTS for B_n $GND_1 = GND_2 = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_{TTL} = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
TTL	$3.0V_{p-p}$	1MHz	500ns	2.5 ± 0.2ns

INPUT PULSE REQUIREMENTS for CE and DIR $GND_1 = GND_2 = +2.0V \pm 0.010V$, $V_{EE} = -2.8V$ to $-2.2V$, $V_{TTL} = +6.5V$ to $+7.5V$, $V_T = 0V$ (system ground)				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	$740mV_{p-p}$	1MHz	500ns	0.7 ± 0.1ns

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.

INPUT PULSE DEFINITION FOR ECL–TO–TTL DATA FLOW



INPUT PULSE REQUIREMENTS for A_n, CE, and DIR $GND_1 = GND_2 = 0V$ (system ground), $V_{EE} = -4.8V$ to $-4.2V$, $V_{TTL} = +4.5V$ to $+5.5V$				
Family	**Amplitude**	**Rep Rate**	**$t_w(L)$, $t_w(H)$**	**t_{TLH}, t_{THL}**
100K ECL	$3.0V_{p-p}$	1MHz	500ns	0.7 ± 0.1ns