SN54LS384/SN74LS384

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

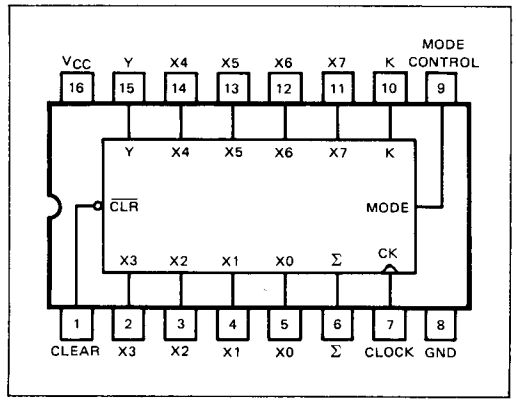
Advance Information

DESCRIPTION — The SN54LS/74LS384 is an 8 x 1 bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to obtain a two's-complement product. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled by the clear input. With the clear input low, all internal flip-flops are cleared and the X latches opened to accept new multiplicand data. When the clear input is high, the latches are closed.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the Σ output.

The multiplication of an m-bit number by an n-bit number results in an (m + n)-bit product. The LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

(TOP VIEW)



- **TWO'S-COMPLEMENT MULTIPLICATION**
- **8-BIT PARALLEL MULTIPLICAND DATA INPUT**
- **SERIAL DATA OUTPUT FOR MULTIPLICATION PRODUCT**
- **MAGNITUDE ONLY MULTIPLICATION**
- **SERIAL MULTIPLIER DATA INPUT**
- **CASCADABLE FOR ANY NUMBER OF BITS**
- **40 MHz TYPICAL MAXIMUM CLOCK FREQUENCY**

INPUTS				INTERNAL	OUTPUT	FUNCTION
CLR	CK	X_j	Y	Y_{-1}	Σ	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output per Booth's algorithm	Shift sum register
H	↑	X	L	H		Add multiplicand to sum register and shift
H	↑	X	H	L		Subtract multiplicand from sum register and shift
H	↑	X	H	H		Shift sum register

H = high-level, L = low-level, X = irrelevant, ↑ = low-to-high-level transition

This is advance information and specifications are subject to change without notice.