MEMORY
CMOS
256M BIT
DOUBLE DATA RATE FCRAM™

MB81N26847A/261647A-22/-24/-30

CMOS 4-BANK x 67,108,864 BIT
Fast Cycle Random Access Memory
with Double Data Rate

■ DESCRIPTION

The Fujitsu MB81N26847A/261647A is a CMOS Fast Cycle Random Access Memory (FCRAM) containing 268,435,456 memory cells accessible in an 8-bit or 16-bit format. The MB81N26847A/261647A features a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81N26847A/261647A is designed to reduce the complexity of using a standard Dynamic RAM (DRAM) which requires many control signal timing constraints. The MB81N26847A/261647A uses Double Data Rate (DDR) where data bandwidth is twice of fast speed compared with regular SDRAMs.

The MB81N26847A/261647A is designed using Fujitsu advanced FCRAM Core Technology.

The MB81N26847A/261647A is ideally suited for Enterprise Servers, Network Systems, Hardware Accelerators, Buffers, and other applications where large memory density and high effective bandwidth are required and where a simple interface is needed.

The MB81N26847A/261647A adopts CMOS I/O interface circuitry, 2.5 V Half-strength SSTL-2 interface, which is capable of extremely fast data transfer of quality.

■ PRODUCT LINE

Parameter		MB81N26847A (x8) / MB81N261647A (x16)		
		-22	-24	-30
Clock Frequency	CL = 3	154 MHz max	143 MHz max	133 MHz max
	CL = 2	133 MHz max	125 MHz max	100 MHz max
Random Access Time		22.5 ns max	24.0 ns max	30.0 ns max
Random Address Cycle Time		30 ns min	32 ns min	40 ns min
DQS Access Time From Clock		+/– 0.85 ns max	+/– 0.9 ns max	+/– 1.0 ns max
Operating Current (I_{DD1S})		170 mA max	165 mA max	150 mA max
Power Down Current (I_{DD2P})		2 mA max	2 mA max	2 mA max

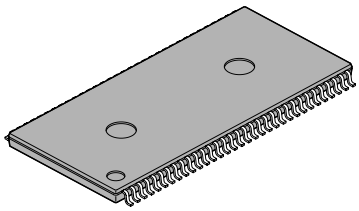
Notice: FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Double Data Rate
- Bi-directional Data Strobe Signal
- Four independent bank operation
- Burst read/write operation
- Programmable burst type, burst length, and CAS latency
- Variable Write Length Control per Byte
- Distributed Auto-refresh cycle in 7.8 μs
- 2.5 V CMOS I/O comply with SSTL_2 (Half Strength Driver)
- V_{DD}: +2.5V Supply ± 0.2V tolerance
- V_{DDQ}: +2.5V Supply ± 0.2V tolerance

■ PACKAGE

Plastic TSOP(II) Package



(FPT-66P-M01)
(Normal Bend)

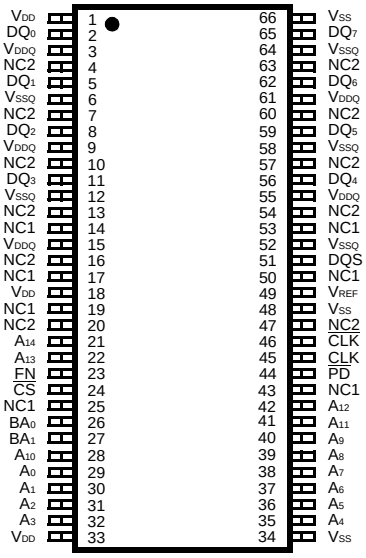
Package and Ordering Information

– 66-pin plastic (400 mil) TSOP-II, order as MB81N26847A/261647A-××FN

■ PIN ASSIGNMENTS AND DESCRIPTIONS #1

Fig. 1 – MB81N26847A PIN ASSIGNMENTS

66-Pin TSOP(II)
(TOP VIEW)

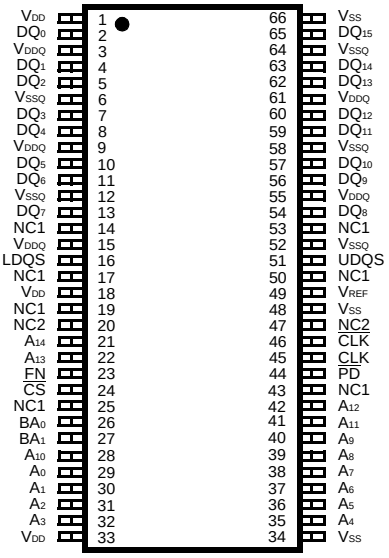


Pin Number	Symbol	Function
1, 3, 9, 15, 18, 33, 55, 61	V_{DD}, V_{DDQ}	Supply Voltage
2, 5, 8, 11, 56, 59, 62, 65	DQ_0 to DQ_7	Data I/O
6, 12, 34, 48, 52, 58, 64, 66	V_{SS}, V_{SSQ}	Ground
21, 22, 28, 29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 41, 42	A_0 to A_{14}	Address Input • Upper: A_0 to A_{14} • Lower: A_0 to A_7
23	FN	Function Select
24	$\overline{CS}$	Chip Select
26, 27	BA_1, BA_0	Bank Address
44	$\overline{PD}$	Power Down
45	CLK	Clock Input
46	$\overline{CLK}$	Clock Input
49	V_{REF}	Input Reference Voltage
51	DQS	Data Strobe
14, 17, 19, 25, 43, 50, 53	NC1	No Connection
4, 7, 10, 13, 16, 20, 47, 54, 57, 60, 63	NC2	No Connection (Left Open)

■ PIN ASSIGNMENTS AND DESCRIPTIONS #2

Fig. 2 – MB81N261647A PIN ASSIGNMENTS

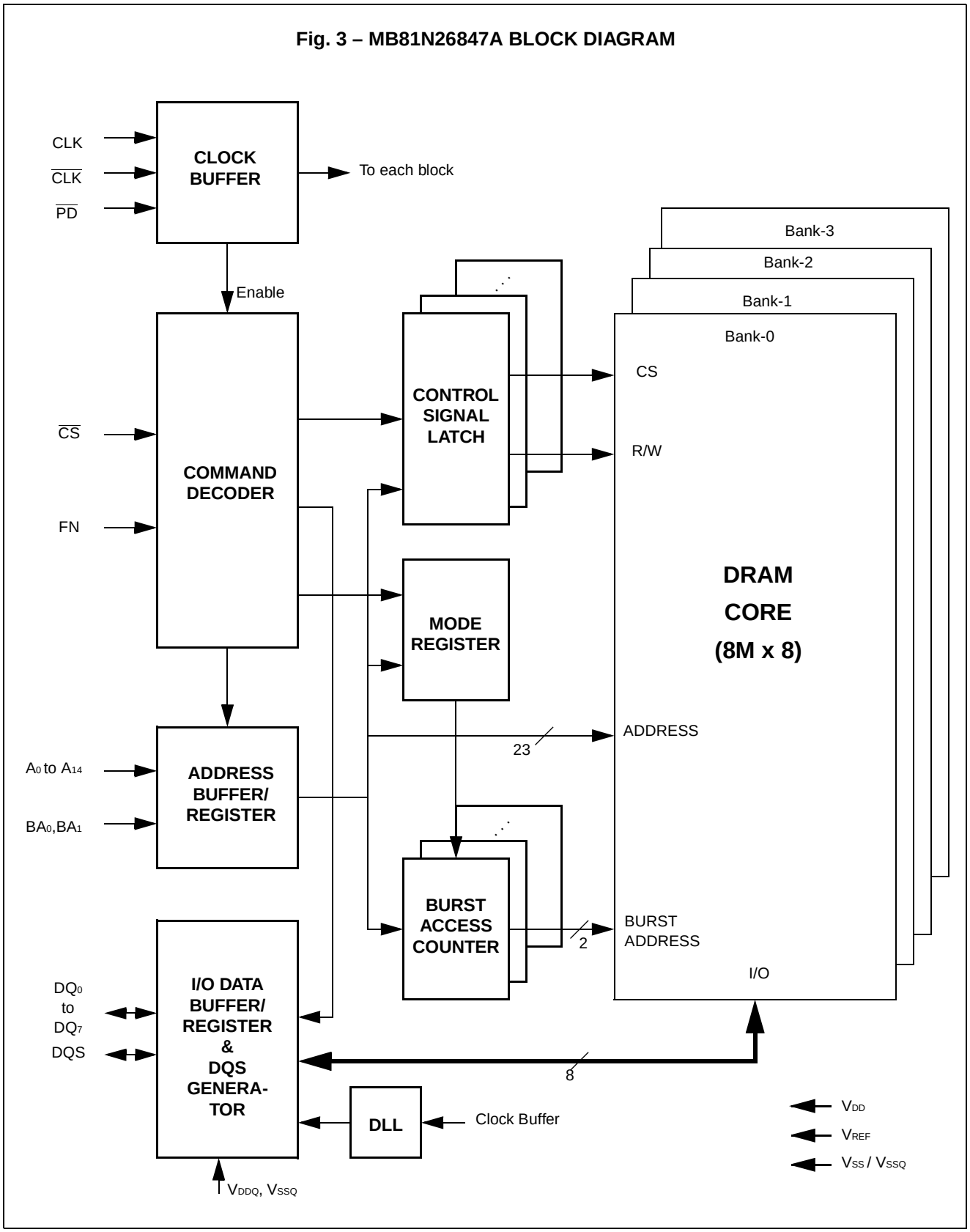
66-Pin TSOP(II)
(TOP VIEW)



Pin Number	Symbol	Function
1, 3, 9, 15, 18, 33, 55, 61	V_{DD}, V_{DDQ}	Supply Voltage
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ_0 to DQ_{15}	Data I/O • Upper: DQ_8 to DQ_{15} • Lower: DQ_0 to DQ_7
6, 12, 34, 48, 52, 58, 64, 66	V_{SS}, V_{SSQ}	Ground
21, 22, 28, 29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 41, 42	A_0 to A_{14}	Address Input • Upper: A_0 to A_{14} • Lower: A_0 to A_6
23	FN	Function Select
24	$\overline{CS}$	Chip Select
26, 27	BA_1, BA_0	Bank Address
44	$\overline{PD}$	Power Down
45	CLK	Clock Input
46	$\overline{CLK}$	Clock Input
49	V_{REF}	Input Reference Voltage
16	LDQS	Lower Byte Data Strobe
51	UDQS	Upper Byte Data Strobe
14, 17, 19, 25, 43, 50, 53	NC1	No Connection
20, 47	NC2	No Connection (Left Open)

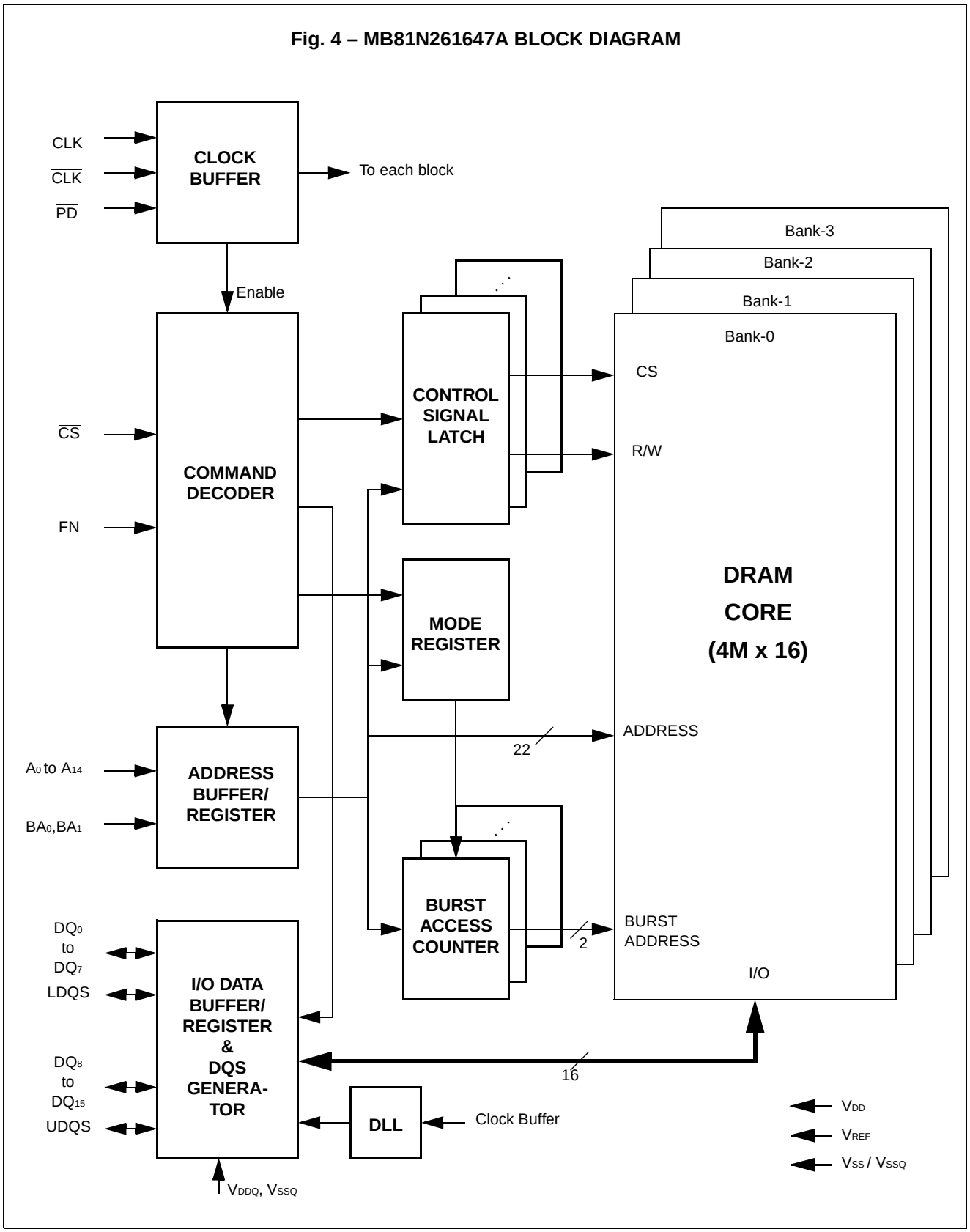
■ BLOCK DIAGRAM #1

Fig. 3 – MB81N26847A BLOCK DIAGRAM



■ BLOCK DIAGRAM #2

Fig. 4 – MB81N261647A BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE Note *1

COMMAND TRUTH TABLE Note *2, and *3

1st Command

Function	Notes	Symbol	$\overline{CS}$	FN	BA_{1-0}	A_{14-0}
Device Deselect		DESL	H	X	X	X
Read (with Auto-close)	*4	RDA	L	H	BA	UA
Write (with Auto-close)	*4	WRA	L	L	BA	UA

2nd Command (1 clock after from RDA or WRA command)

Function	Notes		Symbol	$\overline{CS}$	FN	BA_{1-0}	A_{14-13}	A_{12-11}	A_{10-8}	A_7	A_{6-0}
Lower Address Latch	*5	x16	LAL	H	X	X	V	V	X	X	LA
		x8	LAL	H	X	X	V	X	X	LA	LA
Auto-refresh	*6		REF	L	X	X	X	X	X	X	X
Mode Register Set	*6, *7		MRS	L	X	V	L	L	L	V	V

Notes: *1. L = Logic Low, H = Logic High, X = either L or H, V = Valid (Specified Value), Hi-Z = High Impedance, UA = Upper Address, LA = Lower Address
*2. All commands are assumed to be valid state transitions.
*3. All inputs for command are latched on the cross point of clock input where CLK goes to High.
*4. RDA and WRA commands should only be issued to the back in standby state.
Refer to Figure 5, STATE DIAGRAM, in page 9.
*5. LAL command is the same command state as DESL and used at both Read and Write operation.
A14 to A11 are only used for Variable Write Length control at Write operation.
Refer to READ and WRITE command table below.
*6. Required at Power-up Initialization.
REF and MRS command should only be issued if all banks are in standby state.
*7. Refer to MODE REGISTER TABLE.

READ COMMAND TABLE

Command		$\overline{CS}$	FN	BA_1	BA_0	A_{14} to A_8	A_7	A_6 to A_0
RDA (First)		L	H	BA_1	BA_0	UA	UA	UA
LAL (2nd)	x16	H	X	X	X	X	X	LA
	x8	H	X	X	X	X	LA	LA

WRITE COMMAND TABLE

Command		$\overline{CS}$	FN	BA_1	BA_0	A_{14}	A_{13}	A_{12}	A_{11}	A_{10-8}	A_7	A_6 to A_0
WRA (First)		L	L	BA_1	BA_0	UA	UA	UA	UA	UA	UA	UA
LAL (2nd)	x16	H	X	X	X	LVW0	LVW1	UVW0	UVW1	X	X	LA
	x8	H	X	X	X	VW0	VW1	X	X	X	LA	LA

■ FUNCTION TRUTH TABLE (continued)

VW TRUTH TABLE (Effective during Write mode) Note 8

	Function	Notes	VW0	VW1
BL=2	Write All Words		L	X
	Write First One Word		H	X
BL=4	Reserved	*9	L	L
	Write All Words		H	L
	Write First Two Words		L	H
	Write First One Word		H	H

*8. LVW and UVW controls DQ_{0-7} and DQ_{8-15}, respectively. Unless specifically noted, VW represents both LVW and UVW in later descriptions.
*9. Must not be used

$\overline{PD}$ TRUTH TABLE

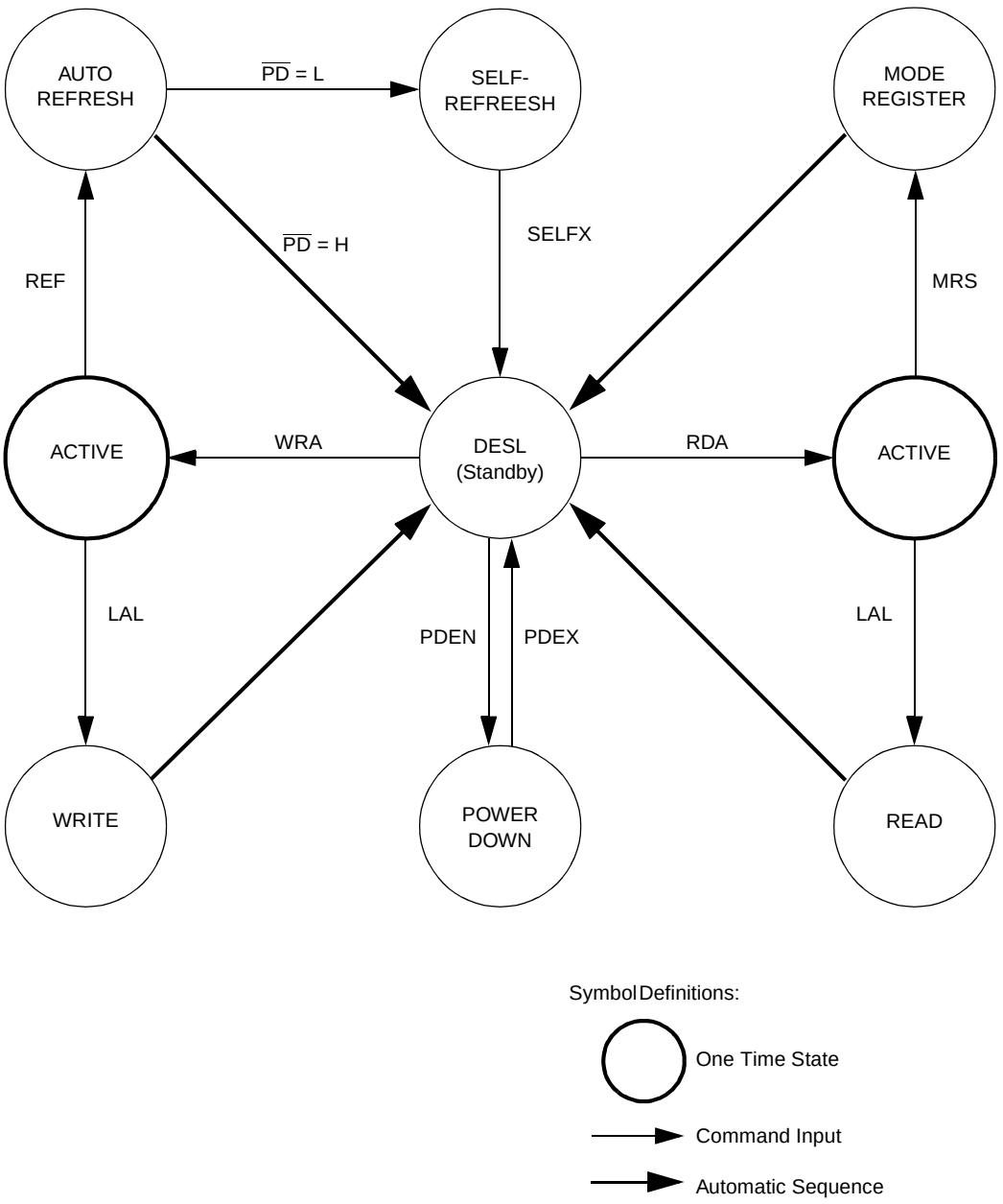
Power Down Table

Current State	Function	Notes	Command	$\overline{PD}$ (n-1)	$\overline{PD}$ (n)	$\overline{CS}$	FN	BA_1	BA_0	A_{14-0}	*11 DQ
Standby	Power Down Entry		PDEN	H	L	H	X	X	X	X	Hi-Z
Power Down	Power Down Continue		—	L	L	X	X	X	X	X	Hi-Z
Power Down	Power Down Exit		PDEX	L	H	H	X	X	X	X	Hi-Z
Active	Self-refresh Entry	*10	REF	H	L	L	X	X	X	X	Hi-Z
Self-refresh	Self-refresh Continue		—	L	L	X	X	X	X	X	Hi-Z
Self-refresh	Self-refresh Exit		SELFX	L	H	H	X	X	X	X	Hi-Z
Read / Write	Illegal		—	H	L	X	X	X	X	X	Hi-Z
other than above	Illegal		other than above	H	L	any					

*10. $\overline{PD}$ can be brought to Low within t_{FPDL} from REF command for Self-refresh entry.
*11. $\overline{PD}$ has asynchronous OE function but its AC parameters wil not be guaranteed.

■ STATE DIAGRAM

Fig. 5 – STATE DIAGRAM (Simplified for Single Bank Operation)



■ FUNCTIONAL DESCRIPTION

FCRAM™

The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time. The FCRAM also provides low latency and low power consumption than regular DRAMs.

DDR, Double Data Rate Function

The regular SDRAM read and write cycle have only used the rising edge of external clock input. When clock signal goes to High from Low at the read mode, the read out data will be available at every rising clock edge after the specified latency up to burst length. The MB81N26847A/261647A DDR FCRAM features a twice of data transfer rate within the same clock period by transferring data at every rising and falling clock edge.

CLOCK (CLK, $\overline{CLK}$)

The MB81N26847A/261647A adopts differential clock scheme. CLK is a master clock and its rising edge is used to latch all command and address inputs. $\overline{CLK}$ is a complementary clock input.
The MB81N26847A/261647A implements Delay Locked Loop (DLL) circuit. This internal DLL tracks the signal cross point between CLK and $\overline{CLK}$ and generate some clock cycle delay for the output buffer control at Read mode.
The internal DLL circuit requires some Lock-on time for the stable delay time generation. In order to stabilize the delay, a constant stable clock input for t_{LOCK} period is required during the Power-up initialization and a constant stable clock input for t_{LOCK} period is also required after Self-refresh exit as specified t_{LOCK} prior to RDA command.

POWER DOWN ($\overline{PD}$)

$\overline{PD}$ is a synchronous input signal and enables low power mode; Power Down and Self-refresh mode.
The Power Down mode is entered when $\overline{PD}$ is brought to Low while all banks are in idle state and exited when it return to High.

$\overline{PD}$ must be brought to Low within the timing between t_{FPDL}(min) and t_{FPDL}(max) to Self-refresh mode.

When $\overline{PD}$ is bourght to Low after t_{PDV}, FCRAM perform Auto-refresh and enter Power Down mode.
During the Power Down and Self-refresh mode, both CLK and $\overline{CLK}$ are disabled after specified time.
$\overline{PD}$ does not have a Clock Suspend function unlike CKE pin of regular SDRAMs, and it is illegal to bring $\overline{PD}$ into Low if any read or write operation is being performed. For the detail, refer to STATE DIAGRAM.
It is recommended to maintain $\overline{PD}$ to be Low until V_{DD} gets in the specified operating range in order to assure the power-up initialization.

CHIP SELECT ($\overline{CS}$) and FUNCTION SELECT (FN)

Unlike regular SDRAMs' command input signals, the MB81N26847A/261647A has only two control signals; $\overline{CS}$ and FN.
Each operation is determined by two consecutive command input. Refer to FUNCTION TRUTH TABLE in page 7.

■ FUNCTIONAL DESCRIPTION (continued)

BANK ADDRESS (BA_0, BA_1)

The MB81N26847A/261647A has four internal banks. Bank selection by BA occurs at Read (RDA) or Write (WRA) command.

ADDRESS INPUTS (A_0 to A_{14})

Address input selects an arbitrary location of each memory cell matrix within each bank. MB81N26847A/261647A adopts an address multiplexer in order to reduce the pin count of the address lines. At either RDA or WRA command, fifteen Upper addresses are initially latched as well as two bank addresses and the remainder of Lower addresses are then latched by an LAL command. Refer to FUNCTIONAL TRUTH TABLE.

DATA STROBE (DQS)

DQS is a bi-directional signal and used as data strobe. During Read operation, DQS provides the read data strobe signal that is intended to use input data strobe signal at the receiver circuit of the controller(s). It turns Low before first data is coming out and toggle High to Low or Low to High till end of burst read. Refer to the timing diagrams.
The CAS Latency is specified to the first Low to High transition of this DQS output.
During the write operation, DQS is used to latch corresponding byte of write data signals. As well as the behavior of read data strobe, the first rising edge of DQS input latches first input data and following falling edge of DQS signal latches second input data. This sequence shall be continued till end of burst count. Therefore, DQS must be provided from the driver circuit of the controller that drives write data.
Note that DQS input signal should not be tristated from High at the end of write mode, and LDQS and UDQS of MB81N261647 are for Lower Byte Data (DQ_{0-7}) and Upper Byte Data (DQ_{8-15}), respectively.

DATA INPUTS AND OUTPUTS (DQ_n)

Input data is latched by DQS input signal and written into memory at the clock following the write command input.
Output data is obtained together with DQS output signals at programmed read CAS latency.
The polarity of the output data is identical to that of the input. Data is valid from DQS output signal transition (t_{QSQ}) till next transition as specified in Data Valid Time from DQS (t_{QSQV}).

READ (RDA) and LOWER ADDRESS LATCH (LAL)

The MB81N26847A/261647A adopts two consecutive command input scheme. The read or write operation is determined at first RDA or WRA command input from Standby state of the bank to be accessed.
Refer to Figure 5, STATE DIAGRAM in page 9.

The read mode is entered when RDA command is asserted with Bank Address and Upper Address input and LAL command with Lower Address input must be followed at next clock input. The output data is then valid after programmed CAS Latency (CL) from a clock at LAL command till end of burst. The read mode is automatically exited after I_{RC}, Random Cycle Latency.

Refer to FUNCTION TRUTH TABLE.

■ FUNCTIONAL DESCRIPTION (continued)

WRITE (WRA), LOWER ADDRESS LATCH (LAL) and VERIABLE WRITE LENGTH

The write mode is entered and exited as the same manner as read mode. The input data store is started at the rising edge of DQS input from CL-1 till end of burst count. Refer to FUNCTION TRUTH TABLE.

The MB81N26847A/261647A write operation has a feature of “on-the-fly” Variable Write Length (VW) at every LAL command input following WRA command.
Unlike Data Mask (DM) of regular DDR SDRAM, VW does not provide random data mask capability and the VW controls the burst counter for the write burst and its burst length is set by a combination of two control addresses, VW0 and VW1, and programmed Burst Length condition. Refer to VW TRUTH TABLE in page 8.
The data in masked address location remain unchanged.

Note that the DQS signal input must be continued till end of burst length set by Burst Length (BL) at standard mode register field regardless of actual write burst count set by VW.
During read cycle, the VW field is inactive and does not have any effect on read operation.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access and MB81N26847A/261647A read and write operations are burst oriented. The burst mode is implemented by keeping the same addresses and by automatic strobing least significant addresses in every single clock edge till programmed burst length (BL). Access time from clock of burst mode is specified as t_{AC}. The internal lower address counter operation is determined by a mode register which defines burst type (BT) and burst count length(BL) of 2 or 4 bits of boundary.

The burst type can be selected either sequential or interleave mode. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to the least significant address(= 0). The interleave mode is a scrambled decoding scheme for A_0 to A_1 of Lower Address depending on the burst length. If the first access of lower address is even (0), the next address will be odd (1), or vice-versa.

BURST ORDER

Burst Length	Starting Lower Address		Sequential	Interleave
	A_1	A_0		
2	—	0	0 – 1	0 – 1
	—	1	1 – 0	1 – 0
4	0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
		1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
		1	3 – 0 – 1 – 2	3 – 2 – 1 – 0

■ FUNCTIONAL DESCRIPTION (continued)

MODE REGISTER SET (MRS)

The mode register provides a variety of different operations as specified above and can be programmed MRS command following RDA command input if all banks are in standby state. Note that the read operation initiated by RDA command is cancelled if MRS command is asserted at next clock input from RDA command instead of LAL command required for read operation.
The MB81N26847A/261647A has two registers; Standard and Extended mode register. The Standard mode register has four operation fields; Burst Length, Burst Type, CAS Latency, and Test Mode (This Test Mode must not be used.) The Extended mode register has two fields; DLL Enable and Output Driver Strength.
Refer to MODE REGISTER TABLE in page 15.
These two registers are selected by BA0 at MRS command entry and each field is also set by the address line at MRS command as well. Once those fields are programmed, the contents will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all banks are in idle state and all outputs are in High-Z. The condition of the mode register is undefined after the power-up stage and it is required to set each field after initialization.
Refer to POWER-UP INITIALIZATION below.

AUTO-REFRESH (REF)

The memory core of MB81N26847A/261647A is the same as conventional DRAM's capacitor cell and requires refresh operation to maintain the data written into the cell. The Auto-refresh mode is entered by REF command following to WRA command. REF command should only be issued under condition that all banks are in idle state and all outputs are in High-Z. Note that the write operation initiated by WRA command is cancelled if REF command is asserted at next clock input from WRA command instead of LAL command required for write operation.

The Auto-refresh command should also be issued within every 7.8 μs period. In case of burst refresh operation, more than 8 consecutive auto-refresh should not be performed within 400ns as average of 8 refresh. In other words, at least 3.2 μs (8 times 400ns) must be waited for next 8 consecutive refresh operation.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh operation until cancelled by SELFX.
The Self-refresh mode is entered by applying an REF command (that is following WRA command) in conjunction with $\overline{PD}$ = Low (SELF) or $\overline{PD}$ to bring LOW within the timing between t_{FPDL} (min) and t_{FPDL} (max) from REF command. However when $\overline{PD}$ is brought to Low after l_{PDV}, FCRAM perform Auto-refresh and enter Power Down mode. Note that actual Self-refresh mode will be entered after Auto-refresh operation. The DESL command must be kept for at least l_{REFC} period and clock input must also be kept for at least l_{CKD} period. Once MB81N26847A/261647A enters the self-refresh mode, all inputs except for $\overline{PD}$ can be either logic high or low level state and outputs will be in a High-Z state. During Self-refresh mode, $\overline{PD}$ = Low should be maintained. SELF command should only be issued under condition that all banks are in idle state and all outputs are in High-Z.

SELF-REFRESH EXIT (SELFX)

To exit Self-refresh mode, $\overline{PD}$ must brought to High for at least 2 clock cycles together with DESL condition.
Refer to Timing Diagram for the detail procedure. It is recommended to issue at least one Auto-refresh command just after the l_{REFC} period to avoid the violation of refresh period.

WARNING: A stable clock for l_{LOCK} period with a constant duty cycle must be supplied prior to applying any command other than Auto-refresh command to insure the DLL is locked against the latest device conditions.

■ FUNCTIONAL DESCRIPTION (continued)

POWER-UP INITIALIZATION

The MB81N26847A/261647A internal condition at and after power-up will be undefined. Since MB81N26847A/261647A does not have designated reset function, following procedure must be followed in order to initialize internal state machine, DLL, and forcing DRAM to be a standby state.

1. Apply V_{DD} before or the same time as V_{DDQ} and attempt to maintain $\overline{PD}$ to be equal or less than 0.2V before power supply injection.
2. Apply V_{DDQ} before or same time as V_{REF}.
3. Apply V_{REF}.
4. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200µs.
5. Maintain stable power and clock, apply DESL command with either A_8 = Low or A_7 = High and take $\overline{PD}$ to High state.
6. Keep $\overline{CS}$ = High and set either or both BA = Low. (note *1)
7. Set $\overline{CS}$ = Low with $BA_{[1-0]}$ = $A_{[14-8]}$ = High, A_7 = Low for two clocks (MRS command with Reset Address)
8. Set $\overline{CS}$ = High and maintain same address input for a minimum of 4 clocks.
9. Keep $\overline{CS}$ = High and change one or more address input within $BA_{[1-0]}$ to $A_{[14-7]}$ and maintain them for a minimum of 4 clocks.
10. Set Extended mode register to enable DLL. (note *2)
11. Set Standard mode register. (note *2)
12. Issue Auto-refresh commands twice or more. (note *2)
13. Issue Write command to all four banks after minimum l_{LOCK} clocks from Extended mode register programming. (note *3)
14. Ready for normal operation.

Notes: *1. The reset/initialization after Power-up can be also performed if the procedure from step 6 to step 12 are issued. Refer to RESET CONDITION below.
*2. These steps can be issued in random order. For example, Auto-refresh command can be issued prior to Extended mode register programming of step 10.
*3. Order of bank address can be arbitrarily but must be write to all banks before normal operation.

RESET CONDITION

Clock	Command	CS	FN	BA1	BA0	A14-9	A8	A7	A6-0
n-13:1 *1	DESL	H	X	X or L	L or X	X	L or X	X or H	X
n	RDA	L	H	X	X	X	X	X	X
n+1	MRS	L	X	H	H	H	H	L	X
n+2:5	DESL	H	X	H	H	H	H	L	X
n+6	DESL	H	X	Note *2					X
n+7:10	DESL	H	X	Note *3					X

Notes: *1. DESL condition must be maintained at least 12 clocks.
*2. At least one address bit must be flipped from previous state.
*3. Same address input conditions at n+6 state must be maintained at least 4 clocks.

■ MODE REGISTER TABLE

STANDARD MODE REGISTER

ADDRESS	BA_1	BA_0	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
STANDARD MODE REGISTER	0*1	0*1	0							TM	CL			BT	BL		

A_6	A_5	A_4	CAS Latency (CL)
0	0	X	RESERVED *2
0	1	0	2
0	1	1	3
1	X	X	RESERVED

A_2	A_1	A_0	Burst Length (BL)
0	0	0	RESERVED
0	0	1	2
0	1	0	4
0	1	1	RESERVED
1	X	X	RESERVED

A_7	Test Mode (TM)
0	Regular Mode (Default)
1	Test Mode (supplier specific mode) *3

A_3	Burst Type (BT)
0	Sequential (Wrap round, Binary up)
1	Interleave (Wrap round)

EXTENDED MODE REGISTER *1

ADDRESS	BA_1	BA_0	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
EXTENDED MODE REGISTER	0*1	1*1	RESERVED *4													OD	DE

A_1	Output Driver Strength (OD)
0	Standard Strength *5
1	RESERVED *5

A_0	DLL Enable (DE)
0	DLL Enable *6
1	DLL Disable

Notes: *1. A combination of BA_1 = BA_0 = 0 (Low) selects Standard mode register, a combination of BA_1 = 0 and BA_0 = 1 (High) selects Extended mode register, and a combination of BA_1 = BA_0 = 1 can only be used at RESET operation.
*2. The RESERVED field in Standard mode register must not be used.
*3. Must not be used. A7 = 1 should only be used at power-up initialization and RESET.
*4. The RESERVED field in Extended mode register must be set as 0.
*5. A1 of Extended mode register must always be set at 0.
*6. Must be set at power-up initialization.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{DDQ}	–0.3 to +3.6	V
Input Reference Voltage	V_{REF}	–0.3 to +3.6	V
Input Voltage	V_{IN}	–0.3 to V_{DDQ} + 0.3	V
Output Voltage	V_{OUT}	–0.3 to V_{DDQ} + 0.3	V
Output Short Circuit Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	–55 to +150	°C
Operating Temperature	T_{OPR}	0 to +70	°C
Soldering Temperature(10s)	T_{SOLDER}	260	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	2.3	2.5	2.7	V
		V_{DDQ}	2.3	V_{DD}	V_{DD}	V
Input Reference Voltage	*3	V_{REF}	V_{DDQ}/2 * 96%	V_{DDQ}/2	V_{DDQ}/2 * 104%	V
Single Ended DC Input High Level	*5	$V_{IH(DC)}$	V_{REF} + 0.2		V_{DDQ} + 0.2	V
Single Ended DC Input Low Level	*5	$V_{IL(DC)}$	–0.1	—	V_{REF} – 0.2	V
Single Ended AC Input High Level	*6	$V_{IH(AC)}$	V_{REF} + 0.35	—	V_{DDQ} + 0.2	V
Single Ended AC Input Low Level	*6	$V_{IL(AC)}$	–0.1	—	V_{REF} – 0.35	V
Differential Clock DC Input Level		$V_{ICK(DC)}$	–0.1	—	V_{DDQ} + 0.1	V
Differential DC Input Differential Level	*7	$V_{ID(DC)}$	0.4	—	V_{DDQ} + 0.2	V
Differential AC Input Differential Level	*7	$V_{ID(AC)}$	0.7	—	V_{DDQ} + 0.2	V
Differential AC Input Cross Point Level	*8	$V_{X(AC)}$	V_{DDQ}/2 – 0.2	—	V_{DDQ}/2 + 0.2	V
Differential AC Input Signal Offset Level	*4	$V_{ISO(AC)}$	V_{DDQ}/2 – 0.2	—	V_{DDQ}/2 + 0.2	V
Ambient Temperature		T_A	0	—	70	°C

■ RECOMMENDED OPERATING CONDITIONS(Continued)

Notes: *1. Overshoot greater than the $V_{IH(AC)}$ maximum limit is V_{DD} + 0.9V for pulse width ≤ 5 ns. Refer to Figure 6.
*2. Undershoot greater than the $V_{IL(AC)}$ minimum limit is V_{SS} – 0.9V for pulse width ≤ 5 ns. Refer to Figure 7.
*3. V_{REF} is expected to track variations in the DC level of V_{DDQ} of the transmitting device. Peak-to-Peak noise level on V_{REF} may not exceed +/- 2% of the supplied DC value.
*4. V_{ISO} means {$V_{ICK(CLK)}$ + $V_{ICK(\overline{CLK})}$} / 2. Refer to Figure 8.
*5. $V_{IH(DC)}$ and $V_{IL(DC)}$ are levels to maintain the current logic state.
*6. $V_{IN(AC)}$ and $V_{IL(AC)}$ are levels to change to the new logic state.
*7. V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.
*8. The value of $V_{X(AC)}$ is expected to equal V_{DDQ}/2 of the transmitting device.
*9. In case of external termination, VTT (Termination Voltage) must be within a range of $V_{REF(DC)}$ +/- 0.04V.

Overshoot and Undershoot Definition

Fig. 6 – Overshoot Definition

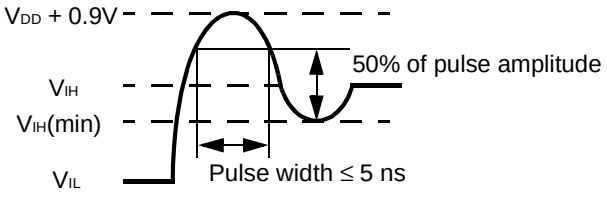
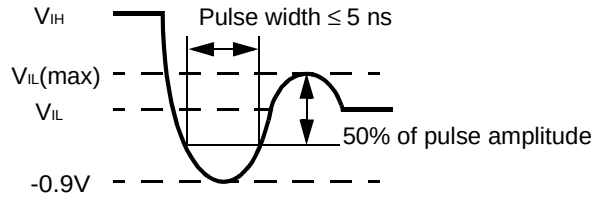
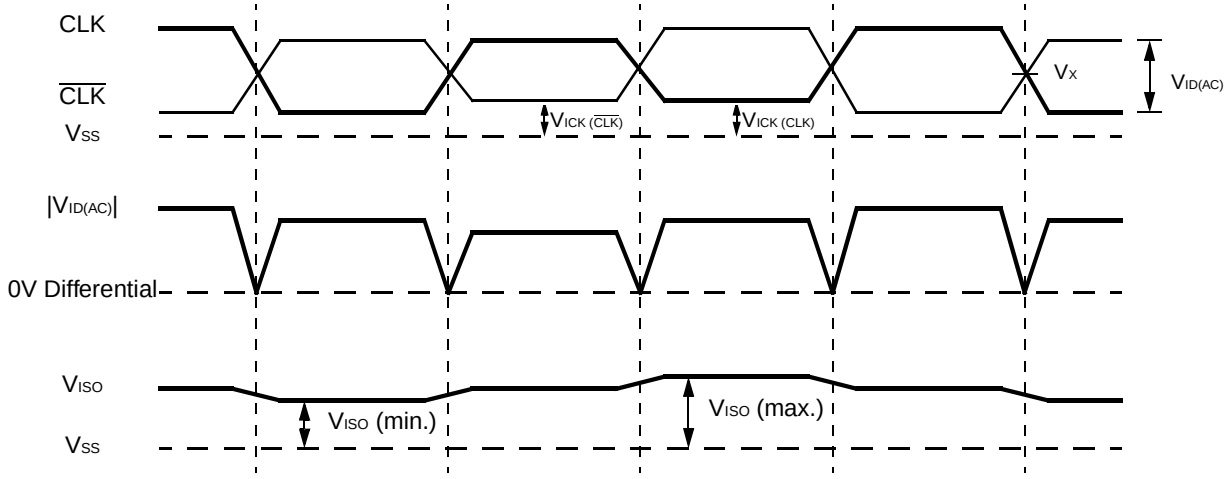


Fig. 7 – Undershoot Definition



Differential Input Signal Definition

Fig. 8 – Differential Input Signal Offset Voltage (For Clock Input)



■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Pin Capacitance	C_{IN1}	2.5	—	4.0	pF
Input Pin Capacitance	C_{IN2}	2.5	—	4.0	pF
I/O Pin Capacitance	$C_{I/O}$	4.0	—	6.0	pF
NC1 Pin Capacitance	C_{NC1}	—	—	1.5	pF
NC2 Pin Capacitance *	C_{NC2}	4.0	—	6.0	pF

Note:*The NC2 pins have additional capacitance for adjustment of adjacent pin capacitance. The NC2 pins have power and Ground clamp.

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) **Note *1,*2**

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Output Source Current		I_{OH}	V_{DDQ} = 2.3V for min, 2.7V for max V_{OH} = V_{DDQ}-0.4V	-10.0	—	mA
Output Sink Current		I_{OL}	V_{DDQ} = 2.3V for min, 2.7V for max V_{OL} = +0.4V	10.0	—	mA
Input Leakage Current (any input)		I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}; All other pins not under test = 0 V	-5	5	µA
Output Leakage Current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{DDQ}; Data out disabled	-5	5	µA
V_{REF} Current		I_{REF}		-5	5	µA
Operating Current (Average Power Supply Current) *3,*4	-22	I_{DD1S}	t_{CK} = min, I_{RC} = min, Burst Length = 4, One bank active, Read/Write command cycling, Address change up to 2 times during minimum I_{RC}, 0 V ≤ V_{IN} ≤ $V_{IL(AC)}$ (max), $V_{IH(AC)}$ (min) ≤ V_{IN} ≤ V_{DDQ}	—	170	mA
	-24			—	165	
	-30			—	150	
Standby Current *3	-22	I_{DD2N}	$\overline{PD}$ = V_{IH}, t_{CK} = min All banks idle, DESL commands only, Other input signals are changed one time during four clock inputs, 0 V ≤ V_{IN} ≤ $V_{IL(AC)}$ (max), $V_{IH(AC)}$ (min) ≤ V_{IN} ≤ V_{DDQ}	—	45	mA
	-24			—	40	
	-30			—	35	
Power Down Current *3		I_{DD2P}	$\overline{PD}$ = $V_{IL(AC)}$, t_{CK} = min All banks idle, 0 V ≤ V_{IN} ≤ V_{DDQ}	—	2	mA
Auto-refresh Current (Average Power Supply Current) *3	-22	I_{DD5}	Auto-refresh; t_{CK} = min, I_{REFC} = min, t_{REFI} = min, Address change up to 2 times during minimum I_{REFC}, 0 V ≤ V_{IN} ≤ $V_{IL(AC)}$ (max), $V_{IH(AC)}$ (min) ≤ V_{IN} ≤ V_{DDQ}	—	65	mA
	-24			—	60	
	-30			—	55	
Self-refresh Current (Average Power Supply Current)		I_{DD6}	Self-refresh; $\overline{PD}$ = 0.2V, 0 V ≤ V_{IN} ≤ V_{DDQ}	—	3	mA

Notes: *1. All voltages referenced to V_{SS}.
*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
*3. I_{DD} depends on the output termination or load conditions, clock cycle rate, and number of address and command change within certain period.
*4. The specified values are obtained with the output open.

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note *1,*2,*3

AC PARAMETERS

Parameter	Notes	Symbol		– 22		– 24		– 30		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period		t_{CK}	CL = 3	6.5	10.0	7.0	10.0	7.5	10.0	ns
			CL = 2	7.5	10.0	8.0	10.0	10.0	10.5	ns
Input Setup Time (Except for LDQS/UDQS and Data)	*4	t_{IS}		1.0	—	1.2	—	1.6	—	ns
Input Hold Time (Except for LDQS/UDQS and Data)	*4	t_{IH}		1.0	—	1.2	—	1.6	—	ns
Command and Address Input Pulse Width (each device)	*4	t_{IPW}		2.2	—	2.6	—	3.4	—	ns
Data Input Setup Time	*5	t_{DS}		0.6	—	0.6	—	0.8	—	ns
Data Input Hold Time	*5	t_{DH}		0.6	—	0.6	—	0.8	—	ns
Data Input Pulse Width	*5	t_{DIPW}		1.9	—	1.9	—	2.3	—	ns
DQS First Input Setup Time	*4,*6	t_{DSPRES}		0	—	0	—	0	—	ns
DQS Input Falling Edge to Clock Setup Time	*5	t_{DSS}	CL = 3	1.5	—	1.5	—	1.6	—	ns
			CL = 2	1.5	—	1.6	—	2.0	—	ns
DQS Last Low Input (Postamble) Hold Time	*4	t_{DSPSTH}	CL = 3	1.5	—	1.5	—	1.6	—	ns
			CL = 2	1.5	—	1.6	—	2.0	—	ns
DQS Access Time from CLK	*4,*7	t_{CKQS}		-0.85	0.85	-0.9	0.9	-1.0	1.0	ns
Data Output skew from DQS	*5	t_{QSQ}		-0.52	0.52	-0.56	0.56	-0.64	0.64	ns
Data Access Time from CLK	*4,*7	t_{AC}		-0.85	0.85	-0.9	0.9	-1.0	1.0	ns
Data Output in Low-Z	*4,*7,*8	t_{LZ}		-0.85	—	-0.9	—	-1.0	—	ns
Data Output Valid Time	*4,*7	t_{OH}		-0.85	0.85	-0.9	0.9	-1.0	1.0	ns
Data Output in High-Z	*4,*7,*9	t_{HZ}		—	0.85	—	0.9	—	1.0	ns
DQS Output in Low-Z (Preamble Setup Time)	*4,*7,*8	t_{QSLZ}		-0.85	—	-0.9	—	-1.0	—	ns
DQS Output in High-Z	*4,*7,*9	t_{QSHZ}		-0.85	0.85	-0.9	0.9	-1.0	1.0	ns
Last Output to $\overline{PD}$ High Hold Time		t_{QPDH}		0	—	0	—	0	—	ns
$\overline{PD}$ Low Input Window for Self-refresh Entry	*4,*10	t_{FPDL}		-0.5*t_{CK}	10.0	-0.5*t_{CK}	10.0	-0.5*t_{CK}	10.0	ns
Power Down Exit Time	*4	t_{PDEX}		2.0	—	2.0	—	3.0	—	ns
Auto-refresh Interval	*11	t_{REFI}		0.4	7.8	0.4	7.8	0.4	7.8	µs
Pause Time after Power-up	*12	t_{PAUSE}		200	—	200	—	200	—	µs
Input Transition Time	*13	t_T		0.2	1.0	0.2	1.0	0.2	1.0	ns

■ AC CHARACTERISTICS (continued)

AC PARAMETERS (FREQUENCY DEPENDANT) Note *10

Parameter	Notes	Symbol	Min.	Max.	Unit
Clock High Time	*4	t_{CH}	0.45 * t_{CK}	—	ns
Clock Low Time	*4	t_{CL}	0.45 * t_{CK}	—	ns
DQS Low to High Setup Time	*4,*14	t_{DQSS}	0.75 * t_{CK}	1.25 * t_{CK}	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)	*6	t_{DSPRE}	0.4 * t_{CK}	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	*4,*6	t_{DSPREH}	0.25 * t_{CK}	—	ns
DQS High or Low Input Pulse Width [Not applicable to last Postamble]	*5	t_{DSP}	0.45 * t_{CK}	0.55 * t_{CK}	ns
DQS Last Low Input (Postamble) Pulse Width	*5,*15	t_{DSPST}	0.45 * t_{CK}	—	ns
LDQS to UDQS Input Skew [Applicable to MB81N261647A only]	*5	t_{DSSK}	– 0.25 * t_{CK}	0.25 * t_{CK}	ns
DQS Preamble Pulse Width	*4	t_{QSPRE}	0.9 * t_{CK} – 0.2	1.1 * t_{CK} + 0.2	ns
DQS Pulse Width		t_{QSP}	0.4 * t_{CK} – 0.2	—	ns
Data Output Valid Time from DQS		t_{QSQV}	0.4 * t_{CK} – 0.4	—	ns

■ AC CHARACTERISTICS (continued)

LATENCY

(The latency values on these parameters are fixed regardless of clock period.)

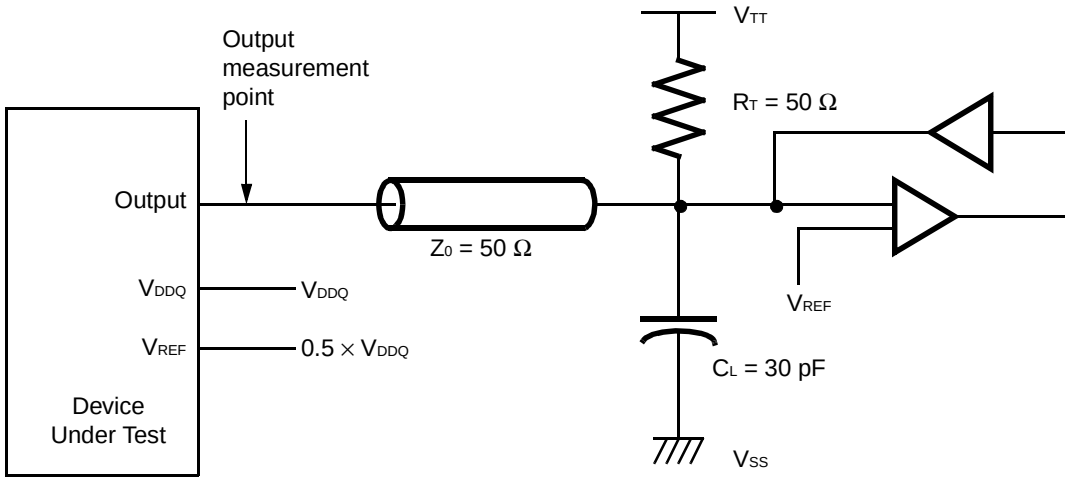
Parameter	Note	Symbol		BL = 2	BL = 4	Unit
Random Read/Write Cycle Time (minimum) [Applicable to same bank]		t_{RC}	CL = 3	5	5	t_{CK}
			CL = 2	4	4	t_{CK}
RDA or WRA to LAL Command Input Delay [Applicable to same bank]		t_{RCD}	CL = 3	1	1	t_{CK}
			CL = 2	1	1	t_{CK}
LAL to RDA or WRA Command Input Delay (minimum) [Applicable to same bank]		t_{RAS}	CL = 3	4	4	t_{CK}
			CL = 2	3	3	t_{CK}
Random Bank Access Delay (minimum) [Applicable to other bank]		t_{RBD}	CL = 3	2	2	t_{CK}
			CL = 2	2	2	t_{CK}
LAL following RDA to WRA Delay Time (minimum) [Applicable to other bank]		t_{RWD}	CL = 3	2	3	t_{CK}
			CL = 2	2	3	t_{CK}
LAL following WRA to RDA Delay Time (minimum) [Applicable to other bank]	*15	t_{WRD}	CL = 3	1	1	t_{CK}
			CL = 2	1	1	t_{CK}
$\overline{PD}$ Low to Input Inactive		t_{PD}		1	1	t_{CK}
$\overline{PD}$ High to Input Active		t_{PDA}		1	1	t_{CK}
Power Down mode valid from REF command		t_{PDV}	CL = 3	4	4	t_{CK}
			CL = 2	3	3	t_{CK}
Auto-refresh Cycle Time (minimum)		t_{REFC}	CL = 3	15	15	t_{CK}
			CL = 2	12	12	t_{CK}
Mode Register Set Cycle Time (minimum)	*16	t_{RSC}	CL = 3	5	5	t_{CK}
			CL = 2	4	4	t_{CK}
REF Command to Clock Input Disable at Self-refresh Entry (minimum)		t_{CKD}		16	16	t_{CK}
DLL Lock-on Time (Applicable to RDA command)		t_{LOCK}	$t_{CK} \leq$ 8ns	200	200	t_{CK}
			$t_{CK} \leq$ 10.5 ns	300	300	t_{CK}

■ AC CHARACTERISTICS (continued)

Notes: *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure and stable clock input with constant clock period and with 50% duty cycle.
*2. Access Times assume input slew rate of 1ns/volt between V_{REF}+0.35V to V_{REF}-0.35V, where V_{REF} is V_{DDQ}/2, with parallel termination load conditions. Refer to AC TEST LOAD CIRCUIT in page 23.
*3. V_{REF} = 1.25V is a typical reference level for measuring timing of input signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max) unless otherwise noted.
Refer to AC TEST CONDITIONS in page 23.
*4. This parameter is measured from the cross point of CLK and $\overline{CLK}$ input.
*5. This parameter is measured from signal transition point of DQS input crossing V_{REF} level.
*6. Not applicable if consecutive write operation within l_{RBD} (min) is performed.
*7. This parameter depends on the clock jitters.
*8. Low-Z (Low Impedance State) is specified and measured at V_{DDQ} / 2 +/- 200mV from steady state.
*9. High-Z is specified where output buffer is no longer driven.
*10. If the result of nominal calculation with regard to tCK contains more than one decimal place, the result should be rounded up to the nearest decimal place.
e.g., if t_{CK}=6.5ns and formula is 0.5*t_{CK}, the result is rounded up to 3.3ns.
*11. The t_{REFI} (max) is applicable for equally distributed refresh method.
The t_{REFI} (min) is applicable for burst refresh method. In such case, more than 8 consecutive auto-refresh operation should not be performed within 400ns as average of 8 refresh. In other words, at least 3.2 µs (8 times 400ns) must be waited for next 8 consecutive refresh operation.
*12. Specified when the clock input is started on the condition of the stable supply voltage
*13. Defined as the transition time between $V_{IH(AC)}$ (min) and $V_{IL(AC)}$ (max).
*14. More than 2 signal edge of DQS should not be input within 1 clock (t_{CK}) cycle.
*15. The maximum value is not a device limit and is a reference value when minimum l_{WRD} at BL=4 is applied.
*16. The l_{RSC} is 5 clock cycles before CL programming during power-up sequence.

■ AC CHARACTERISTICS (continued)

Fig. 9 – AC TEST LOAD CIRCUIT

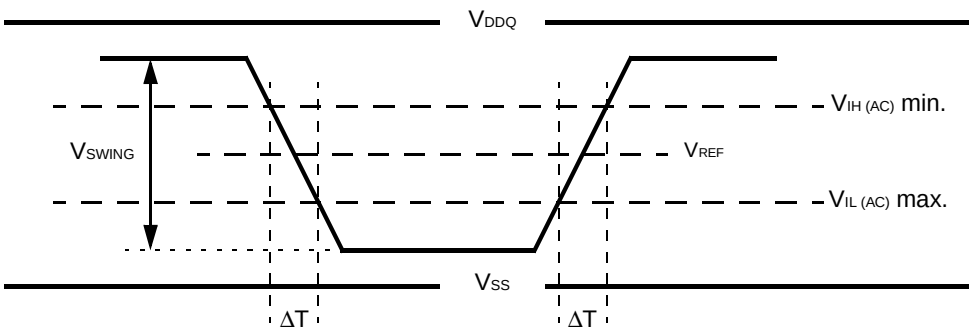


Note: AC characteristics are measured in this condition. This load circuit is not applicable for DC Test.

AC TEST CONDITIONS

Parameters	Symbol	Value	Unit
Input High Level	V_{IH}	V_{REF} + 0.35	V
Input Low Level	V_{IL}	V_{REF} – 0.35	V
Input Reference Level	V_{REF}	V_{DDQ}/2	V
Output Timing Measurement Reference Level	V_{OTR}	V_{DDQ}/2	V
Termination Voltage	V_{TT}	V_{REF}	V
Input Peak to Peak Swing Level	V_{SWING}	1.0	V
Differential Input Level	$V_{ID(AC)}$	1.5	V
Differential Input Reference Level	Vr	$V_{x(AC)}$	V
Input Slew Rate	SLEW	1.0	V/ns

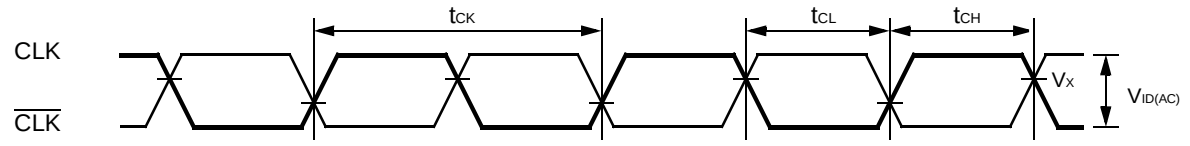
Fig. 10 – AC TEST TIMING SETUP



Note: SLEW is measured between V_{REF}+0.35V to V_{REF}–0.35V in a ΔT period.

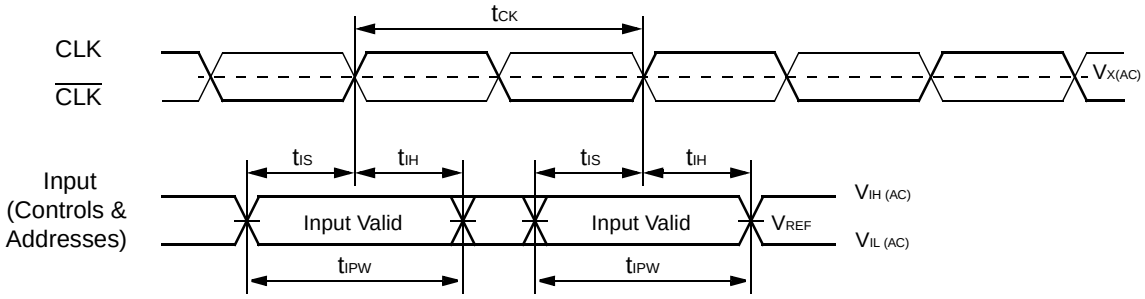
■ AC CHARACTERISTICS (continued)

Fig. 11 – AC TIMING of CLK & $\overline{CLK}$



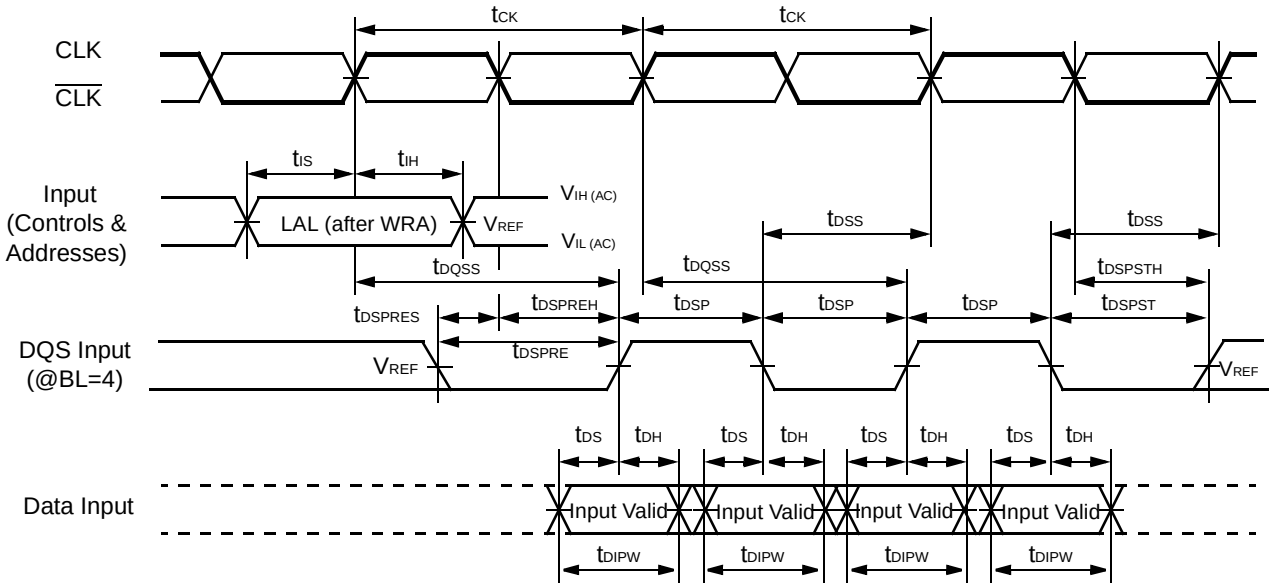
Note: Reference level for AC timings of clock are the cross point of CLK and $\overline{CLK}$ as specified in V_X.

Fig. 12 – AC TIMING of Command Input & Address



Note: The cross point of CLK and $\overline{CLK}$ (V_X) is used for command and address input.
The reference level of single ended input is V_{REF}.

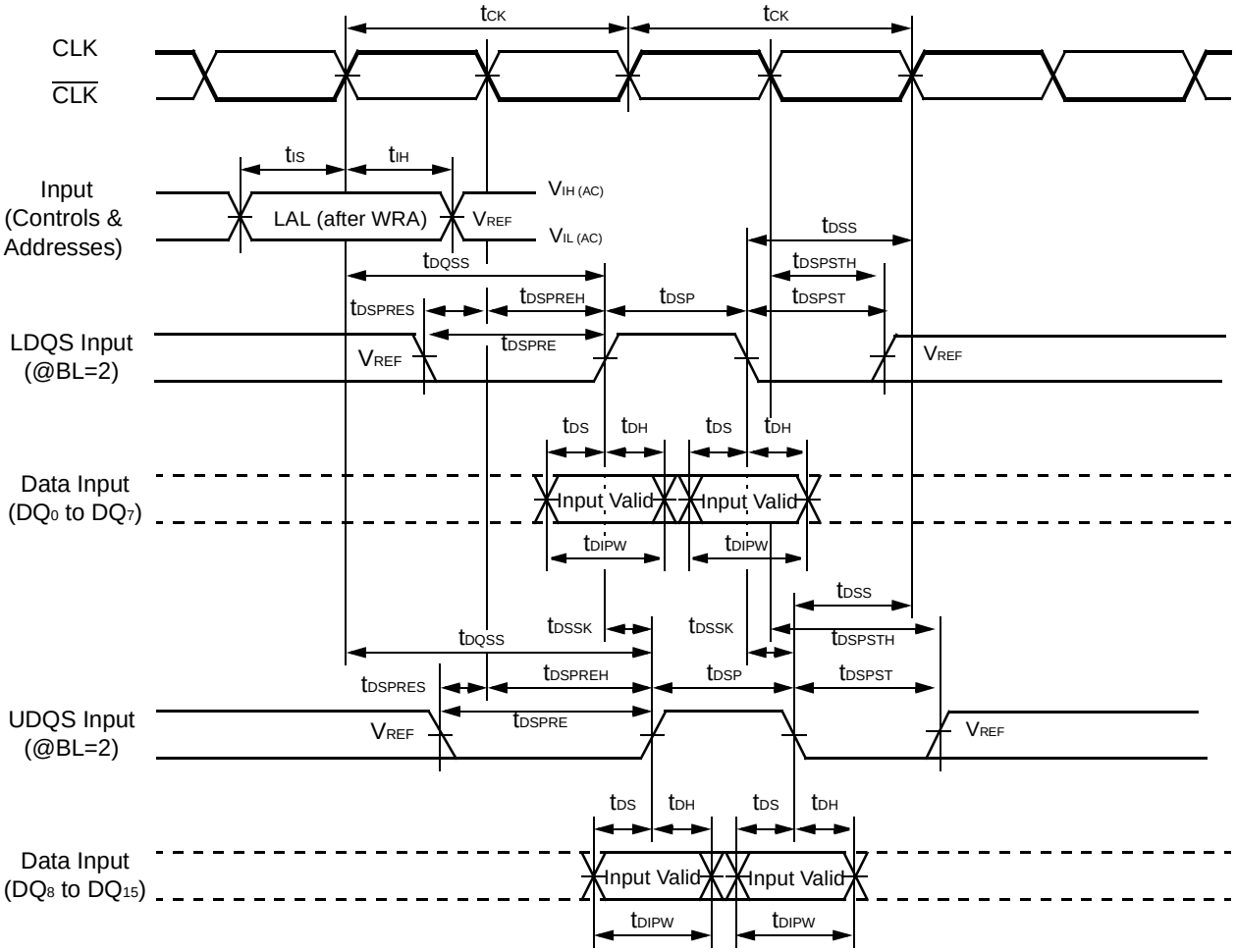
Fig. 13 – AC TIMING of Write Mode (Data Strobe and Write Data Input)



Note: The above timing on DQS and Data input assume CL=2 and BL=4.
The definition point of t_{DQSS}, t_{DSPRES} and t_{DSPREH} at CL=3 shift one clock later from above example.

■ AC CHARACTERISTICS (continued)

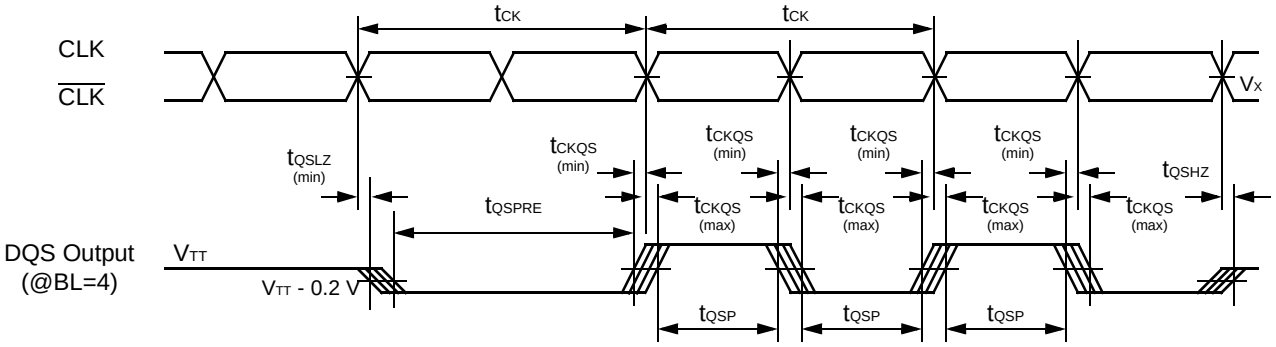
Fig. 14 – AC TIMING of Write Mode (Data Strobe and Write Data Input)



Note: The above timing on DQS and Data input assume CL=2 and BL=2.
The definition point of t_{DQSS}, t_{DSPRES} and t_{DSPREH} at CL=3 shift one clock later from above example.

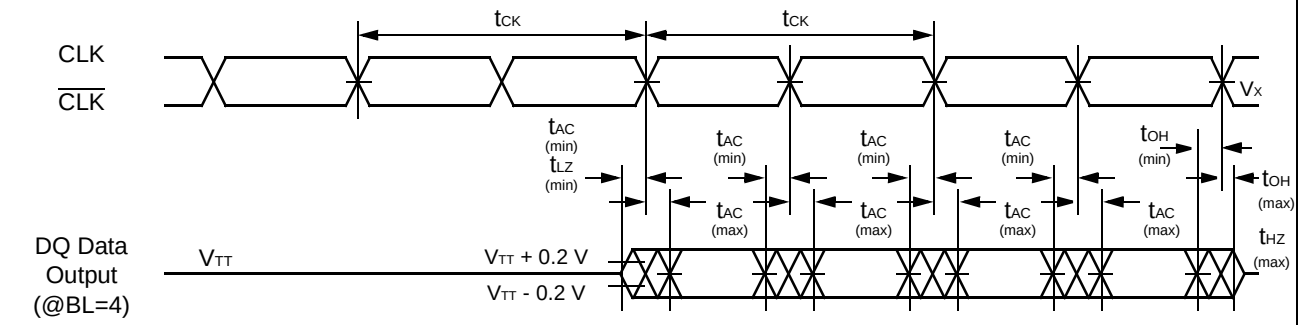
■ AC CHARACTERISTICS (continued)

Fig. 15 – AC TIMING of Read Mode (Clock to DQS Output Delay Time)



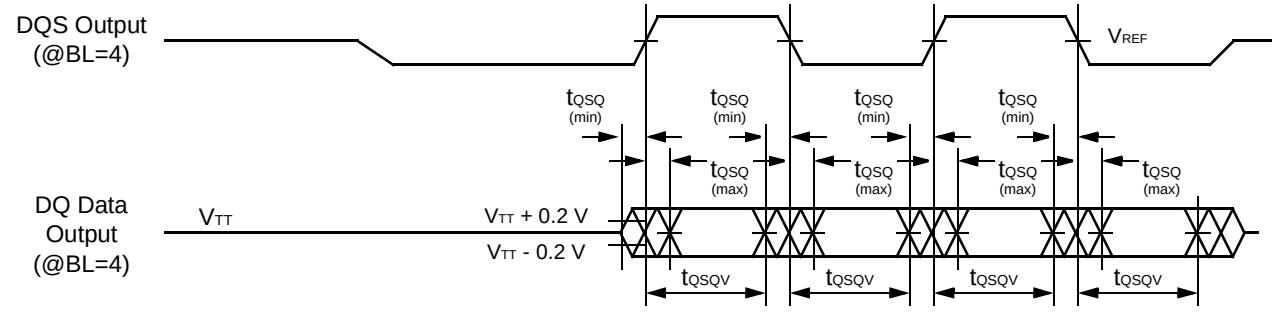
Note: DQS Access time (t_{QSCK}) is measured from the cross point of clock (V_X) and V_{REF}.
The t_{QSHZ} specification is defined at where output buffer is no longer driven.
The starting point of DQS in Low-Z (t_{QSHZ} specification) is CL-1.

Fig. 16 – AC TIMING of Read Mode (Clock to Data Output Delay Time)



Note: Access time (t_{AC}) is measured from the cross point of clock (V_X) and V_{REF}.
The t_{HZ} specification is defined at where output buffer is no longer driven.

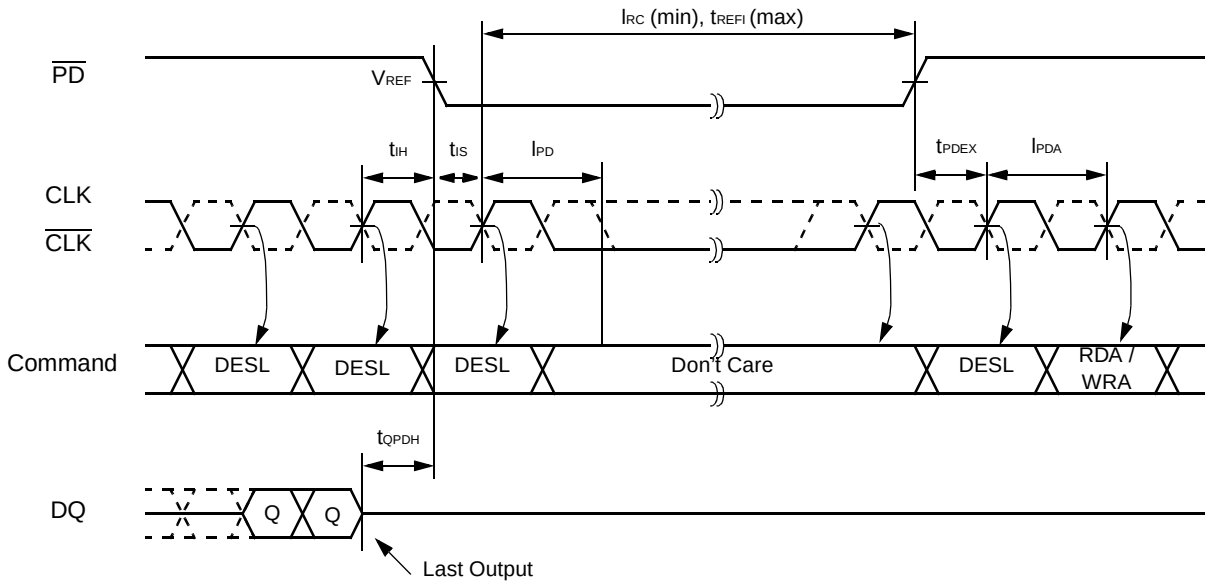
Fig. 17 – AC TIMING of Read Mode (DQS Output to Data Output Delay Time)



Note: DQS Output Edge to Data Output Edge Skew Time (t_{QSQ}) is measured from V_{REF} to V_{REF}.
Data Output Valid Time from DQS (t_{QSQV}) is specified from valid DQS transition crossing V_{REF} to end of data valid.

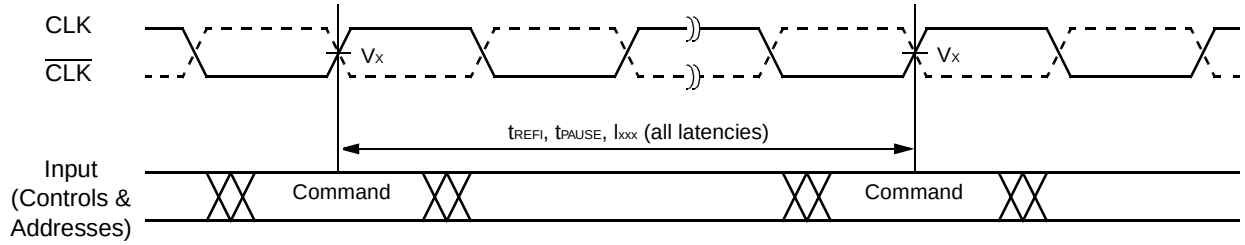
■ AC CHARACTERISTICS (continued)

Fig. 18 – AC TIMING of Power Down



Note: The above timing is for Power Down mode as a reference of $\overline{PD}$ input condition.
The setup and hold time of $\overline{PD}$ High to Low input must comply with t_{IS} and t_{IH} condition for both Power Down and Self-refresh entry.
When is brought to High from Low, t_{PDEX} is applied as a setup time against clock input.

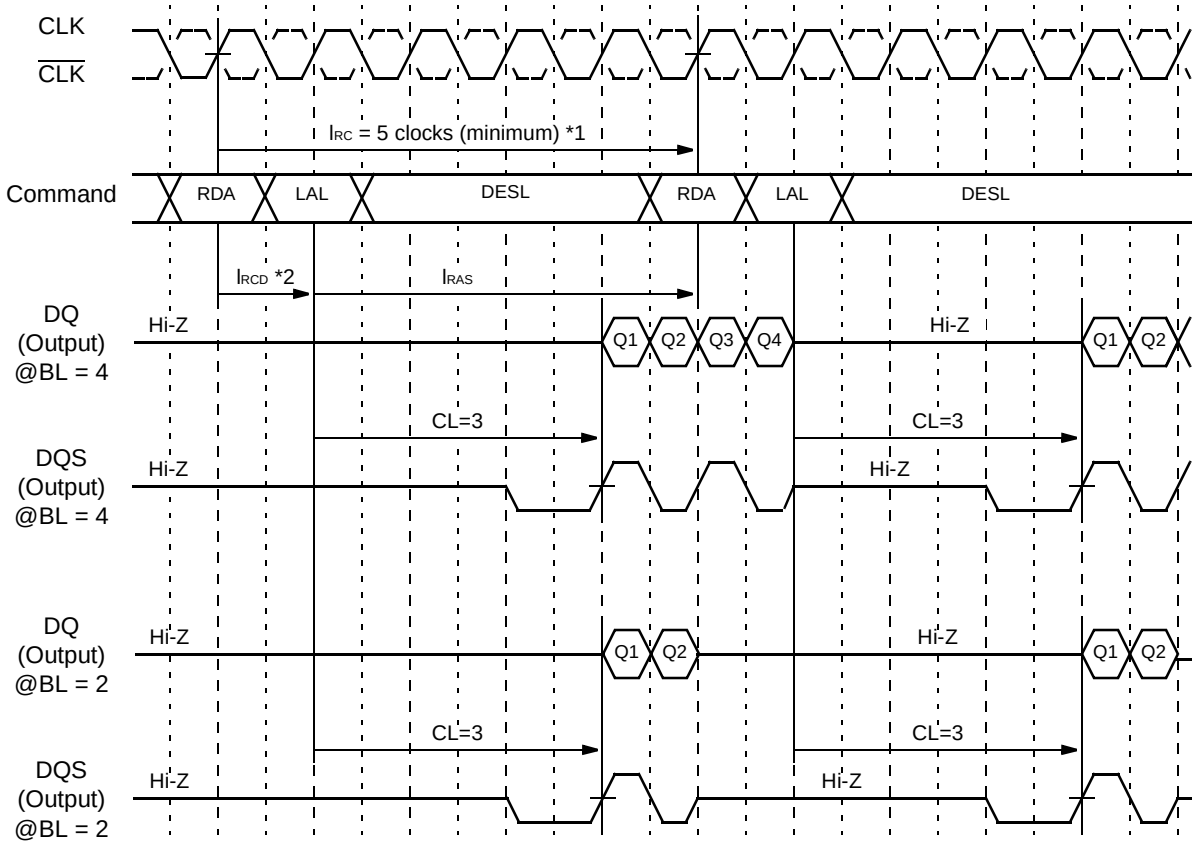
Fig. 19 – AC TIMING of Pulse Width and Latency



Note: All parameters listed above are measured from the cross point at rising edge of the CLK and falling edge of $\overline{CLK}$ of one command input to next command input.

■ TIMING DIAGRAMS

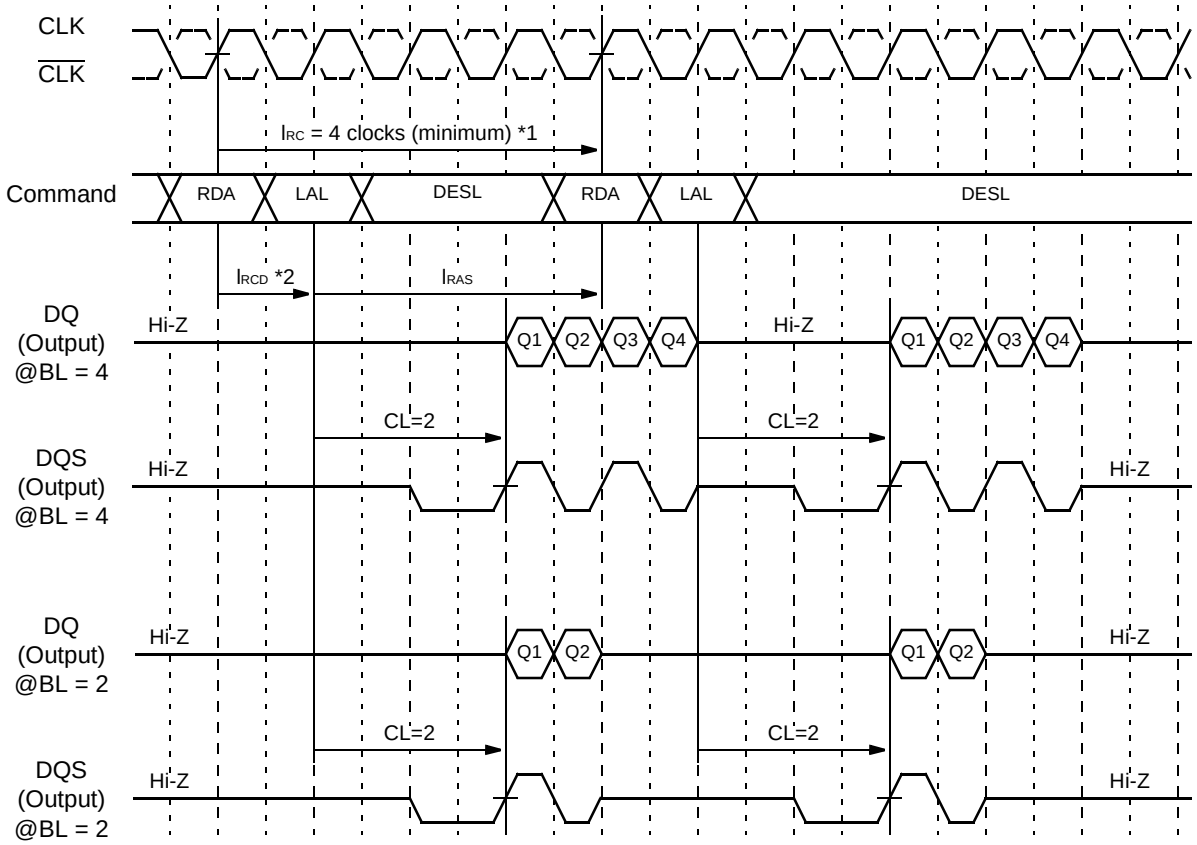
TIMING DIAGRAM – 1 : READ @ CL=3
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 5 clocks regardless of burst length when CL =3.
*2 The I_{RCD} must be 1 clock.

■ TIMING DIAGRAMS (Continued)

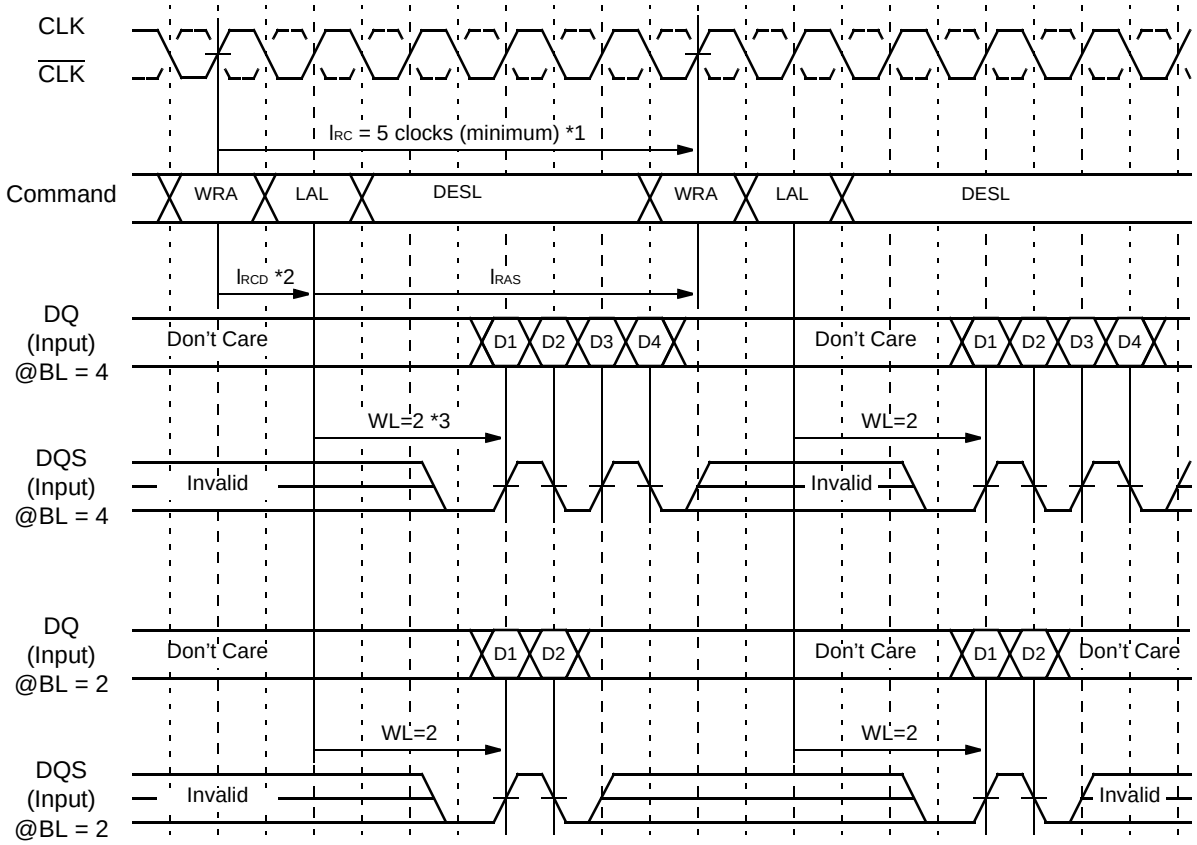
TIMING DIAGRAM – 2 : READ @ CL=2
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 4 clocks regardless of burst length when CL=2.
*2 The I_{RCD} must be 1 clock.

■ TIMING DIAGRAMS (Continued)

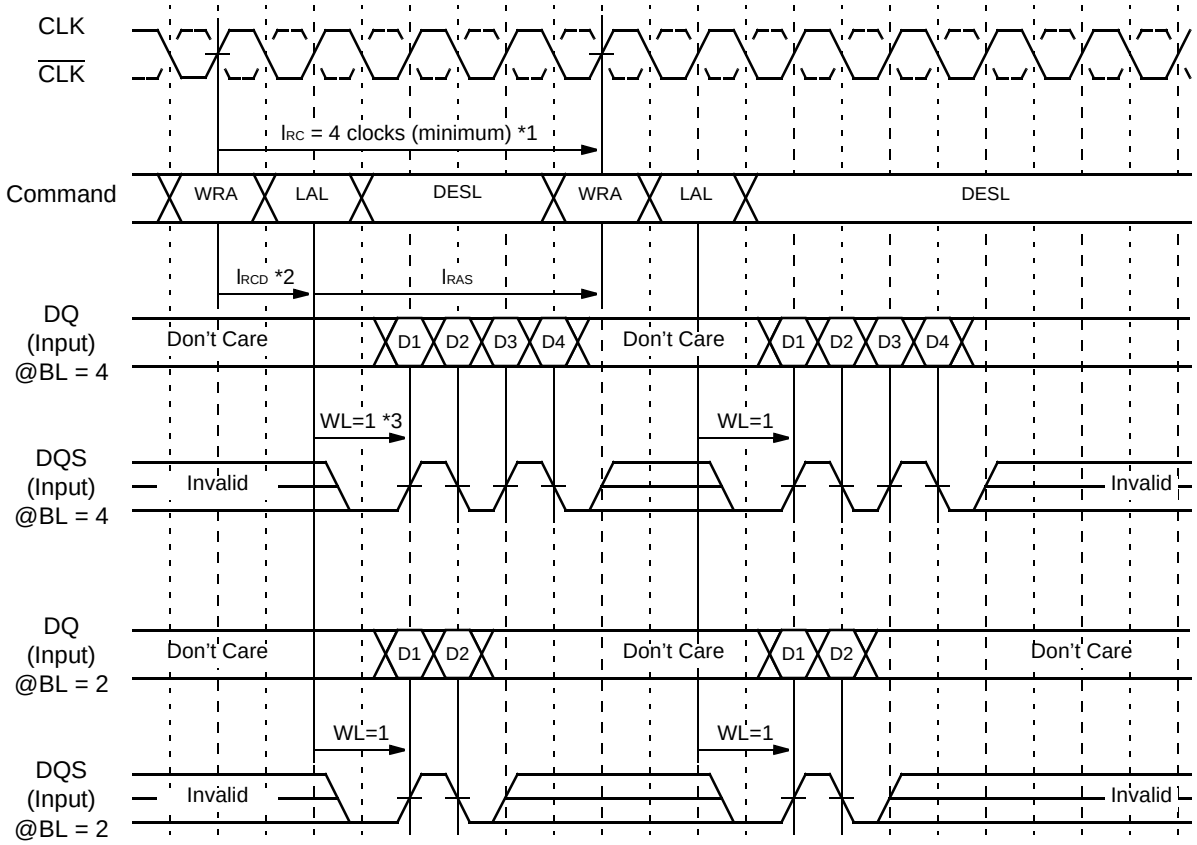
TIMING DIAGRAM – 3 : WRITE @ CL=3
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 5 clocks regardless of burst length when CL=3.
*2 The I_{RCD} must be 1 clock.
*3 The Write Data Latency (WL) is 2 clocks typical when CL=3.

■ TIMING DIAGRAMS (Continued)

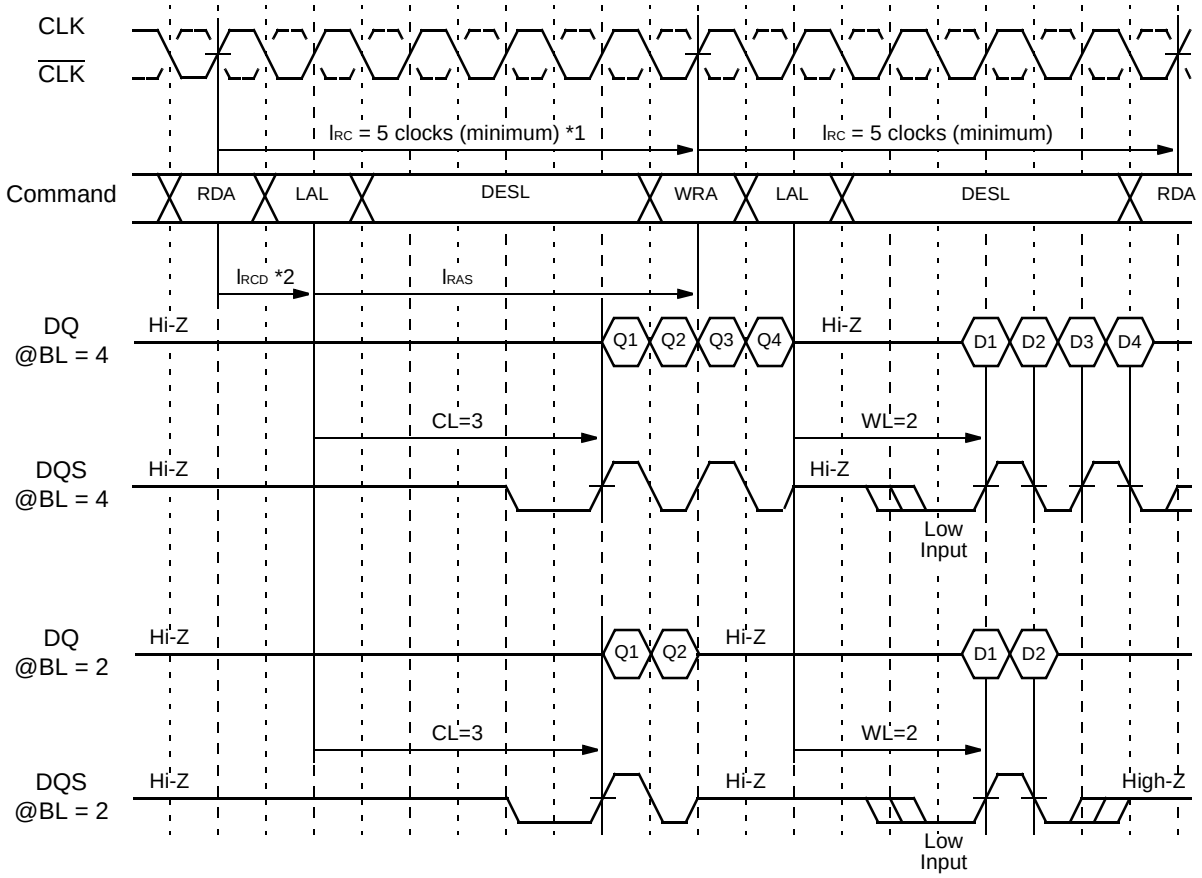
TIMING DIAGRAM – 4 : WRITE @ CL=2
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 4 clocks regardless of burst length when CL=2.
*2 The I_{RCD} must be 1 clock.
*3 The Write Data Latency (WL) is 1 clock typical when CL=2.

■ TIMING DIAGRAMS (Continued)

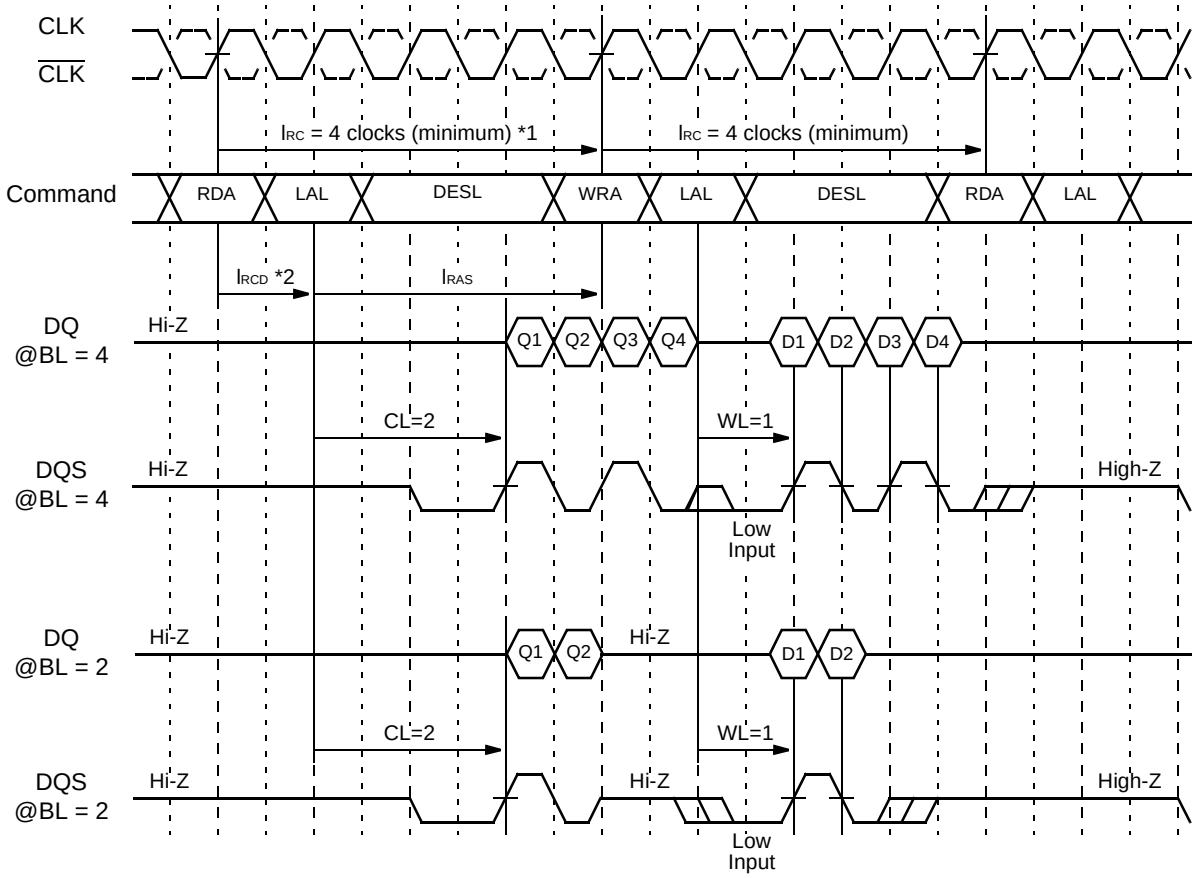
TIMING DIAGRAM – 5 : READ and WRITE @ CL=3
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 5 clocks regardless of burst length when CL =3.
*2 The I_{RCD} must be 1 clock.

■ TIMING DIAGRAMS (Continued)

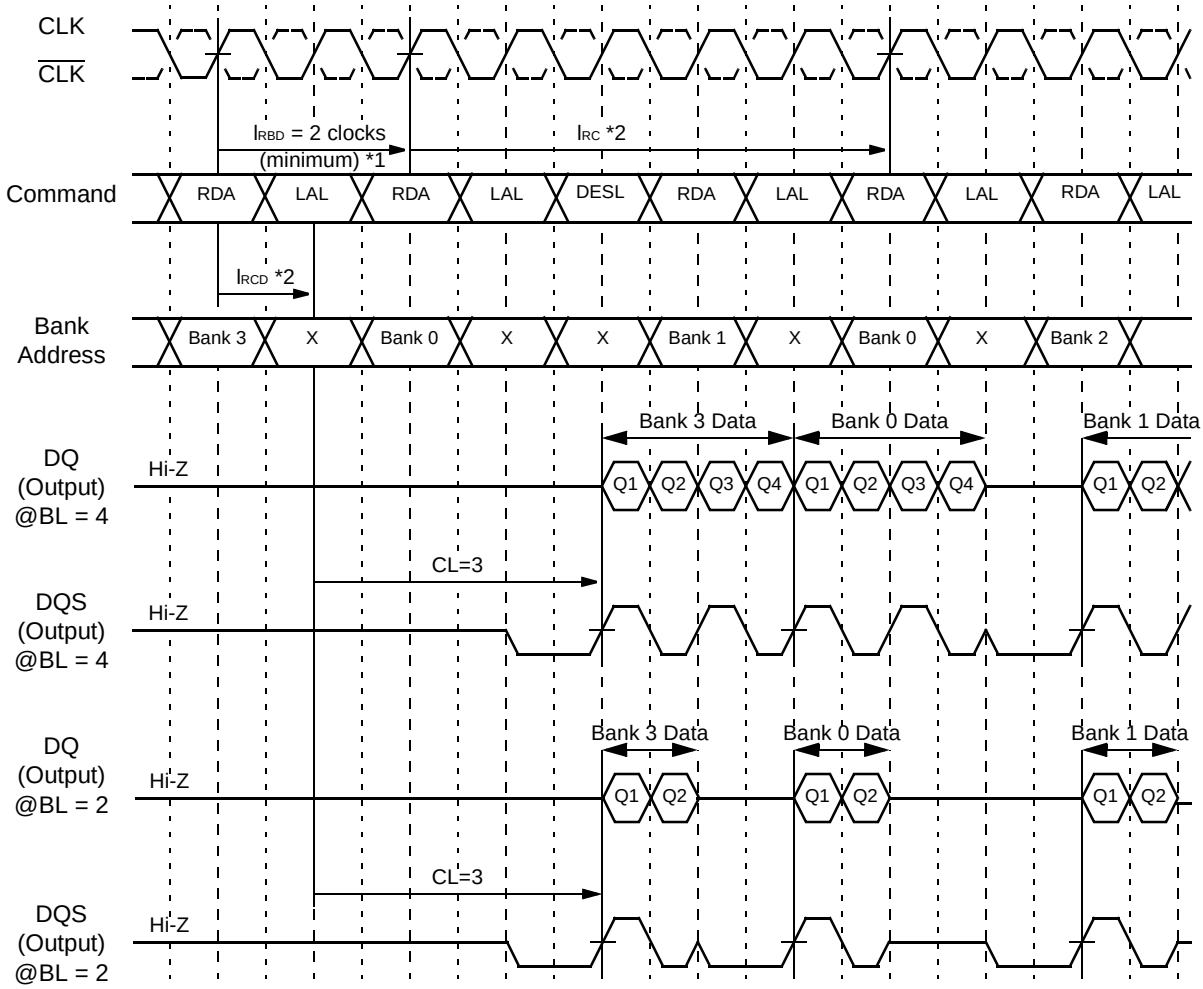
TIMING DIAGRAM – 6 : READ and WRITE @ CL=2
(Single Bank Access)



Notes: *1 The random cycle time I_{RC} is 4 clocks regardless of burst length when CL=2.
*2 The I_{RCD} must be 1 clock.

■ TIMING DIAGRAMS (Continued)

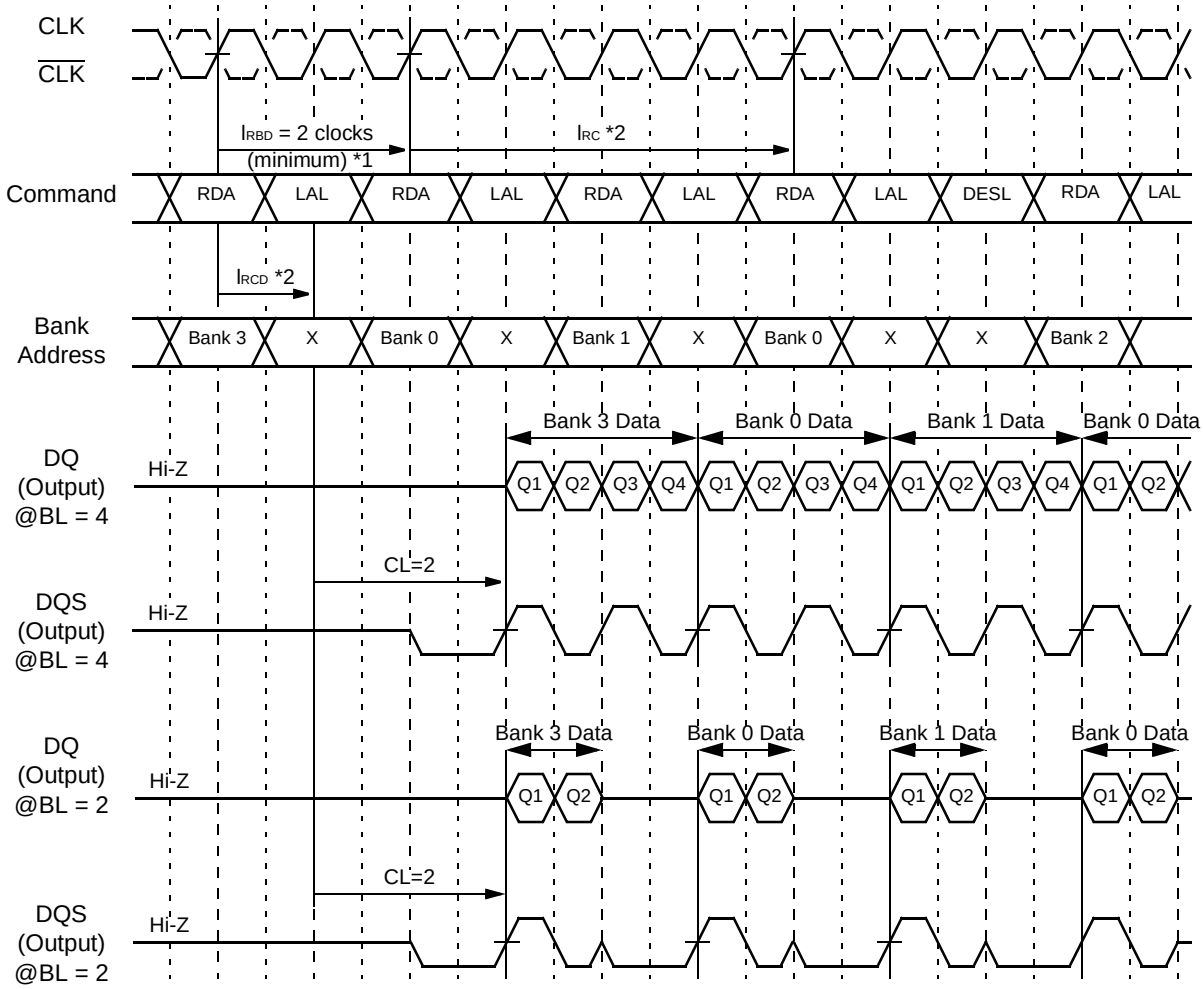
TIMING DIAGRAM – 7 : READ @ CL=3
(Multiple Bank Access)



Notes: *1 The random bank access delay t_{RBD} is 2 clocks minimum.
*2 Both t_{RC} and t_{RCD} must be satisfied for the same bank.

■ TIMING DIAGRAMS (Continued)

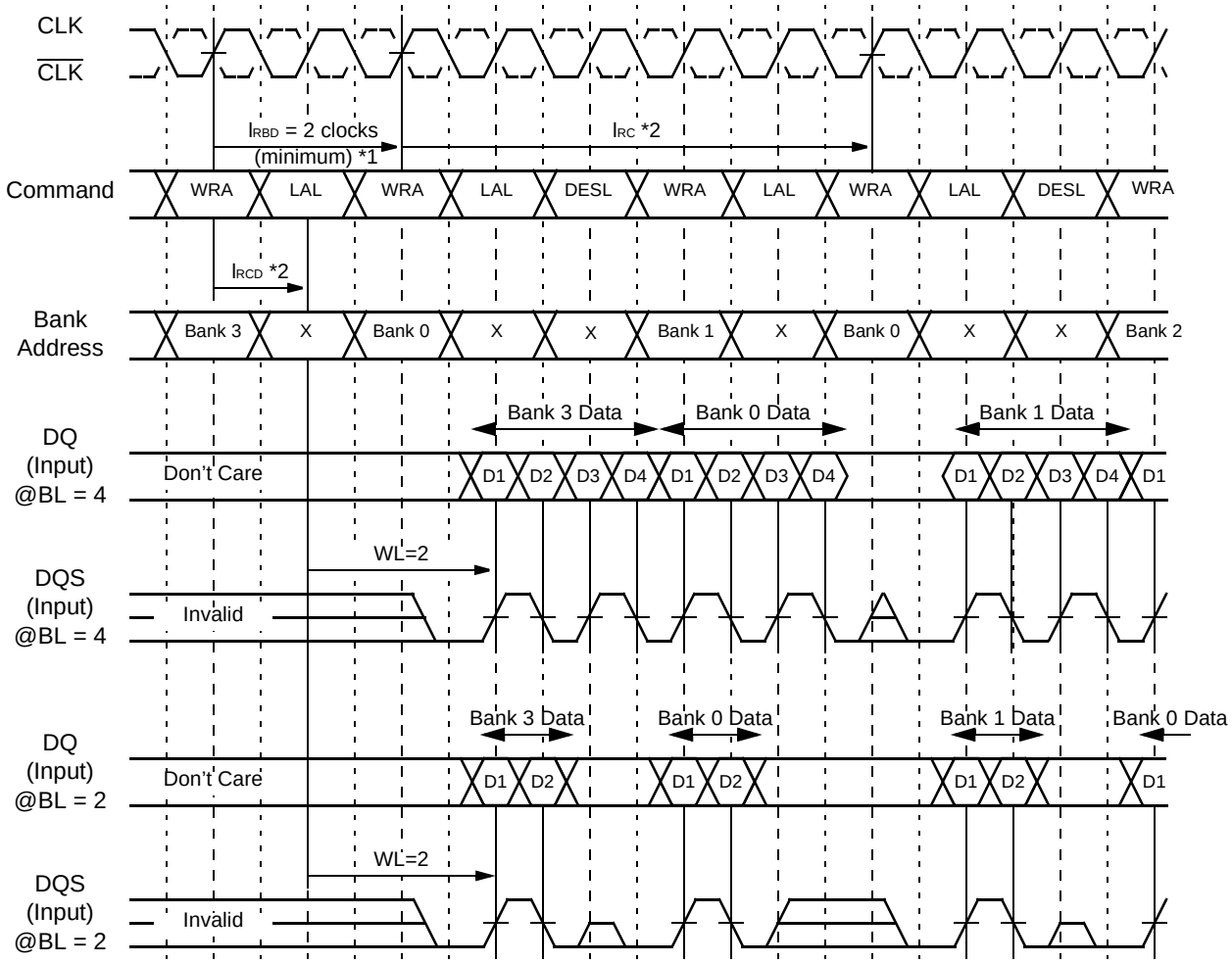
TIMING DIAGRAM – 8 : READ @ CL=2
(Multiple Bank Access)



Notes: *1 The random bank access delay I_{RBD} is 2 clocks minimum.
*2 Both I_{RC} and I_{RCD} must be satisfied for the same bank.

■ TIMING DIAGRAMS (Continued)

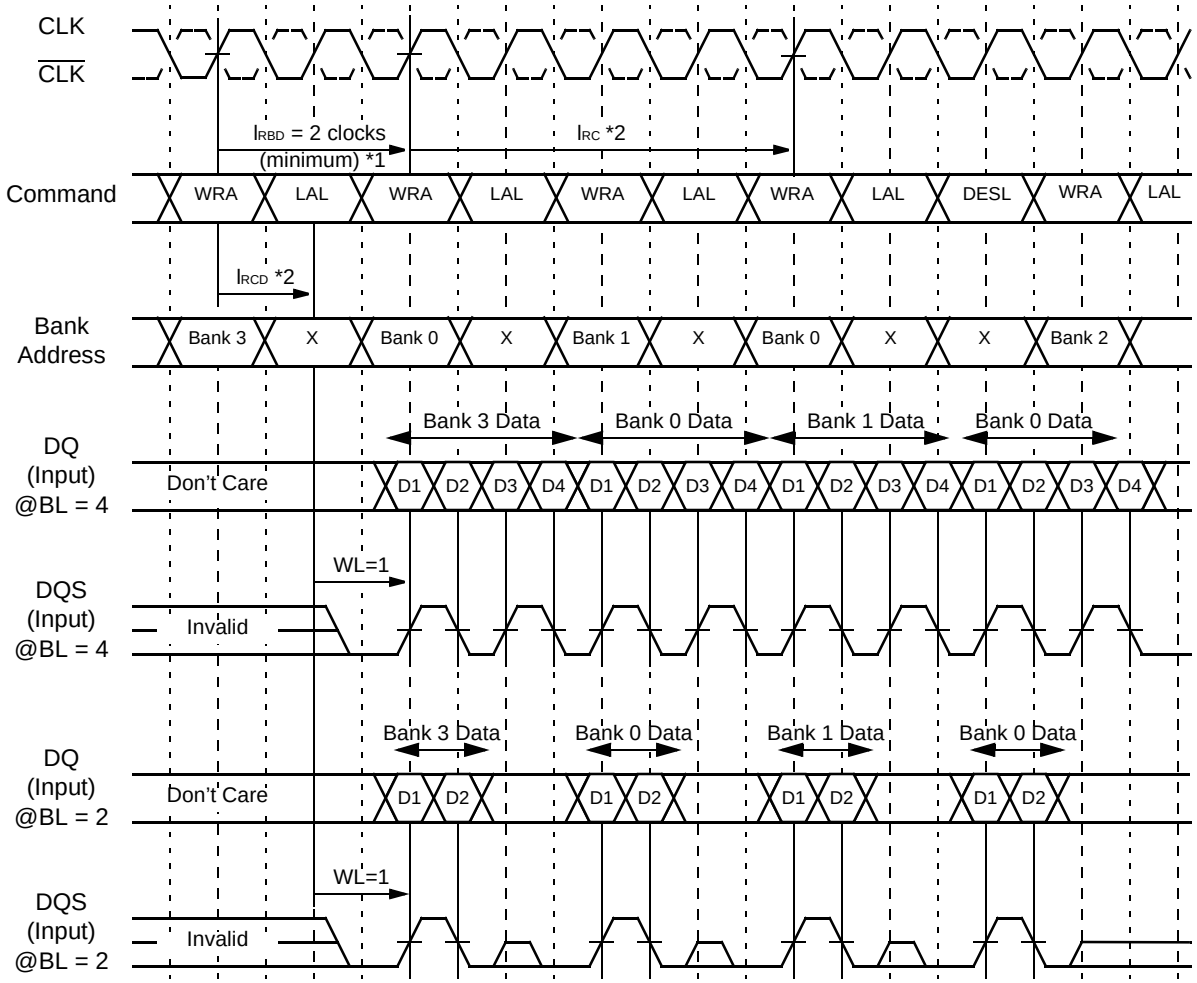
TIMING DIAGRAM – 9 : WRITE @ CL=3
(Multiple Bank Access)



Notes: *1 The random bank access delay I_{RBD} is 2 clocks minimum.
*2 Both I_{RC} and I_{RCD} must be satisfied for the same bank.

■ TIMING DIAGRAMS (Continued)

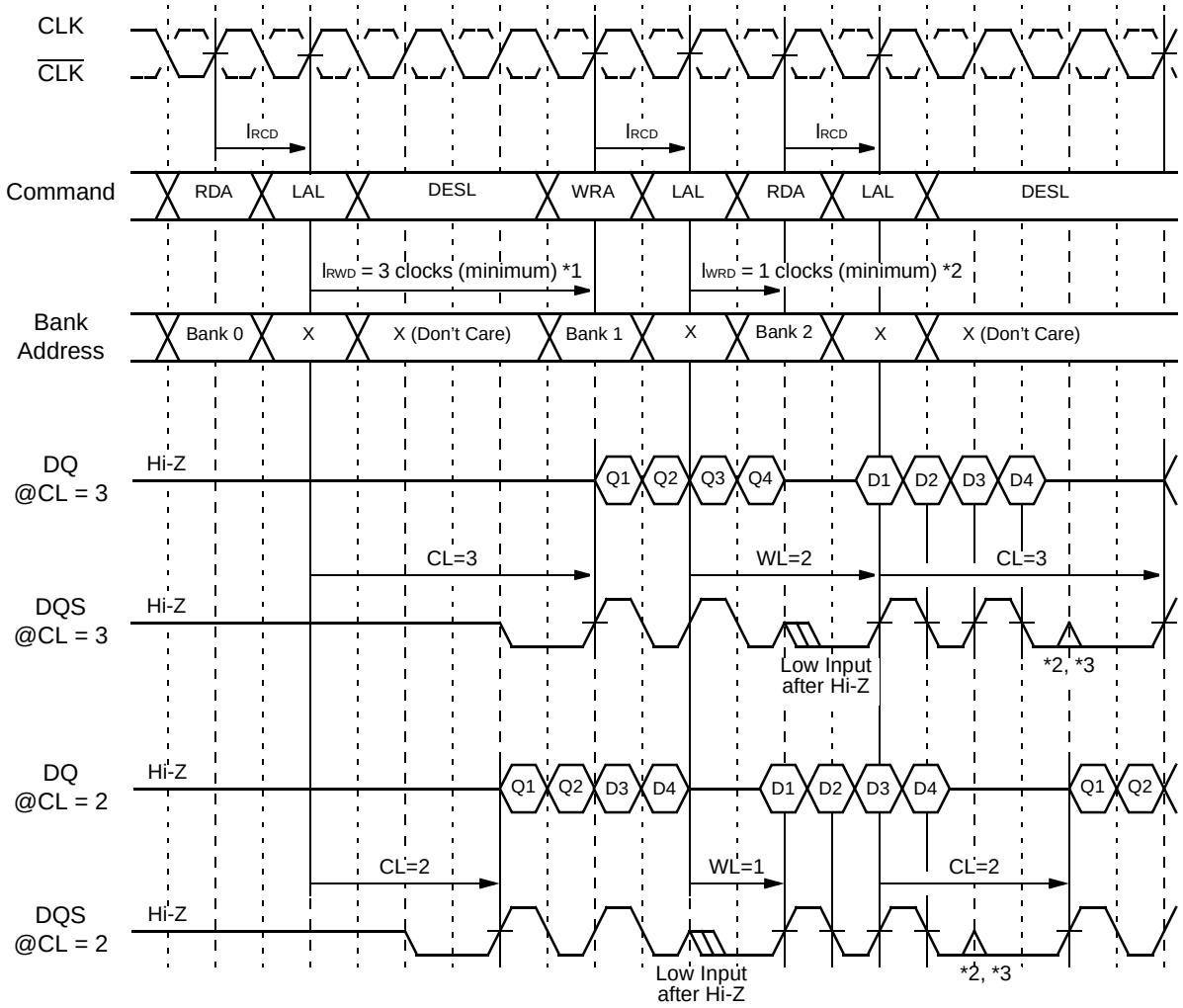
TIMING DIAGRAM – 10 : WRITE @ CL=2
(Multiple Bank Access)



Notes: *1 The random bank access delay t_{RBD} is 2 clocks minimum.
*2 Both t_{RC} and t_{RCD} must be satisfied for the same bank.

■ TIMING DIAGRAMS (Continued)

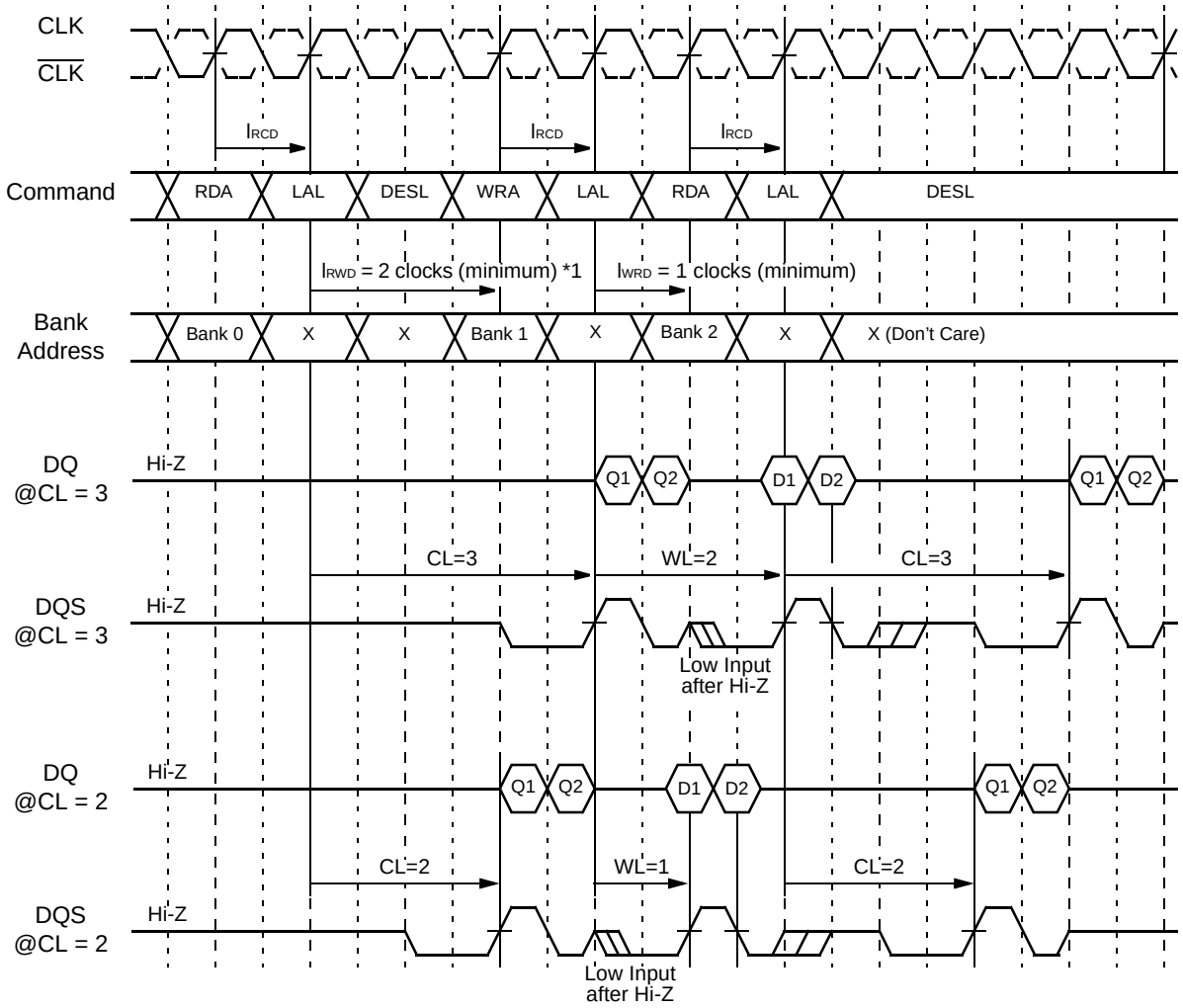
TIMING DIAGRAM – 11 : READ and WRITE @ BL=4
(Multiple Bank Access)



Notes: *1 The read to write delay for different bank, l_{RWD} is 3 clocks minimum at BL=4 regardless of CL.
*2 The l_{WRD} can be 1 clock if maximum t_{DSPST} can be met.
*3 Low to Low input and output conflict is allowed if maximum t_{DSPST} can be met.

■ TIMING DIAGRAMS (Continued)

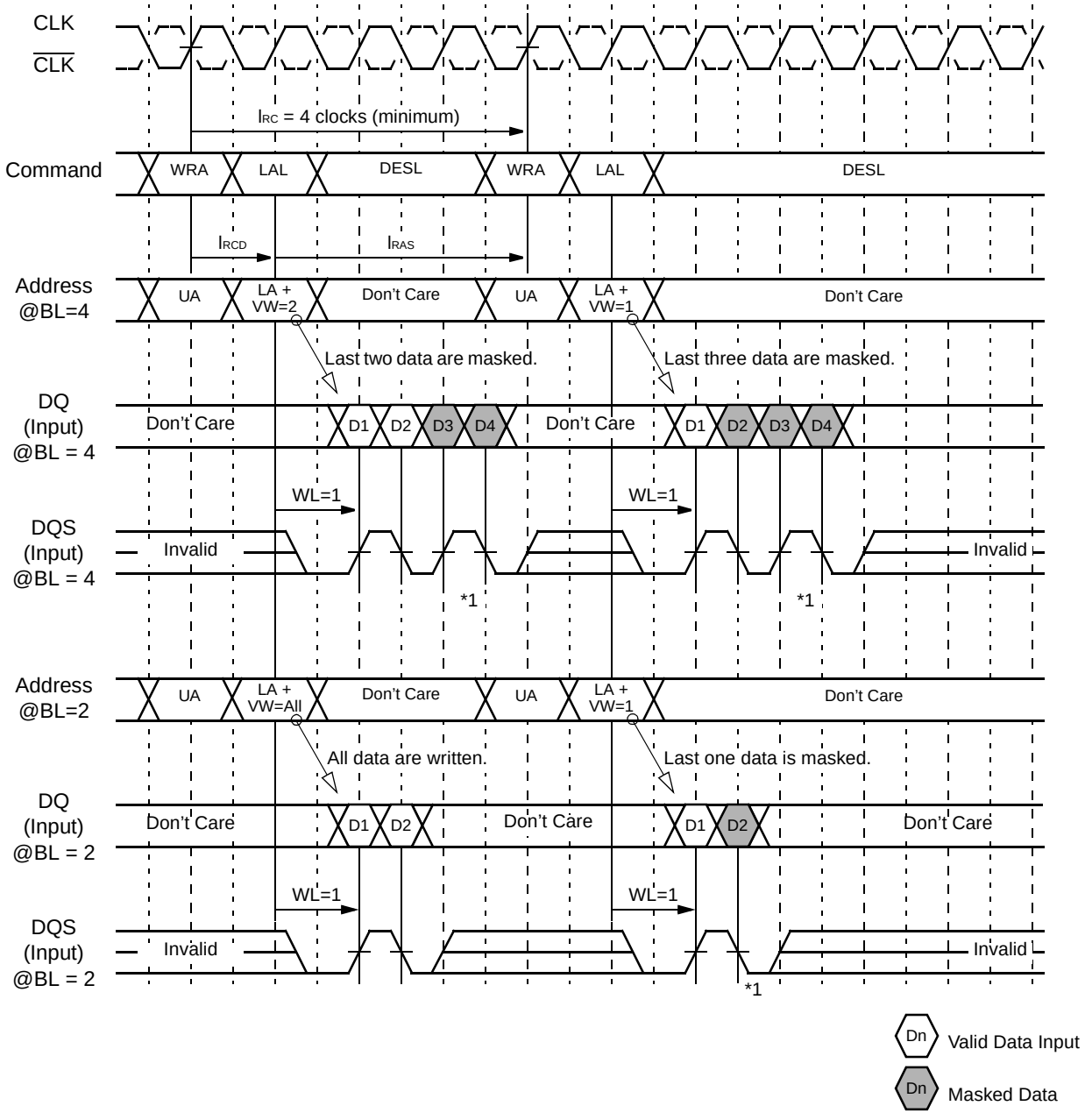
TIMING DIAGRAM – 12 : READ and WRITE @ BL=2
(Multiple Bank Access)



Notes: *1 The read to write delay for different bank, I_{RWD} is 2 clocks minimum at BL=2 regardless of CL.

■ TIMING DIAGRAMS (Continued)

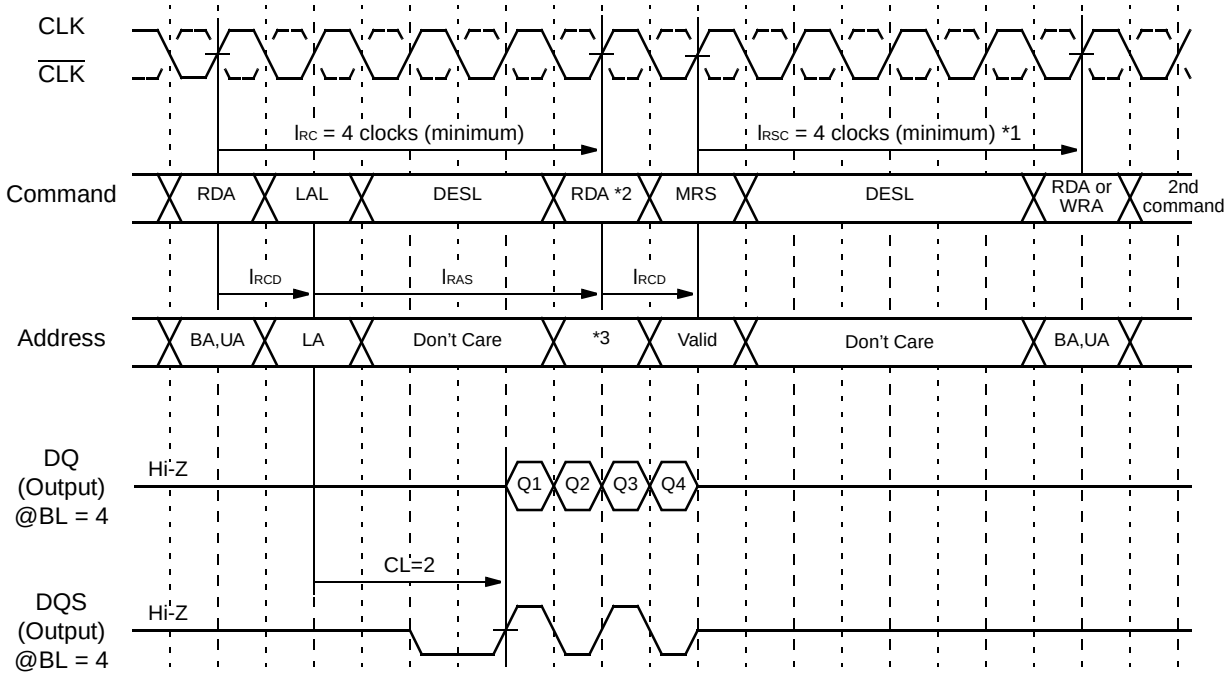
TIMING DIAGRAM – 13 : WRITE with VW
(Example at Single Bank Access with CL=2)



Notes: *1 DQS Input must be continued till end of burst count even if some of later data is masked.

■ TIMING DIAGRAMS (Continued)

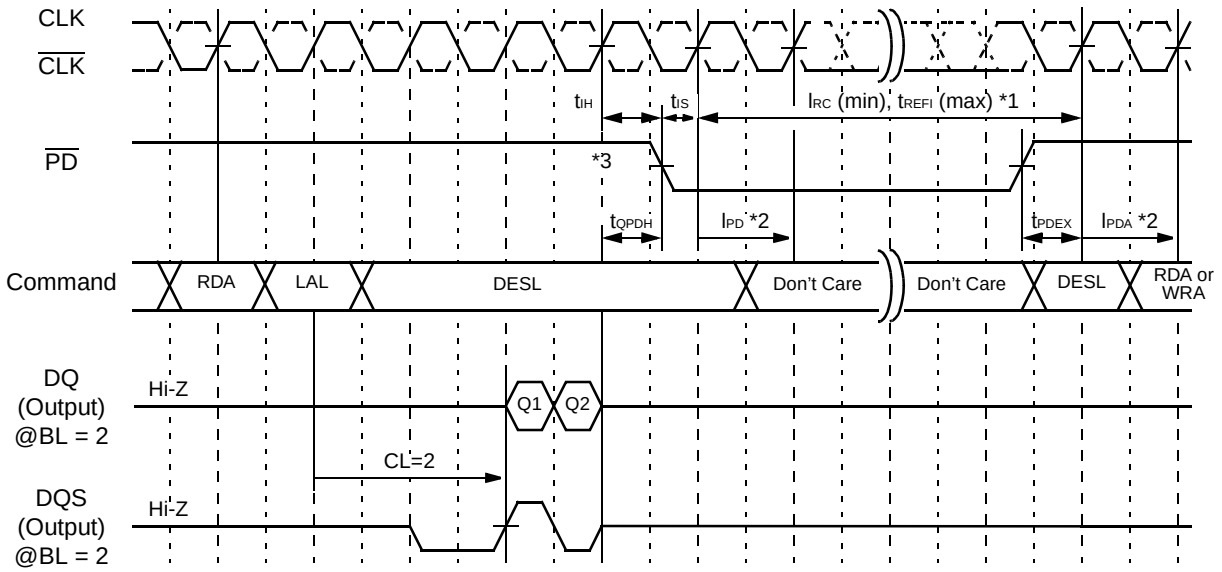
TIMING DIAGRAM – 14 : MODE REGISTER SET
(Example at BL=4 with CL=2)



Notes: *1 The minimum mode register set cycle time I_{RSC} is the same as minimum I_{RC}.
Read command (RDA+LAL) should be asserted after I_{LOCK} at the initialization sequence.
*2 All banks must be in idle state or I_{RC} of last open bank must be satisfied.
*3 The address information will be ignored when MRS command is asserted at next cycle.

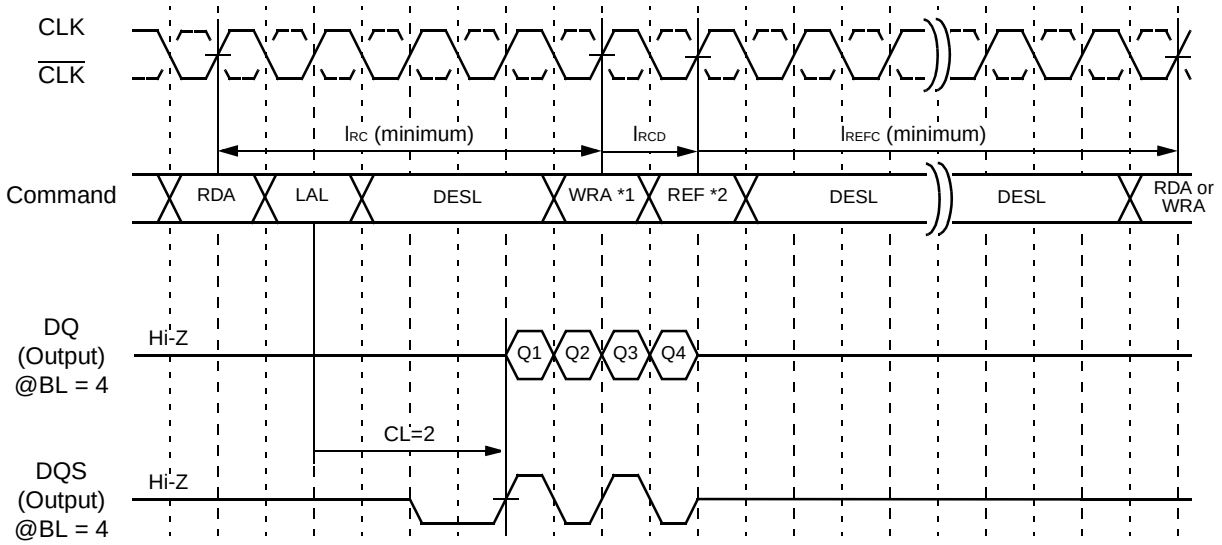
■ TIMING DIAGRAMS (Continued)

TIMING DIAGRAM – 15 : POWER DOWN
(Example at BL=2 with CL=2)



Notes: *1 $\overline{PD}$ should be brought to High within t_{REFI} (max) to maintain the data written into cell.
*2 The $\overline{PD}$ to input enable/disable latency is 1 clock.
*3 All banks must be in idle state and t_{QPDH} from last read data output must be satisfied.

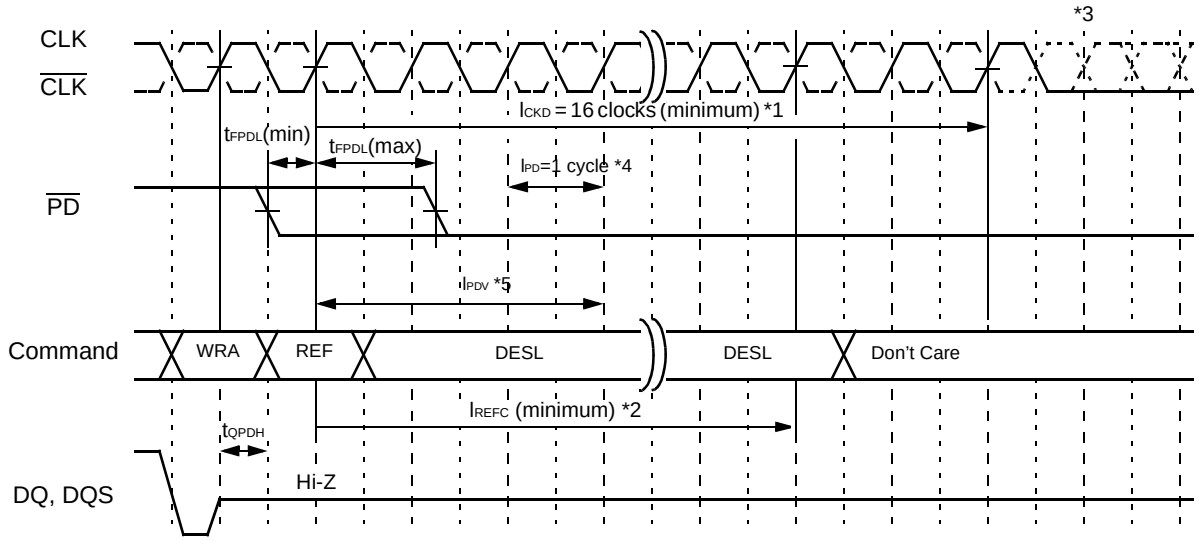
TIMING DIAGRAM – 16 : AUTO-REFRESH
(Example at BL=4 with CL=2)



Notes: *1 All banks must be in idle state or I_{RC} of last open bank must be satisfied.
*2 The write operation will be cancelled when REF command is asserted.

■ TIMING DIAGRAMS (Continued)

TIMING DIAGRAM – 17 : SELF-REFRESH ENTRY
(Example at CL=2)



Notes: *1 Clock input should be continued at least 16 clocks from REF command even though $\overline{PD}$ is brought to Low for Self-refresh entry.

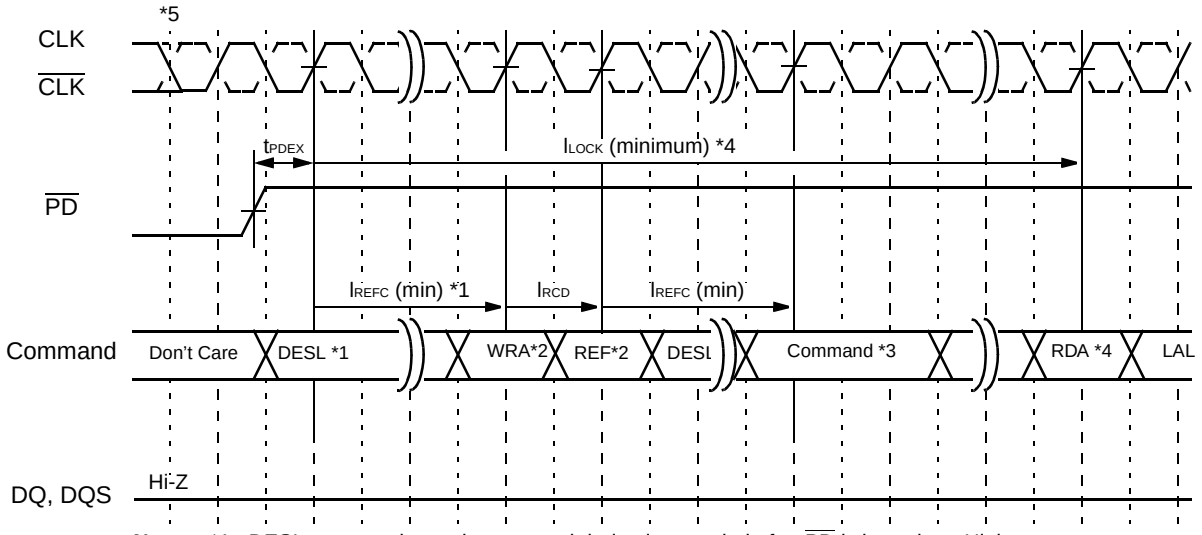
*2 DESL command must be asserted during t_{REFC} period.

*3 Clock can be disabled after t_{CKD} period from REF command when $\overline{PD}$ is brought to Low for Self-refresh.

*4 t_{PD} is defined from the first clock rising edge after $\overline{PD}$ is brought to Low.

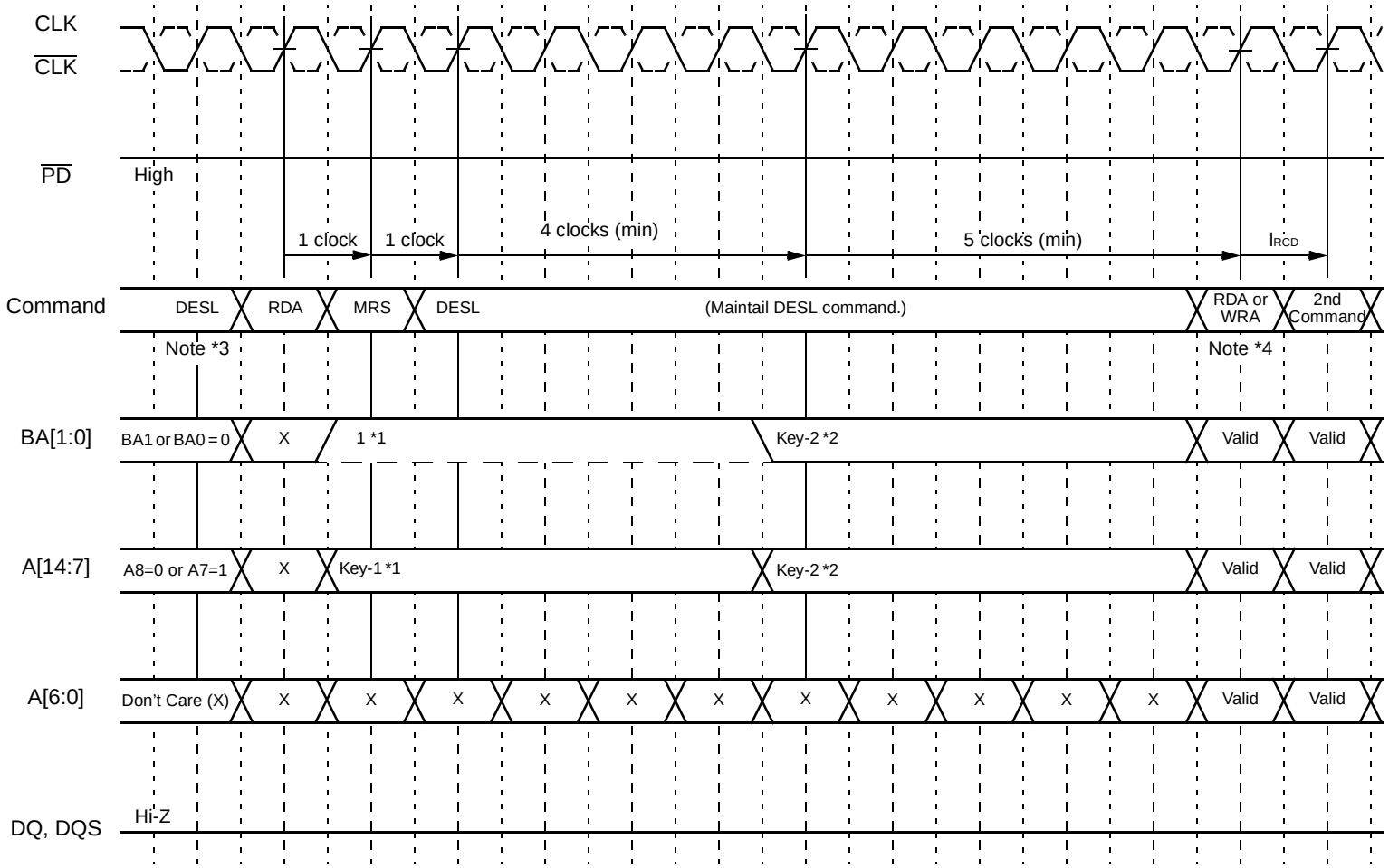
*5 $\overline{PD}$ must be brought to Low within the timing between t_{FPDL} (min) and t_{FPDL} (max) to Self-refresh mode. When $\overline{PD}$ is brought to Low after t_{PDV}, FCRAM perform Auto-refresh and enter Power Down mode.

TIMING DIAGRAM — 18 : SELF-REFRESH EXIT



Notes: *1 DESL command must be asserted during l_{REFC} period after $\overline{PD}$ is brought to High.
*2 One REF command should be asserted just after Self-refresh exit before any other operation.
*3 Any command other than read command can be issued after Auto-refresh period.
*4 Read command (RDA + LAL) can be issued after l_{LOCK} period.
*5 Clock should be stable prior to $\overline{PD}$ = High if clock input is suspended during Self-refresh.

TIMING DIAGRAM — 19 : POWER-UP INITIALIZATION and RESET

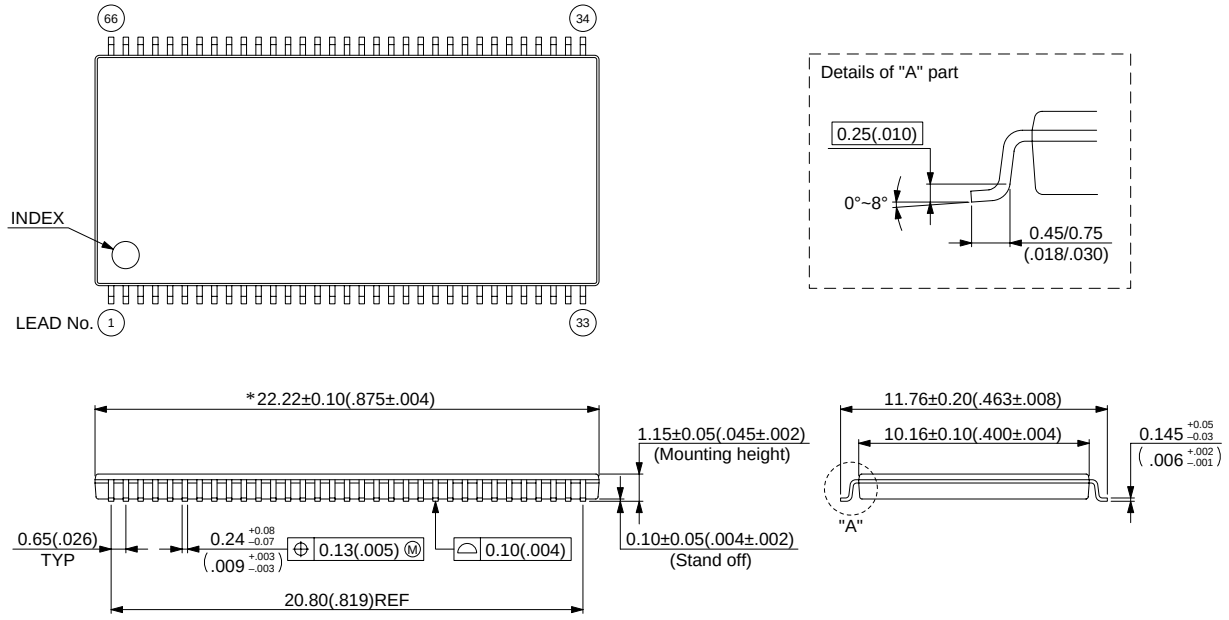


Notes: *1 BA[1:0] and A[14:8] must be High (1) and A7 must be Low (0), and those value must be maintained for 4 clocks.
*2 At least one address must be flipped and maintained at least 5 clocks.
*3 DESL condition must be maintained for 12 clocks when RESET is being performed.
*4 Ready for normal operation after RESET or start MRS programming and Auto-refresh at Power-up Initialization.

■ PACKAGE DIMENSIONS (TENTATIVE)

66-pin plastic TSOP (II)
(FPT-66P-M01)

*: Resin protrusion. (Each side: 0.15 (.006) MAX)



Dimensions in mm (inches)

MEMO

MEMO

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