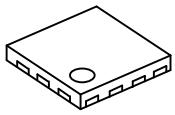
HIGH ISOLATION SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1666MD7 is a GaAs SPDT switch designed for Set-top boxes, TV tuners, CATV tuners, and sub-microwave applications. The NJG1666MD7 features high isolation, low insertion loss and covering a broad frequency range up to 3GHz. The NJG1666MD7operates single bit control switching by control voltage from 1.3V to 4.5V, and includes ESD protection circuits for good ESD tolerance. The NJG1666MD7 is available in a very small, lead-free, halogen-free, 1.6mm x 1.6mm x 0.397 mm, 14-pin EQFN14-D7 package.

■ PACKAGE OUTLINE



NJG1666MD7

■ APPLICATIONS

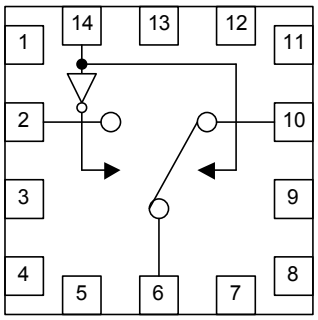
Terrestrial and Satellite applications
Set-top box, TV tuner, CATV tuner, Digital TV and Cable TV applications

■ FEATURES

● Low operating voltage	V_{DD} =+2.0~+4.5V	
● Low control voltage	$V_{CTL(H)}$=+1.3V min	
● Low current consumption	30μA typ.	
● High isolation	70dB typ.	@f=0.25GHz
	60dB typ.	@f=1.0GHz
	60dB typ.	@f=2.2GHz
● Low insertion loss	0.40dB typ.	@f=0.25GHz
	0.45dB typ.	@f=1.0GHz
	0.50dB typ.	@f=2.2GHz
● High ESD tolerance	On-chip ESD protection circuit	
● Ultra- small and ultra-thin package	EQFN14-D7 (package size: 1.6mm x 1.6mm x 0.397mm typ.)	
● Lead and halogen-free		

■ PIN CONFIGURATION

(Top view)



Pin Connection

1.	NC(GND)	8.	NC(GND)
2.	P2	9.	GND
3.	GND	10.	P1
4.	NC(GND)	11.	NC(GND)
5.	GND	12.	VDD
6.	PC	13.	GND
7.	GND	14.	CTL

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

CTL	PATH
H	PC-P1
L	PC-P2

NOTE: The information on this datasheet is subject to change without notice

■ ABSOLUTE MAXIMUM RATINGS

(T_a=25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input power	P_{IN}	V_{DD}=3.0V	28	dBm
Supply voltage	V_{DD}	VDD terminal	5.0	V
Control voltage	V_{CTL}	CTL terminal	5.0	V
Power dissipation	P_D	Four-layer FR4 PCB with through-hole (74.2mmx74.2mm), T_j=150°C	1300	mW
Operating temp.	T_{opr}		-40~+85	°C
Storage temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: V_{DD}=3.0V, $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3.0V, Z_s=Z_l=50Ω, T_a=+25°C, with application circuit)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}		2.0	3.0	4.5	V
Operating current	I_{DD}		-	30	60	μA
Control voltage (L)	$V_{CTL(L)}$		0	-	0.4	V
Control voltage (H)	$V_{CTL(H)}$		1.3	3.0	4.5	V
Control current	I_{CTL}		-	15	30	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: V_{DD}=3.0V, $V_{CTL\ (L)}$=0V, $V_{CTL\ (H)}$=3.0V, Z_s=Z_l=50Ω, T_a=+25°C, with application circuit)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 1	LOSS1	f=250MHz, P_{IN}=0dBm	-	0.40	0.60	dB
Insertion loss 2	LOSS2	f=1000MHz, P_{IN}=0dBm	-	0.45	0.65	dB
Insertion loss 3	LOSS3	f=2200MHz, P_{IN}=0dBm	-	0.50	0.70	dB
Isolation 1	ISL1	f=250MHz, P_{IN}=0dBm	65	70	-	dB
Isolation 2	ISL2	f=1000MHz, P_{IN}=0dBm	55	60	-	dB
Isolation 3	ISL3	f=2200MHz, P_{IN}=0dBm	55	60	-	dB
Input power at 1dB compression point	P_{-1dB}	f=2200MHz	23	27	-	dBm
VSWR	VSWR	f=2200MHz, ON state	-	1.3	1.5	
Switching time	T_{SW}	50% V_{CTL} to 10%/90% RF	-	1	5	μs

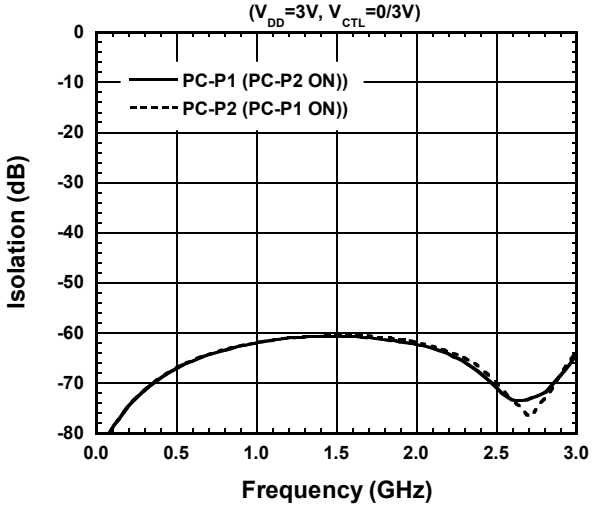
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
2	P2	This port is connected to PC port by applying the control voltage 0~+0.4 V($V_{CTL(L)}$) to 14th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
6	PC	Common RF port. This PC port is connected to P1 or P2 by logical control voltage of 14th pin. In order to block DC bias voltage of internal circuit, an external capacitor is required.
10	P1	This port is connected to PC port by applying control voltage of +1.3~+4.5 V ($V_{CTL(H)}$) to 14th pin. An external capacitor is required to block the DC bias voltage of internal circuit.
12	VDD	A supply voltage terminal (+2.0~+4.5 V). Place a bypass capacitor between this terminal and ground plane for avoiding RF noise from outside.
14	CTL	Control signal input terminal. This terminal is set to High-Level (+1.3~+4.5 V) or Low-Level (0~+0.4 V).
1,4,8,11	NC (GND)	No connected terminal. This terminal is not connected with internal circuit. Connect to the PCB ground plane.
3,5,7, 9,13	GND	Ground terminal. Connect this terminal with ground plane as close as possible for excellent RF performance.

■ **ELECTRICAL CHARACTERISTICS** ((With Application circuit, Loss of external circuit are excluded)

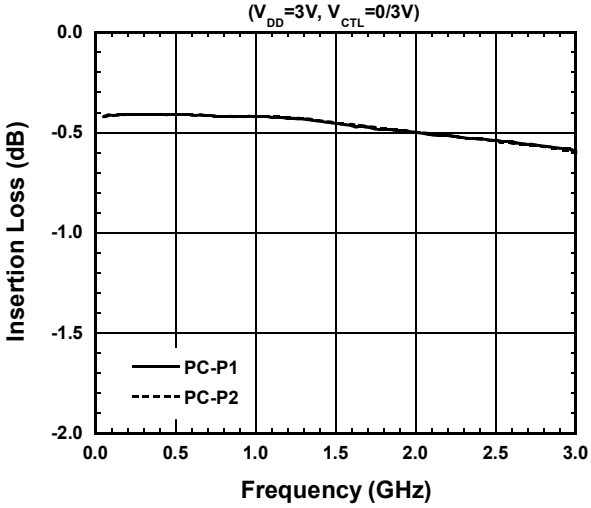
Isolation vs. Frequency

(V_{DD}=3V, V_{CTL}=0/3V)



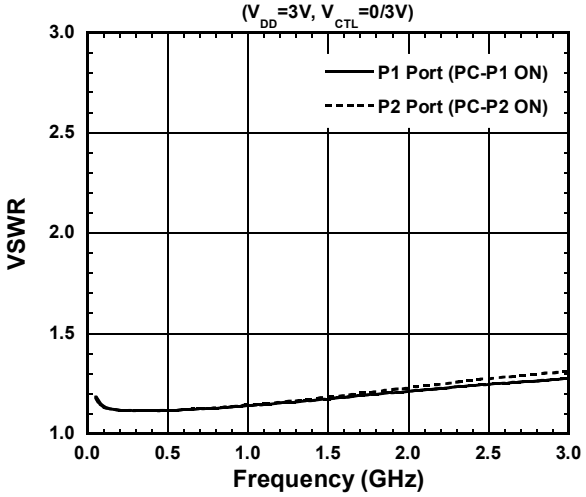
Insertion Loss vs. Frequency

(V_{DD}=3V, V_{CTL}=0/3V)



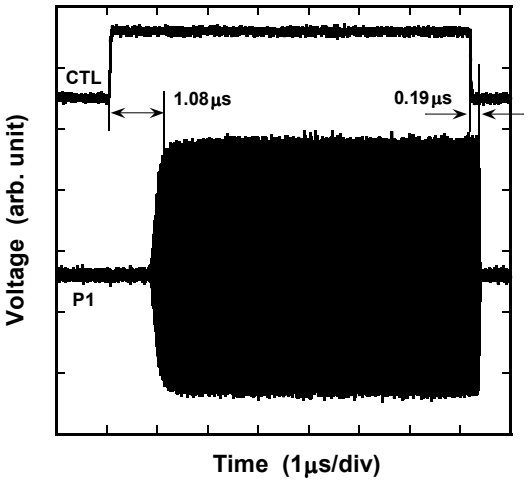
VSWR vs. Frequency

(V_{DD}=3V, V_{CTL}=0/3V)



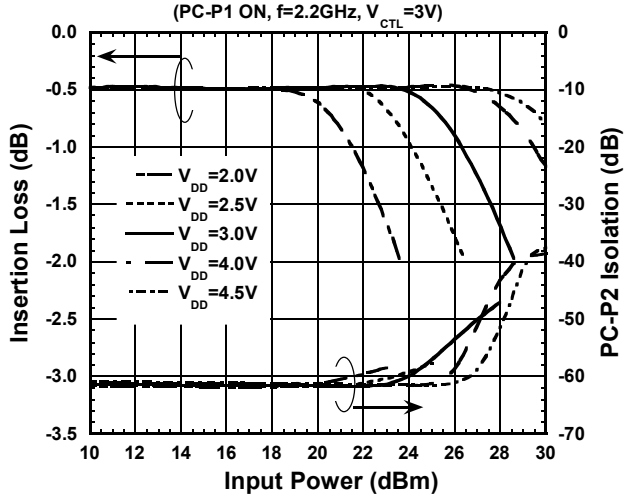
Switching Time

(PC-P1/P2, V_{DD}=3.0V, V_{CTL}=0/3.0V)



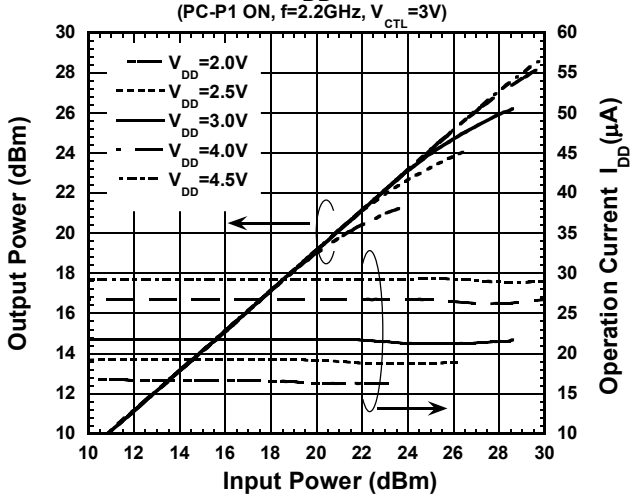
Loss, ISL vs. Input Power

(PC-P1 ON, f=2.2GHz, V_{CTL}=3V)



Output Power, I_{DD} vs. Input Power

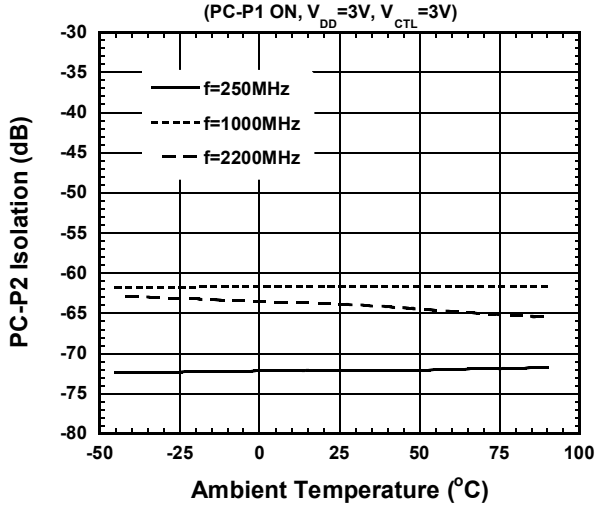
(PC-P1 ON, f=2.2GHz, V_{CTL}=3V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

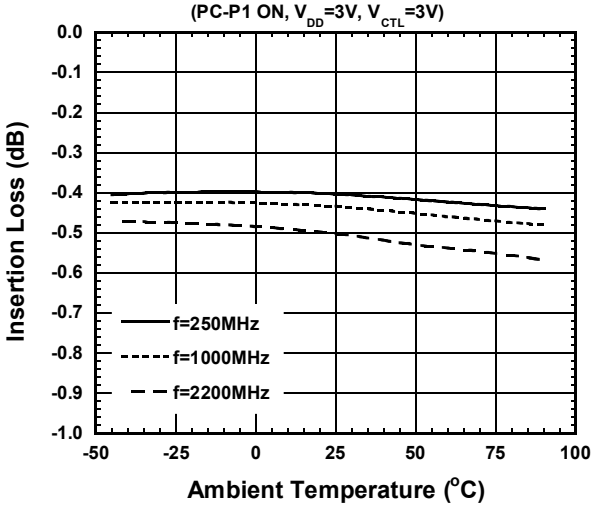
ISL vs. Ambient Temperature

(PC-P1 ON, V_{DD}=3V, V_{CTL}=3V)



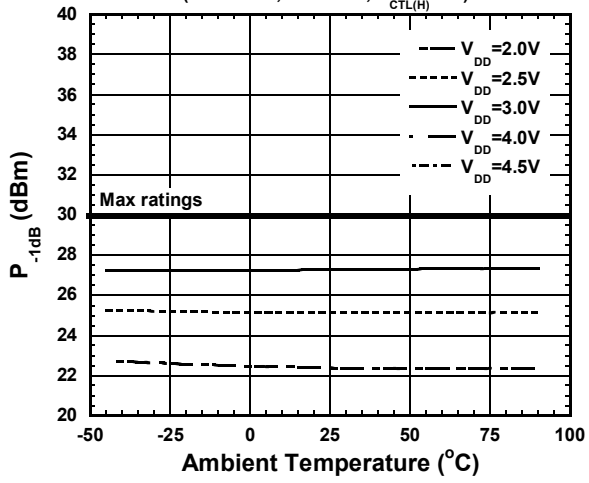
Loss vs. Ambient Temperature

(PC-P1 ON, V_{DD}=3V, V_{CTL}=3V)



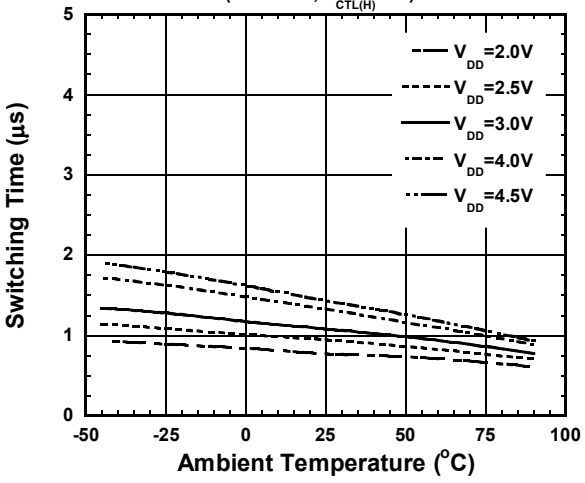
P_{-1dB} vs. Ambient Temperature

(PC-P1 ON, f=2.2GHz, $V_{CTL(H)}$=3V)



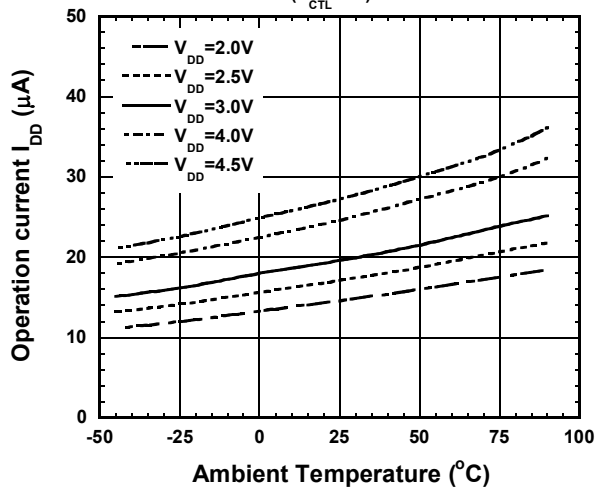
T_{SW} vs. Ambient Temperature

(PC-P1/P2, $V_{CTL(H)}$=3V)



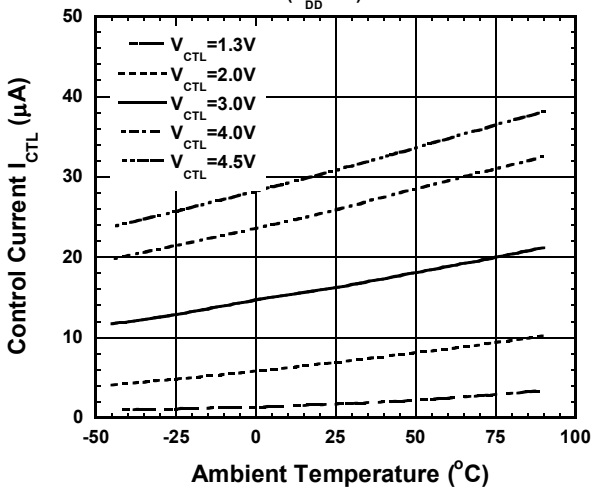
I_{DD} vs. Ambient Temperature

(V_{CTL}=0V)

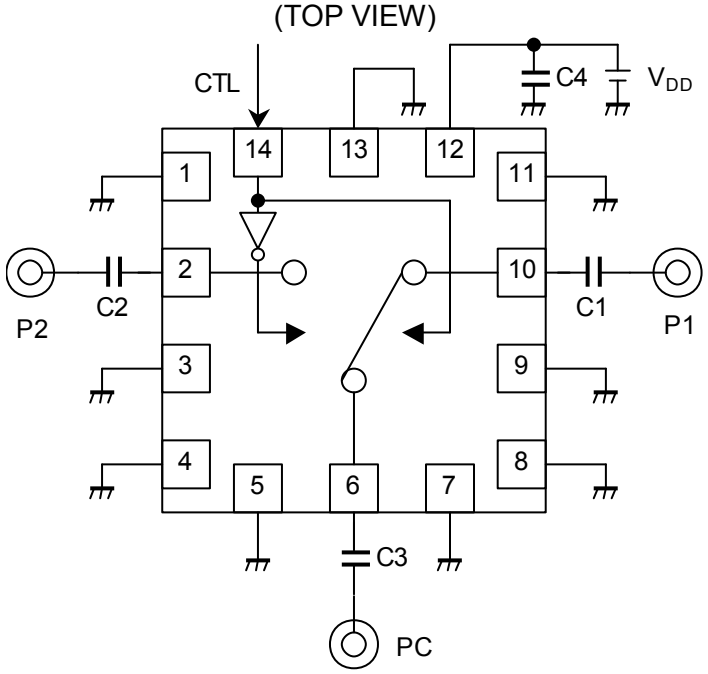


I_{CTL} vs. Ambient Temperature

(V_{DD}=0V)



■ APPLICATION CIRCUIT

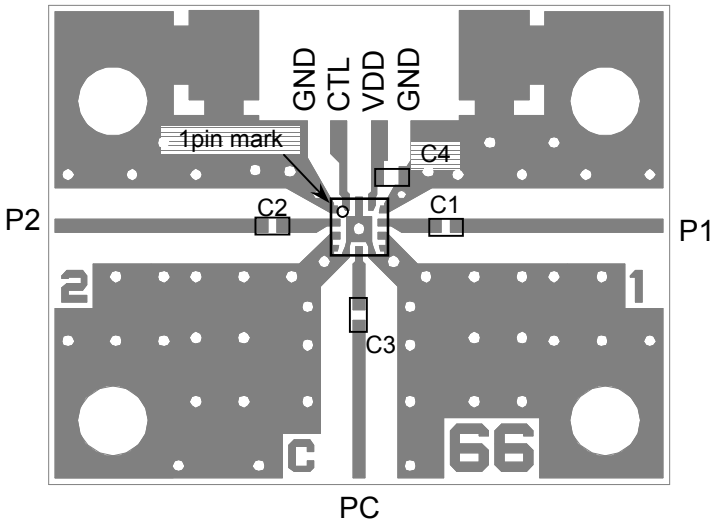


■ PARTS LIST

Parts ID	Value	Notes
C1~C4	1000pF	Murata MFG (GRM15)

■ TEST PCB LAYOUT

(TOP VIEW)



PCB SIZE = 19.4mm x 15.0mm
PCB: FR4, t = 0.2mm
CAPACITOR: SIZE 1005
STRIP LINE WIDTH = 0.4mm(Z_0=50Ω)

■ PCB LOSS

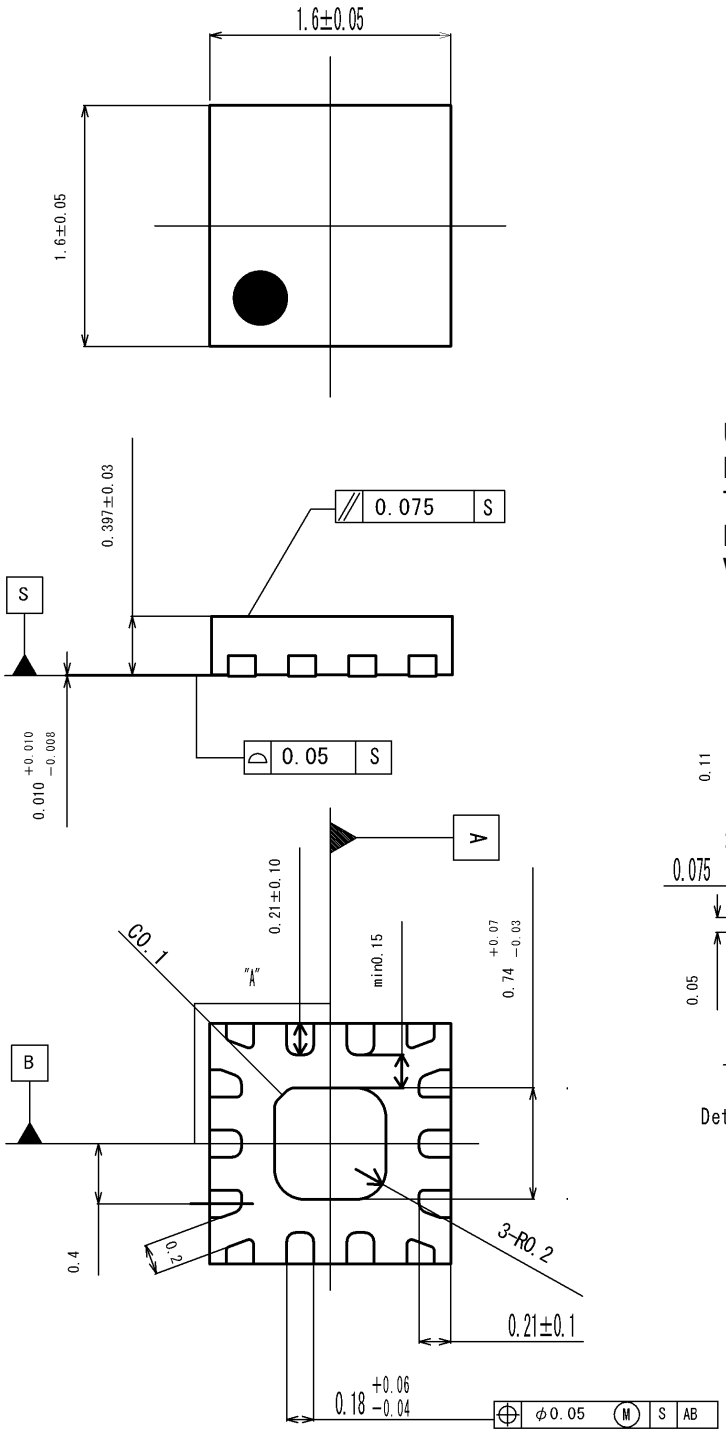
FREQ. (MHz)	PCB LOSS (dB)
250	0.11
1000	0.24
2200	0.40

*) Including PCB, Connector and DC Blocking Capacitor Losses

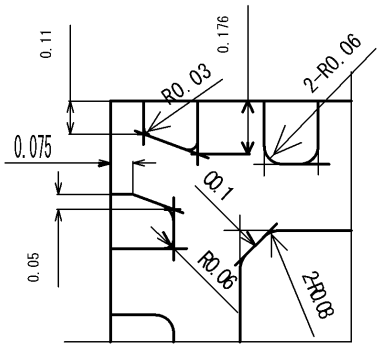
PRECAUTIONS

[1] The DC blocking capacitors have to be placed at RF terminal of PC, P1 and P2.
[2] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.
[3] Bypass capacitor (C4) should be placed close to terminal of VDD to reduce stripline influence of RF characteristics.

■ PACKAGE OUTLINE (EQFN14-D7)



Units : mm
Board : Cu
Terminal treat : SnBi
Molding material : Epoxy resin
Weight : 3.3mg



Details of"A" part (× 2)

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]
The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.