

# UT54ACS164/UT54ACTS164

## Radiation-Hardened 8-Bit Shift Registers

### FEATURES

- AND-gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Direct clear
- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 14-pin DIP
  - 14-lead flatpack

### DESCRIPTION

The UT54ACS164 and the UT54ACTS164 are 8-bit shift registers which feature AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high-level at both serial inputs sets the first flip-flop to the high level at the next clock pulse. Data at the serial inputs may be changed while the clock is high or low, providing the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

The devices are characterized over full military temperature range of -55°C to +125°C.

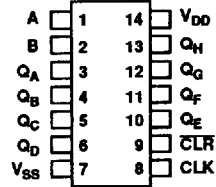
### FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	Q <sub>A</sub>	Q <sub>B</sub> ... Q <sub>H</sub>	
L	X	X	X	L	L ... L	
H	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub> ... Q <sub>H0</sub>	
H	↑	H	H	H	Q <sub>An</sub> ... Q <sub>Cn</sub>	
H	↑	L	X	L	Q <sub>An</sub> ... Q <sub>Cn</sub>	
H	↑	X	L	L	Q <sub>An</sub> ... Q <sub>Cn</sub>	

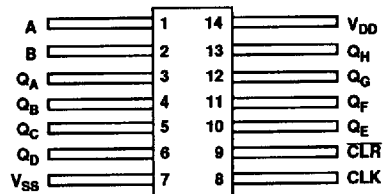
- Notes:
1. Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub> or Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established.
  2. Q<sub>An</sub> and Q<sub>Cn</sub> = the level of Q<sub>A</sub> or Q<sub>C</sub> before the most recent ↑ transition of the clock; indicates a one-bit shift.

### PINOUTS

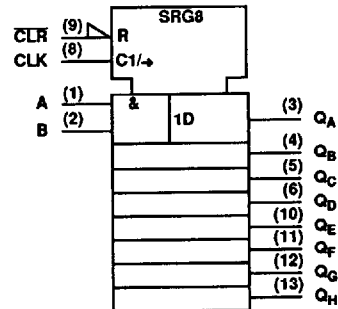
14-Pin DIP  
Top View



14-Lead Flatpack  
Top View

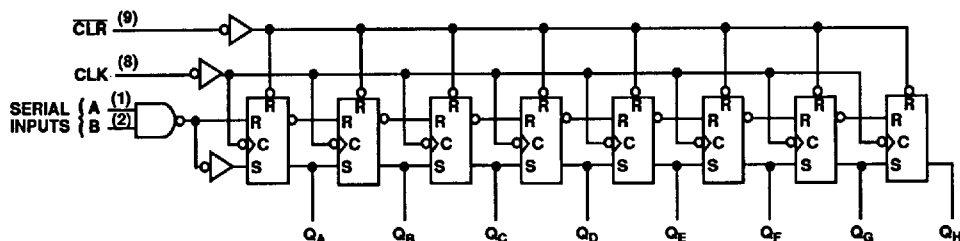


### LOGIC SYMBOL



- Note:
1. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

Notes:

- 1. Logic will not latchup during radiation exposure within the limits defined in the table.
- 2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V <sub>DD</sub>	Supply voltage	4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C

UT54ACS164/UT54ACTS164

DC ELECTRICAL CHARACTERISTICS <sup>7</sup>

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>6</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup> ACTS ACS			0.8 .3 $V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> ACTS ACS		.5 $V_{DD}$ .7 $V_{DD}$		V
$I_{IN}$	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or $V_{SS}$	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup> ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
$V_{OH}$	High-level output voltage <sup>3</sup> ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$	.7 $V_{DD}$ $V_{DD} - 0.25$		V
$I_{OS}$	Short-circuit output current <sup>2,4</sup> ACTS/ACS	$V_O = V_{DD}$ and $V_{SS}$	-200	200	mA
$P_{total}$	Power dissipation <sup>8,9</sup>	$C_L = 50pF$		1.9	mW/ MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{DD} = 5.5V$		10	$\mu A$
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH}(min) + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL}(max) + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH}(min)$  and  $V_{IL}(max)$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>**(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V <sup>1</sup>, -55°C < T<sub>C</sub> < +125°C)

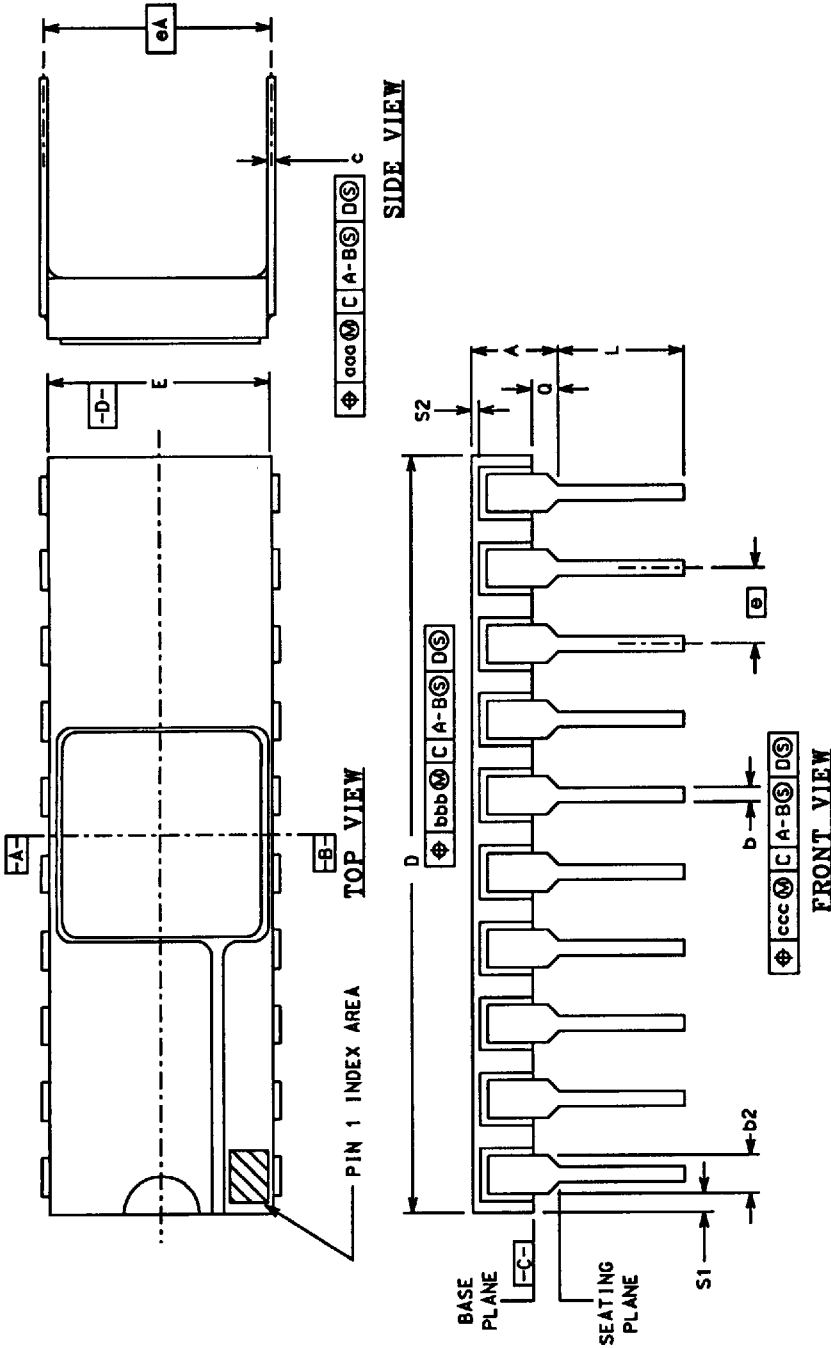
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t <sub>PHL</sub>	CLK to Qn	1	21	ns
t <sub>PLH</sub>	CLK to Qn	1	18	ns
t <sub>PHL</sub>	CLR to Qn	1	21	ns
f <sub>MAX</sub>	Maximum clock frequency		83	MHz
t <sub>SU</sub>	Setup time before CLK ↑ CLR inactive Data	4		ns
t <sub>H</sub>	Data hold time after CLK ↑	2		ns
t <sub>w</sub>	Minimum pulse width CLR low CLR high CLK low	6		ns

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).

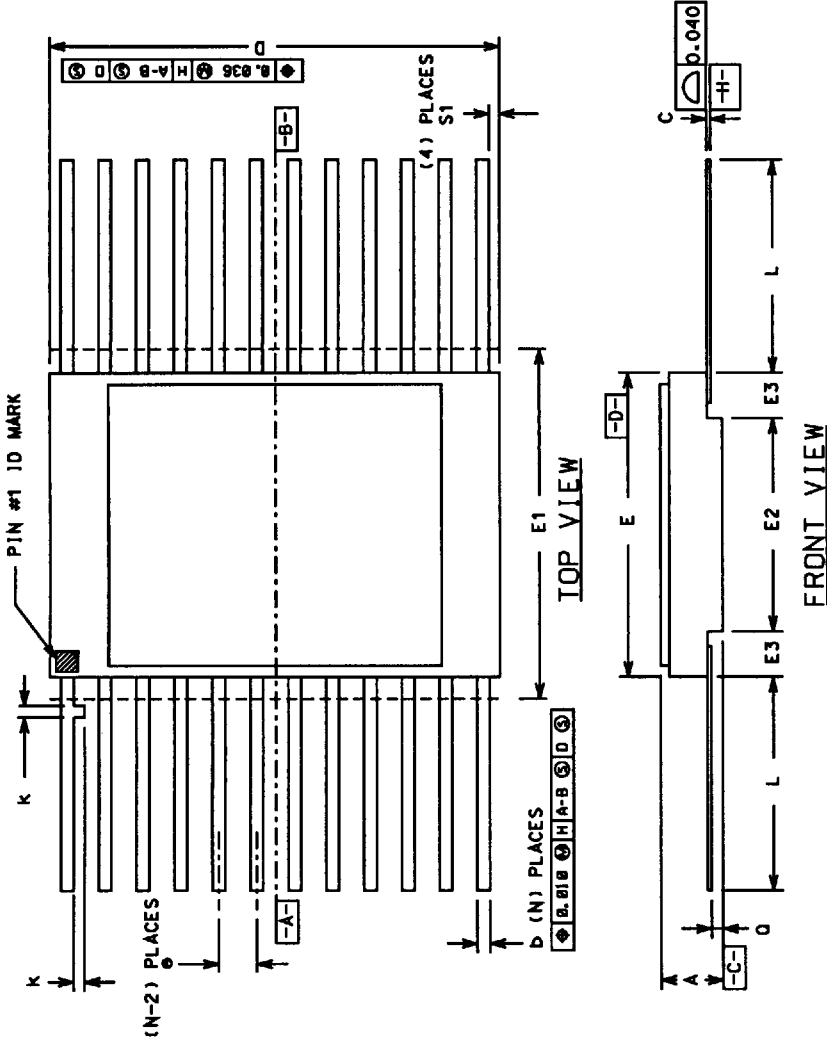
## 2.0 RAD-HARD MSI PACKAGES

### Side-Brazed Packages



PKG CONFIG	MIL-STD- 1835 Dwg CONF C	DIMENSION SYMBOLS														
		A	b	b2	c	D	E	e	eA	L	Q	S1	S2	ddd	bbb	ccc
-01	14 D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-02	16 D-2	0.200	0.014	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-03	20 D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.200	0.125	0.015	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.200	0.125	0.015	0.005	0.015	0.030	0.010

# Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS														
			A	b	c	D	E	E1	E2	E3	e	k	L	o	S1		
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.235	---	---	---	---	---	BSC	0.008	0.270	0.026	0.005
-04	16	F-5A	0.115	0.022	0.009	0.440	0.285	0.315	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	---	---	---	---	BSC	0.008	0.250	0.026	0.005
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	---	---	---	---	BSC	0.008	0.250	0.026	0.000