HB56G232 Series

2,097,152-word × 32-bit High Density Dynamic RAM Module

HITACHI

Description

The HB56G232 is a 2M × 32 dynamic RAM module, mounted 4 pieces of 16-Mbit DRAM (HM5118160AJ) sealed in SOJ package.

An outline of the HB56G232 is 72-pin single in-line package. Therefore, the HB56G232 makes high density mounting possible without surface mount technology.

The HB56G232 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

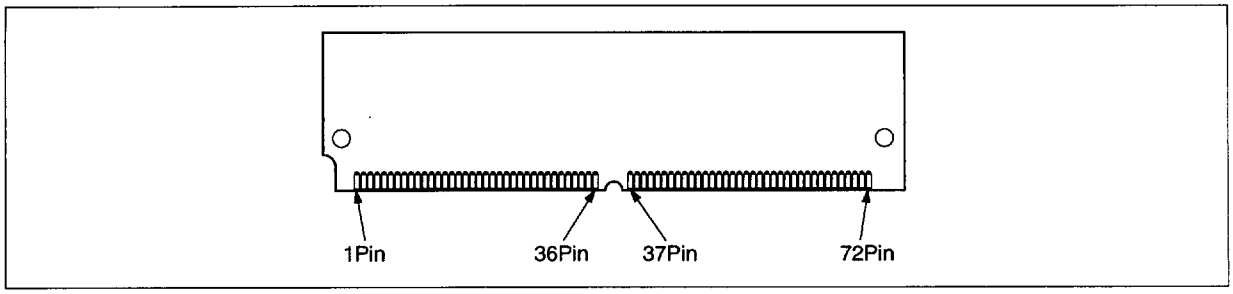
Features

- 72-pin single in-line package
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 70/80 ns (max)
- Low power dissipation
  - — Active mode: 1.7 W/1.5 W (max)
  - — Standby mode: 42 mW (max)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56G232B-7A	70 ns	72-pin SIP socket type	Gold
HB56G232B-8A	80 ns		
HB56G232SB-7A	70 ns	72-pin SIP socket type	Solder
HB56G232SB-8A	80 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{RAS1}$	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

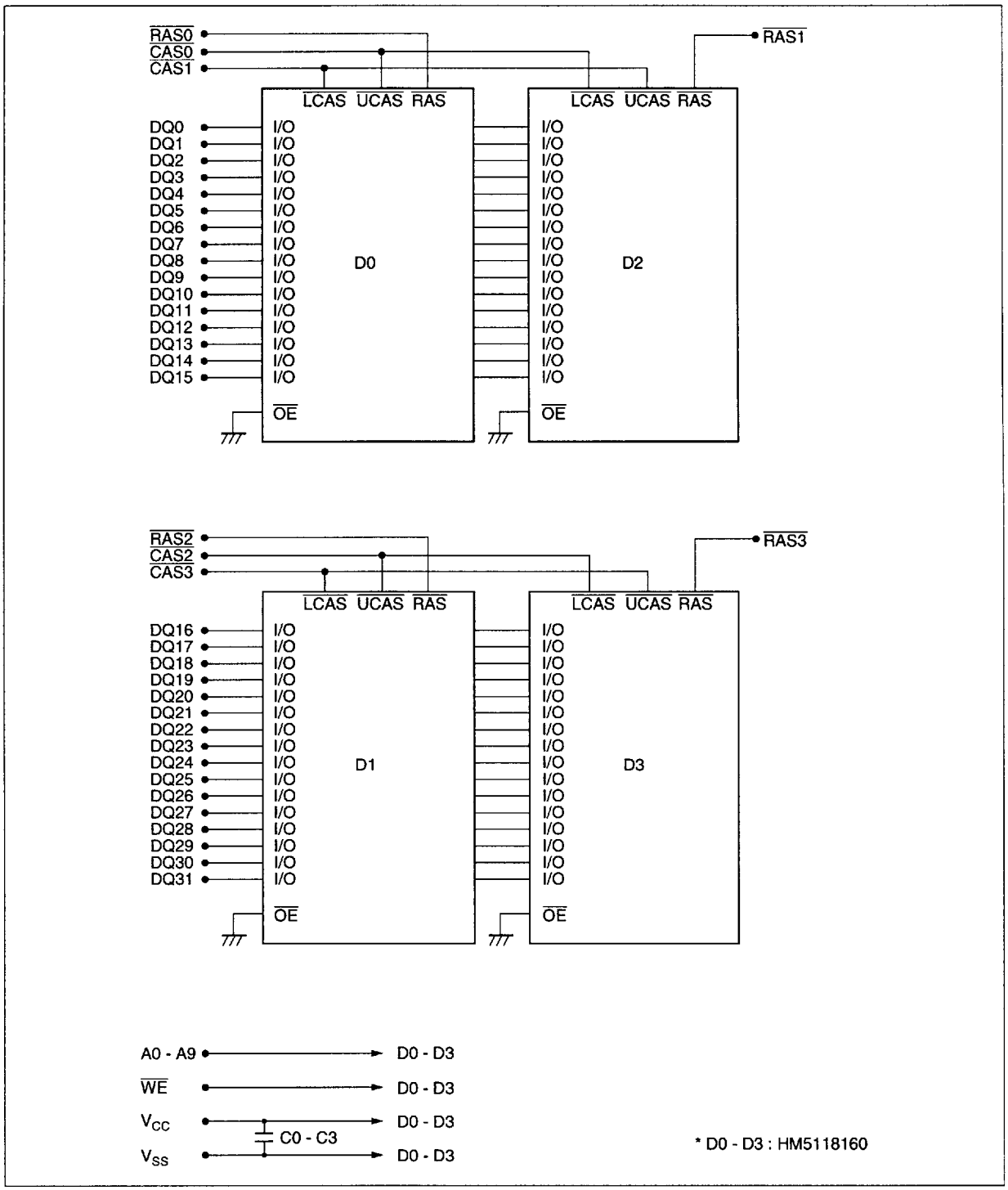
Pin Description

Pin Name	Function
A0 – A9	Address Input
A0 – A9	Refresh Address Input
DQ0 – DQ31	Data-in/Data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence Detect Pin
NC	No Connection

Presence Detect Pin Assignment

		Function	
Pin No.	Pin Name	70 ns	80 ns
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	V_{SS}	NC
70	PD4	NC	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	2	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56G232						
		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions	Notes
Operating current	I_{CC1}	—	310	—	270	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	8	—	8	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	4	—	4	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	310	—	270	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	20	—	20	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	310	—	270	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	310	—	270	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	40	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	48	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	27	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	34	pF	1
I/O capacitance (DQ0 – 31)	$C_{I/O}$	—	34	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

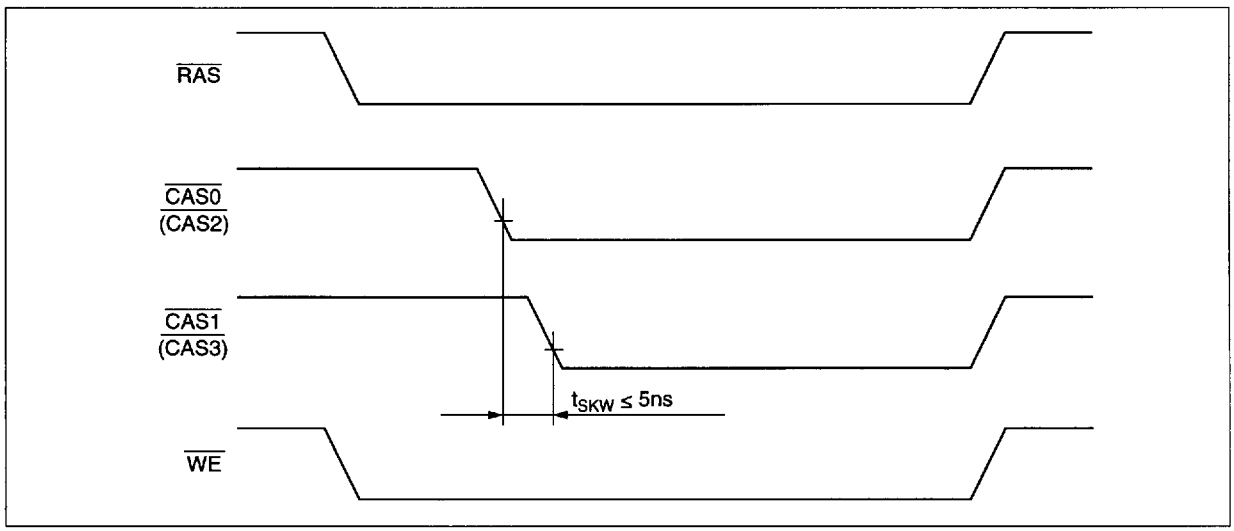
AC Characteristics

- Refer to the HM5118160A Series data sheet.
- The HB56G232 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
  Delayed write cycle is not available ($\overline{OE}$ pin is fixed to V_{SS}).

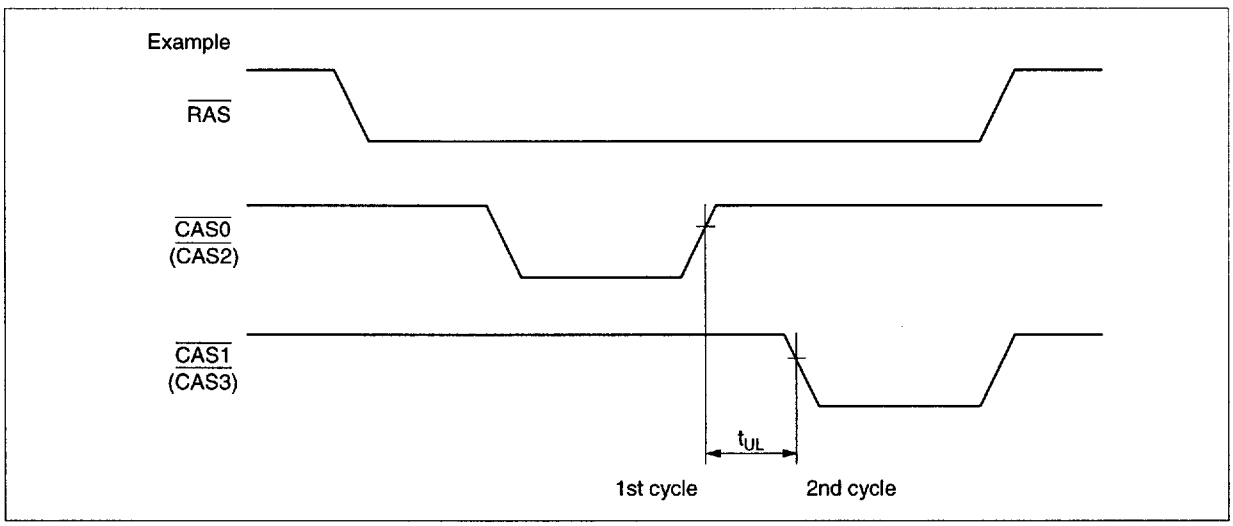
Notes on 2$\overline{CAS}$ control

(1) In one memory cycle, activate both of 2$\overline{CAS}$s ($\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$, or $\overline{CAS2}$ and $\overline{CAS3}$) 5 ns or less.



(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL} the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min $\leq t_{UL}$).



Physical Outline

Unit: mm/inch