CFM8450A

DESCRIPTION: CFM8450A is designed to be functionally compatible with the Hitachi HD6845 "S" version. Performance is much improved. I/Os can be made compatible to the standard part, as shown in the diagram on page 4 of 5. Note that the RD_EN output is used to gate the output of data lines. All other signals are compatible to the standard part. For functional information, see the Hitachi data sheet.

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INPUTS (LOADING IN TRANSISTOR PAIRS):
                CSN(1.5),RS(3),E(4),R_W(2),RESETN(3),CK(19),
                LPSTB(3.5),DI07(1),DI06(1),DI05(1),
                DI04(1),DI03(1),DI02(1),DI01(1),
                DI00(1)

OUTPUTS (DRIVE IN(#P,#N)):
                RA4(2,2),RA3(2,2),RA2(2,2),RA1(2,2),RA0(2,1),
                MA13(2,2),MA12(2,2),MA11(2,2),MA10(2,2),MA09(2,2),
                MA08(2,2),MA07(2,2),MA06(2,2),MA05(2,2),
                MA04(2,2),MA03(2,2),MA02(2,2),MA01(2,2),
                MA00(2,2),VSYNC(2,0.66),HSYNC(4,2),DE(2,0.66),
                CURSOR(2,0.66),RD_EN(8,8),DO7(2,1),DO6(2,1),
                DO5(2,1),DO4(2,1),DO3(2,1),DO2(2,1),
                DO1(2,1),DO0(2,1)

                Z(RA4,RA3,RA2,RA1,RA0,MA13,MA12,MA11,MA10,
                  MA09,MA08,MA07,MA06,MA05,MA04,MA03,MA02,MA01,
                  MA00,VSYNC,HSYNC,DE,CURSOR,RD_EN,DO7,DO6,DO5,
                  DO4,DO3,DO2,DO1,DO0)
                  =CFM8450A (CSN,RS,E,R_W,RESETN,CK,LPSTB,
                             DI07,DI06,DI05,DI04,DI03,DI02,
                             DI01,DI00)$

GATE COUNT:     ARRAY GATE USAGE = 3145
                ARRAY AREA USAGE = 3217
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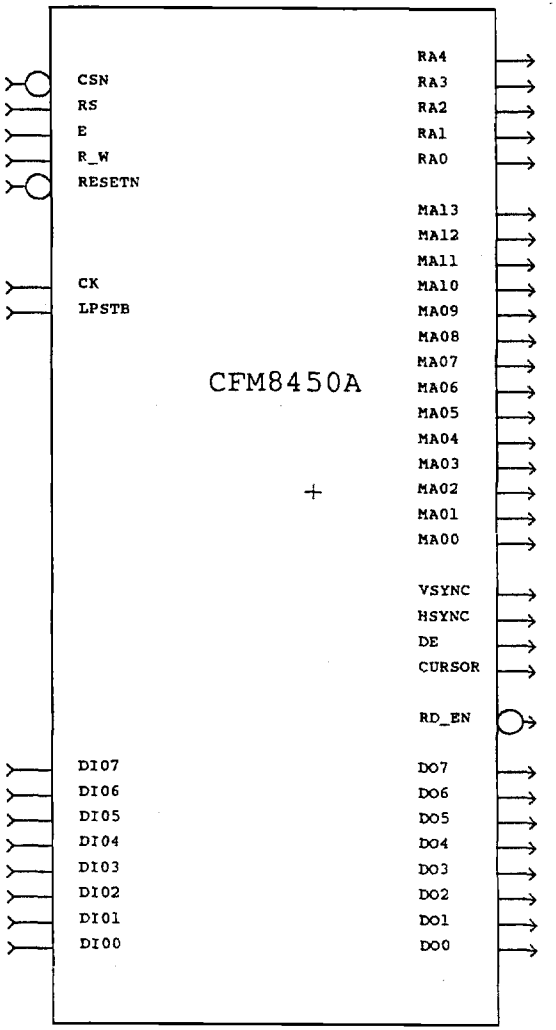
LOGIC SYMBOL:



AC CHARACTERISTICS

ITEM	MIN.	MAX.
T(CYC)C	70	
PW(CH)	35	
PW(CL)	35	
T(MAD)		35
T(RAD)		35
T(DTD)		35
T(CDD)		35
T(HSD)		35
T(VSD)		35
PW(LPH)	50	
T(LPD1)		20
T(CYC)E	70	
PW(EH)	35	
PW(EL)	35	
T(AS)	20	
T(DDR) RD		20
T(H)	10	
T(AH)	10	
T(ACC) RD		40
T(DSW) WR	10	

*ALL UNITS IN NS & ARE TYPICAL(10K TECHNOLOGY)