16M ×1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	tRAC	tCAC	tRC
KM41C16002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16002A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **Self Refresh Operation (LL-ver, only)**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V±10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

The Samsung KM41C16002A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit×1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

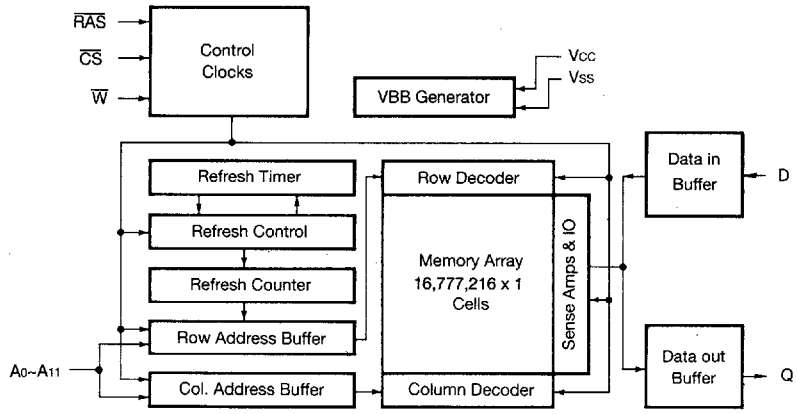
The KM41C16002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C16002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

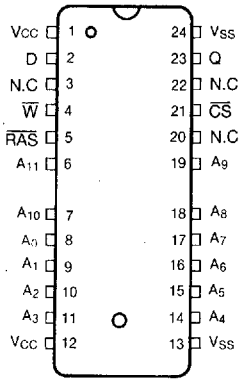
5

FUNCTIONAL BLOCK DIAGRAM



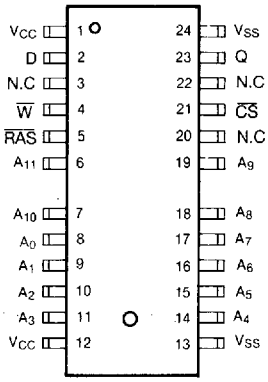
PIN CONFIGURATION (Top Views)

• KM41C16002 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



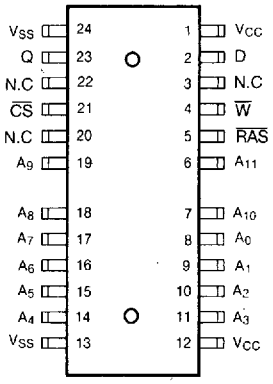
J : 400MIL
K : 300MIL

• KM41C16002 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S: 300MIL(Forward)

• KM41C16002 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data out
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select input
$\overline{W}$	Read/Write Input
VCC	Power(+5.0V)
VSS	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC1}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})	KM41C16002A	I_{CC2}	-	2	mA
	KM41C16002AL			1	mA
	KM41C16002ALL			1	mA
	KM41C16002ASL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC3}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address Cycling @t_{PC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC4}	-	80	mA
	KM41C16002A/AL/ALL/ASL-6			70	mA
	KM41C16002A/AL/ALL/ASL-7			60	mA
	KM41C16002A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)	KM41C16002A	I_{CC5}	-	1	mA
	KM41C16002AL			300	μA
	KM41C16002ALL			200	μA
	KM41C16002ASL			200	μA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C16002A/AL/ALL/ASL-5	I_{CC6}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CS}$=$\overline{CS}$-Before-$\overline{RAS}$ Cycling or 0.2V D=Don't Care t_{RC}=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t_{RAS} =t_{RAS} min~300ns	KM41C16002AL	I_{CC7}	-	450	μA
	KM41C16002ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CS}$=0.2V $\overline{W}$=A0-A11=Vcc-0.2V or 0.2V Vcc-0.2V, 0.2V or Open	KM41C16002ALL	I_{CCS}	-	300	μA
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volts.)		I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)		I_{OL}	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	7	pF
Input Capacitance (A0~A11)	C_{IN2}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	115		135		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	40		50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	13		15		20		20		ns	
Data set-up time	t_{DS}	0		0		0		0		ns	10
Data hold time	t_{DH}	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	t_{DHR}	40		50		55		60		ns	6
Refresh period (Normal)	t_{REF}		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	t_{REF}		128		128		128		128	ms	
Refresh period (Super Low power)	t_{REF}		256		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	15		15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		20		30		30		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	3
Static column mode read-write cycle time	t_{SRWC}	50		60		70		80		ns	
Access time from last write	t_{ALW}		50		55		65		75	ns	3, 12
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{CS}$ pulse width (Static column mode)	t_{CSC}	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10		10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ rising	t_{AH}	5		5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	25	20	25	25	30	25	35	ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Last write to column address hold time	t_{AHLW}	50		55		65		75		ns	
Write command inactive time	t_{WI}	10		10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	13		15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		100		μs	15
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	90		110		130		150		ns	15
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	140		160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	80		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		70		75		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-write cycle time	t_{SRWC}	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	t_{ALW}		50		60		70		80	ns	3,12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

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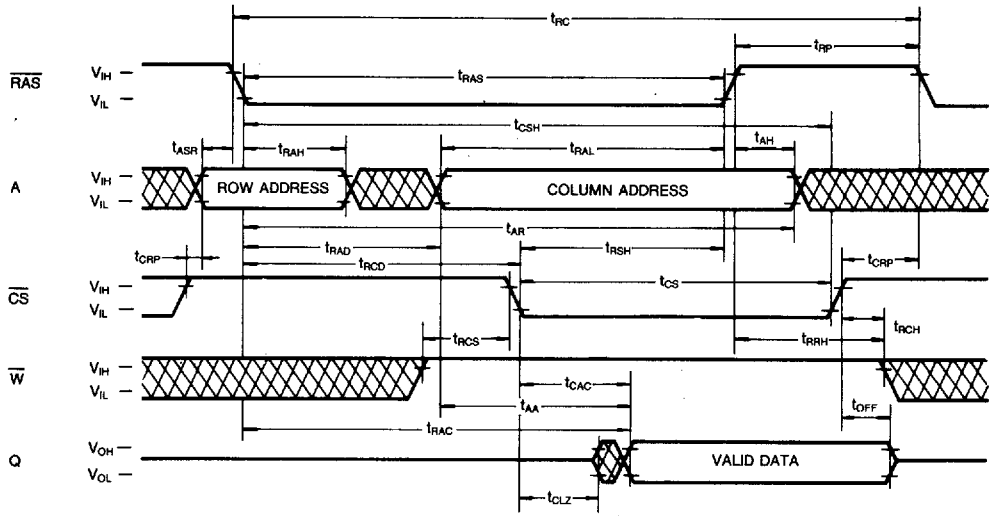
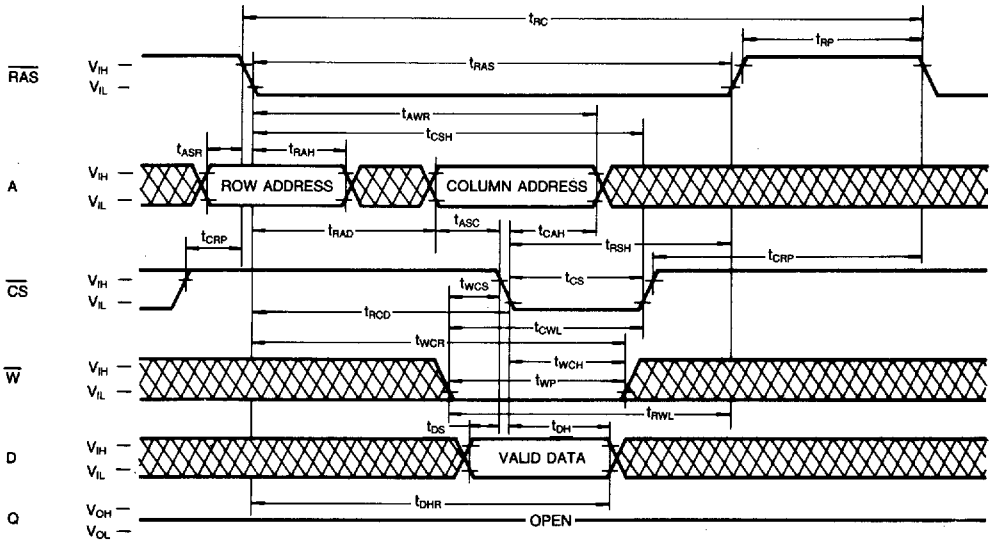
TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

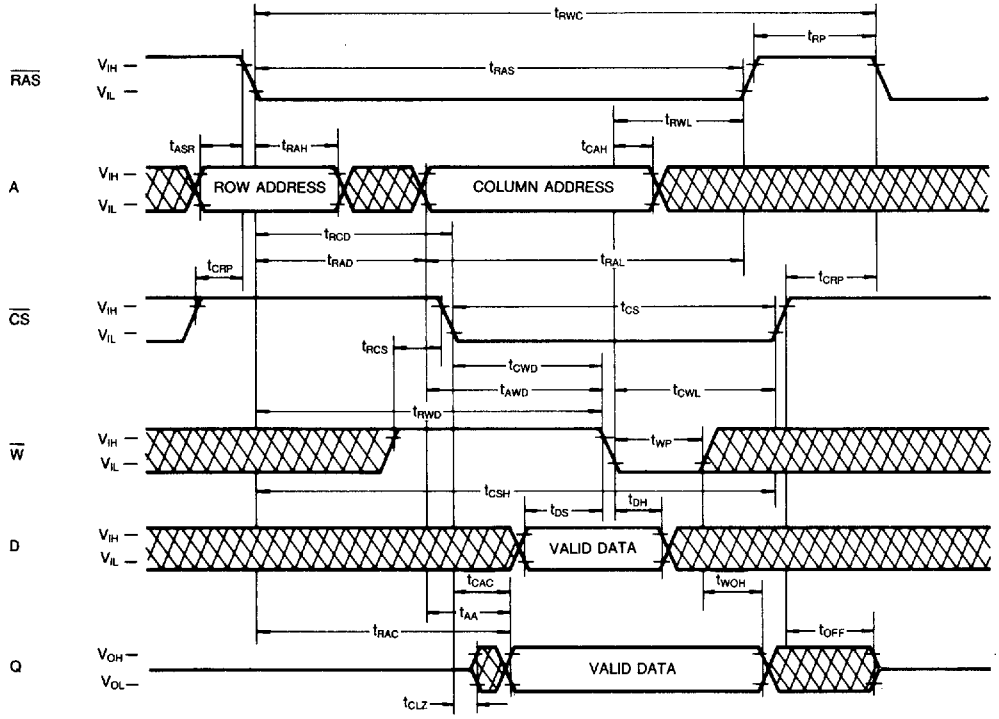


DON'T CARE

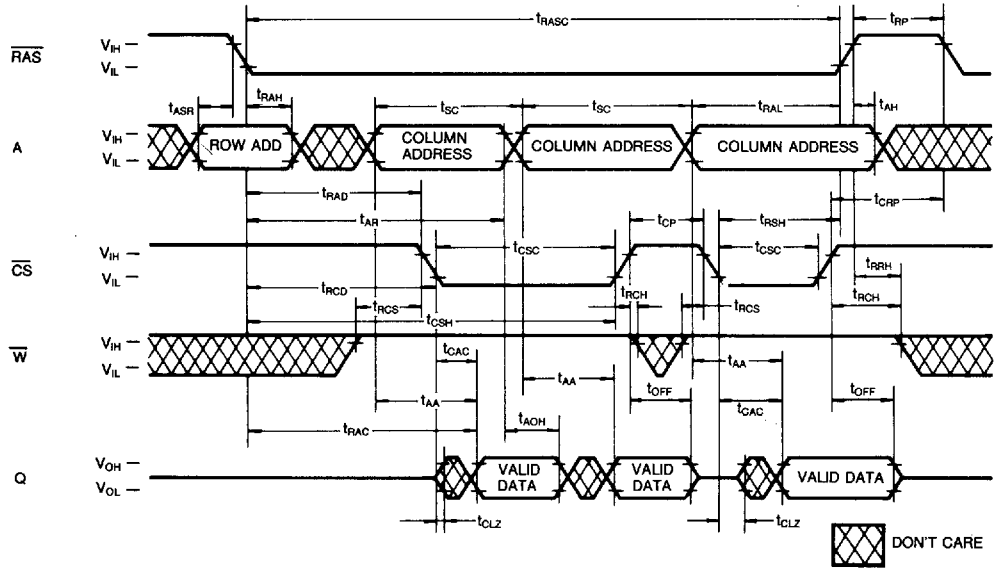
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

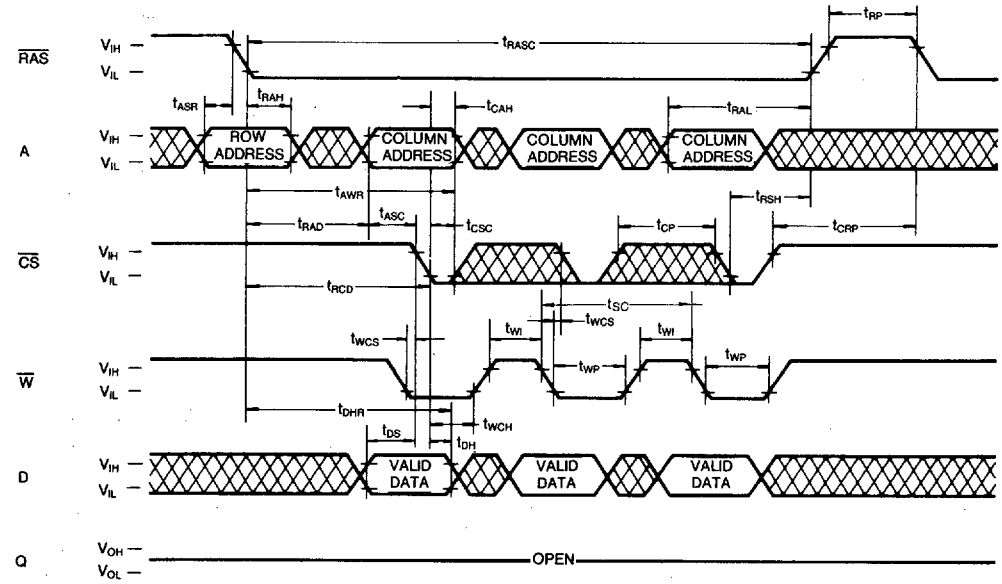


STATIC COLUMN MODE READ CYCLE

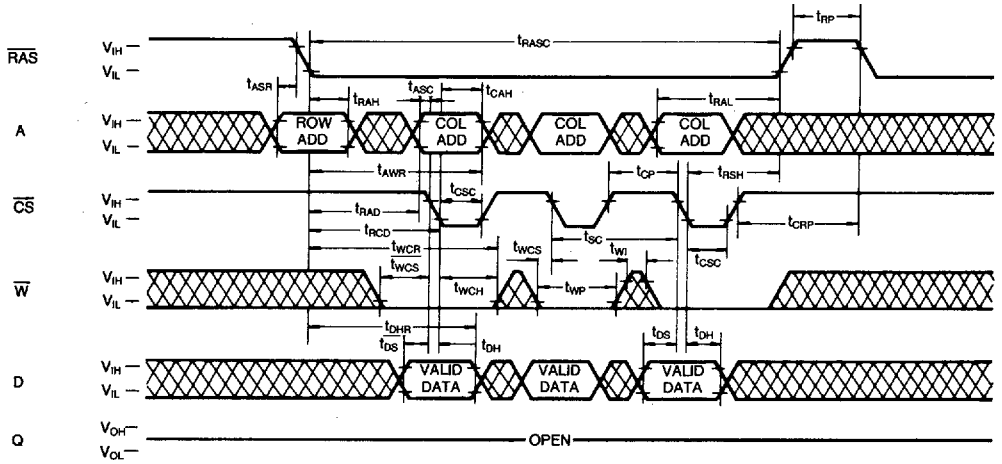


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)



STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)

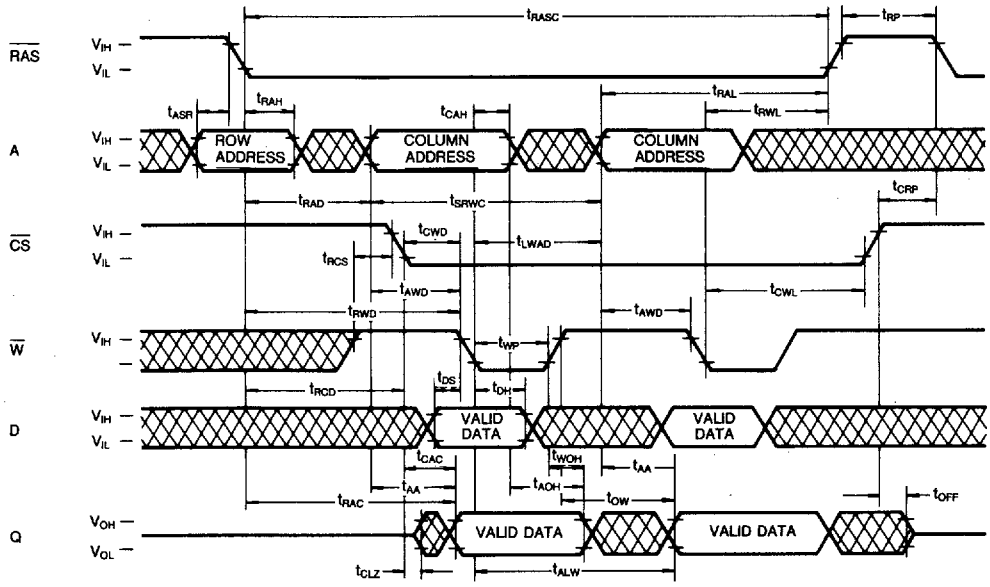


DON'T CARE

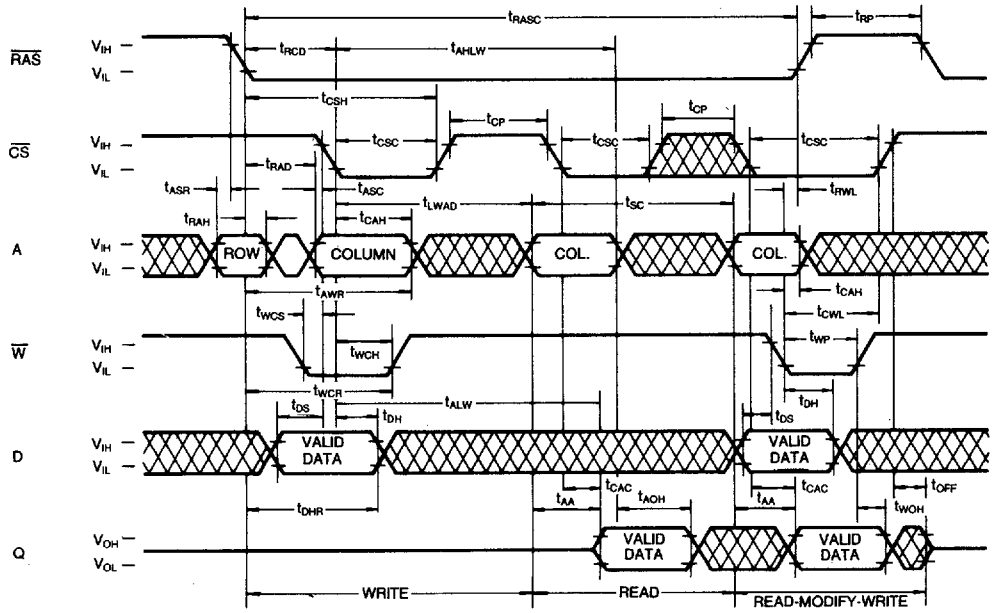
SAMSUNG ELECTRONICS

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

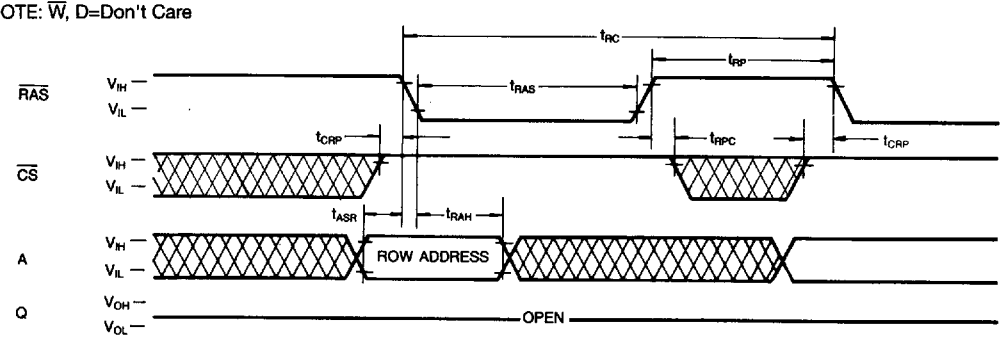


DON'T CARE

TIMING DIAGRAMS (Continued)

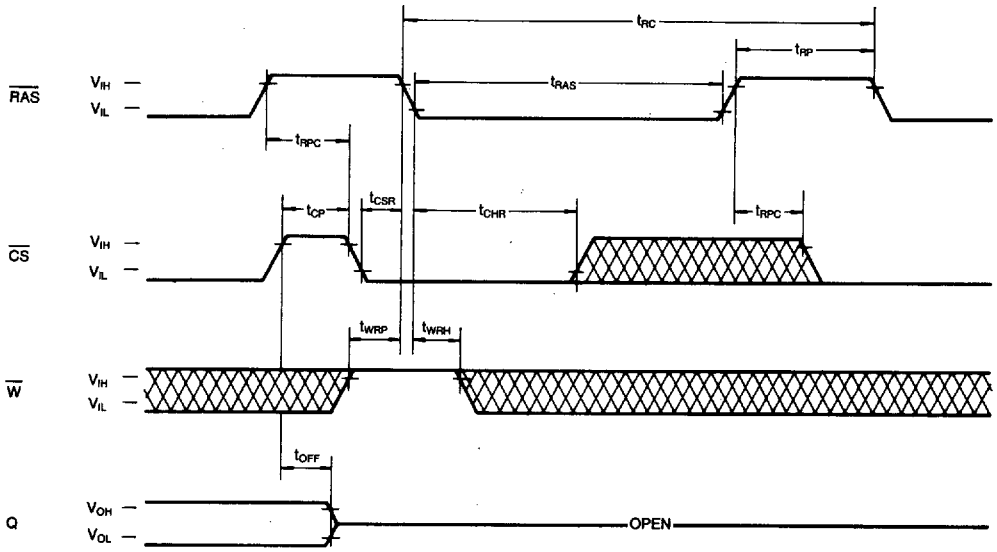
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

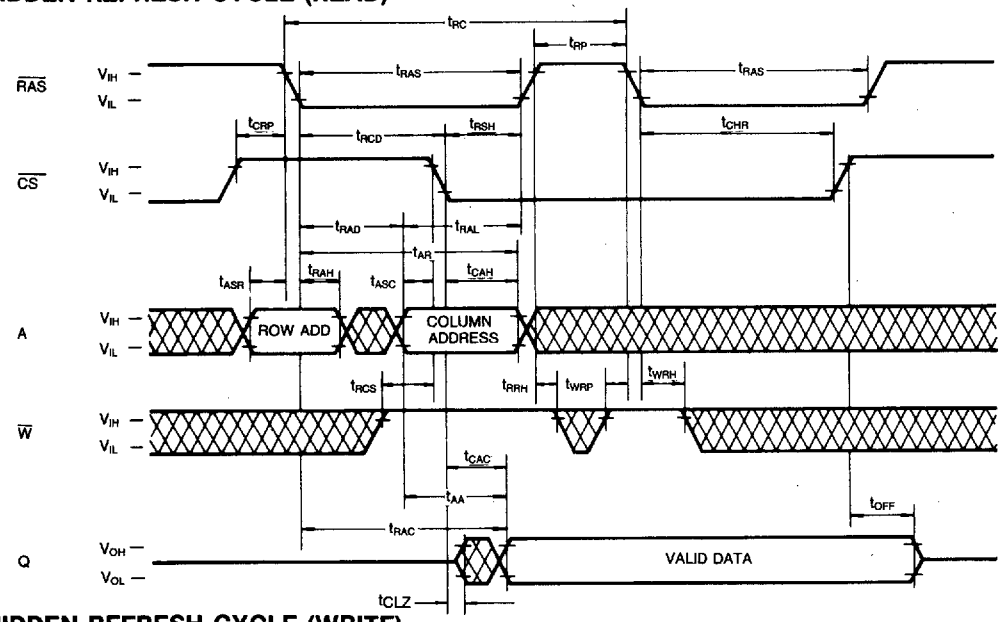
NOTE: Address=Don't Care



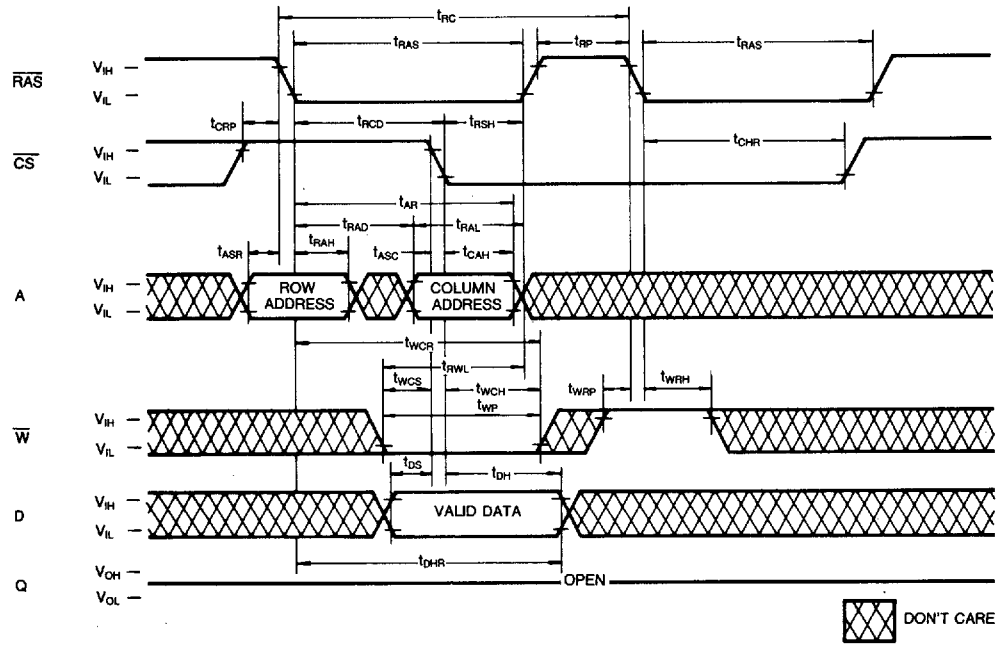
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



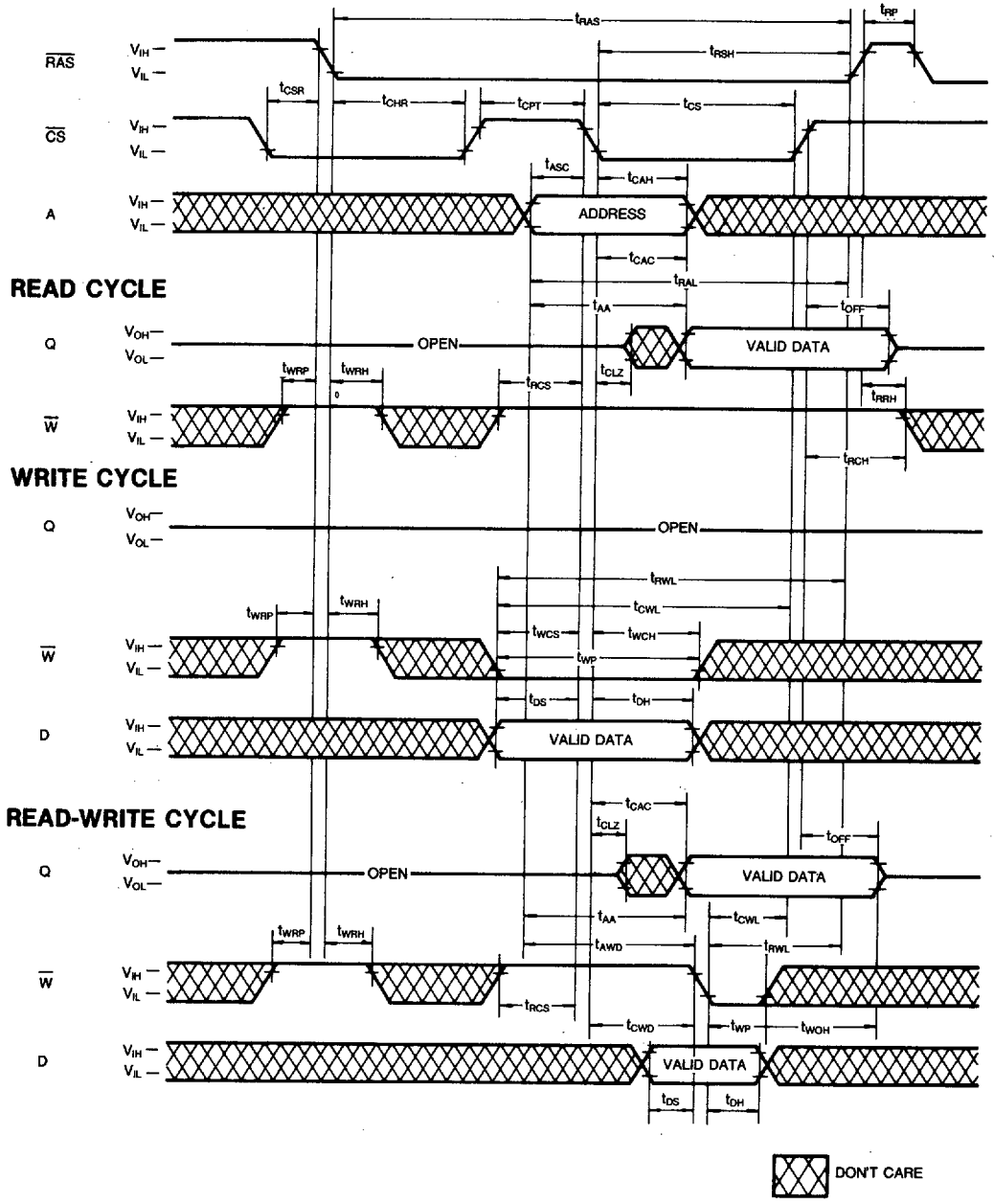
HIDDEN REFRESH CYCLE (WRITE)



5

TIMING DIAGRAMS (Continued)

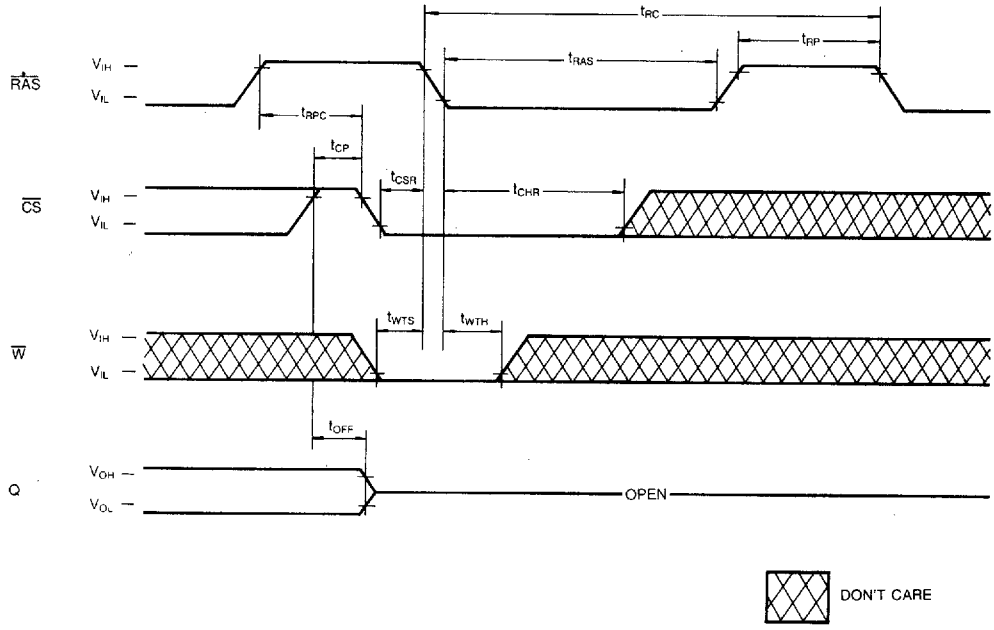
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

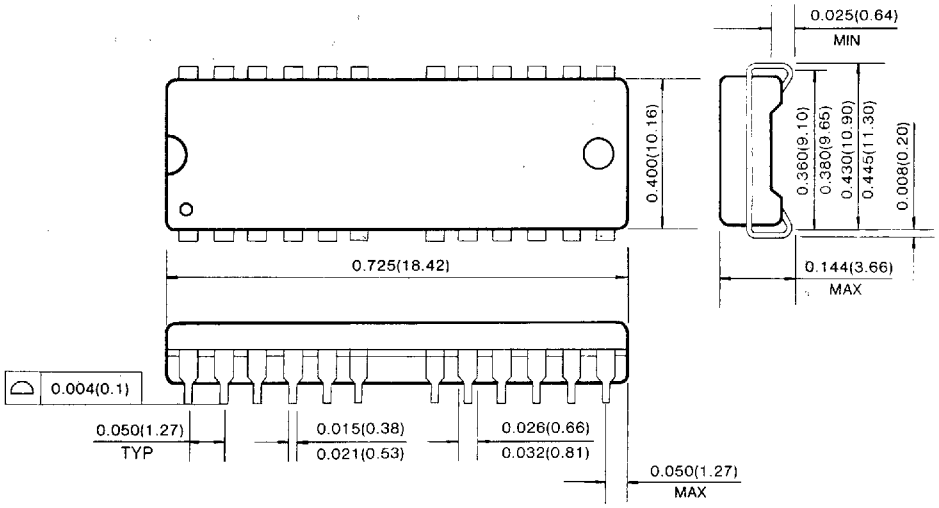
The KM41C16002 is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test mode," data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1."

If they were not equal, the Q pin would indicate a "0." In "Test Mode," the 16M DRAM can be tested as if it were a 1M × 1 DRAM. $\overline{W}$, $\overline{CS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode." And "$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode." The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

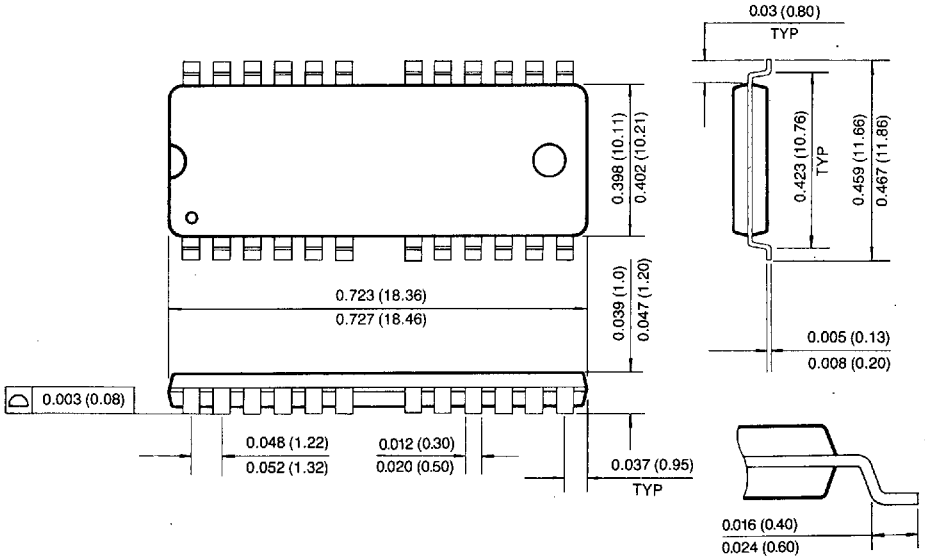
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



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