SEEQ® Technology, Incorporated

83C91
MCC™ Manchester Code Converter

PRELIMINARY

July 1992

Features

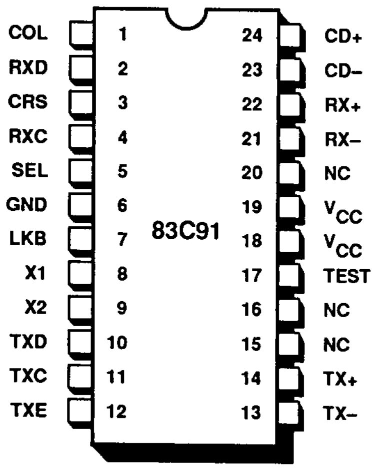
- *Compatible with IEEE 802.3 10BASE-5, 10BASE-2, and 10BASE-T.*
- *10 Mbits/s Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop.*
- *Receiver and Collision Squelch Circuit to Reject Noise.*
- *Requires No External Precision Components.*
- *Loopback Capability for Diagnostics and Isolation.*
- *Decodes Manchester Data with Up to 20 ns of Jitter*
- *Manchester Decoder Acquires Clock and Data within 5 Bit Times*
- *Externally Selectable Half or Full Step Modes of Operation at Transmit Output*
- *TTL/MOS Compatible Controller Interface.*
- *Low Power Dissipation Fabricated by CMOS Process*
- *Functionality and Pin-Out are Compatible with NS DP83910*

General Description

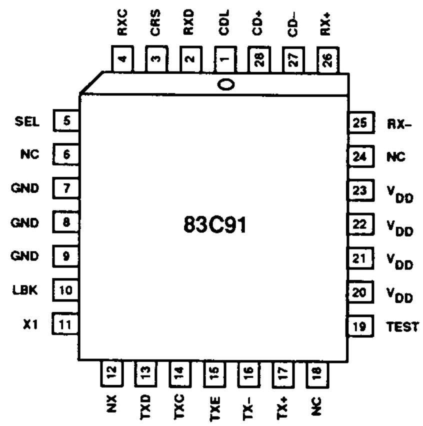
The SEEQ 83C91 Manchester Code Converter (MCC) chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. The 83C91 interfaces the SEEQ 83C90 Ethernet Data Link Controller (EDLC) and any other standard Ethernet transceiver, as defined by IEEE 802.3. When transmitting, the 83C91 converts non-return-to-zero (NRZ) data from the controller into Manchester data and sends the converted data differentially to the transceiver. When receiving a Phase Locked Loop (PLL) decodes the 10 MHz bit per second data from the transceiver into NRZ data for the controller.

Pin Configurations

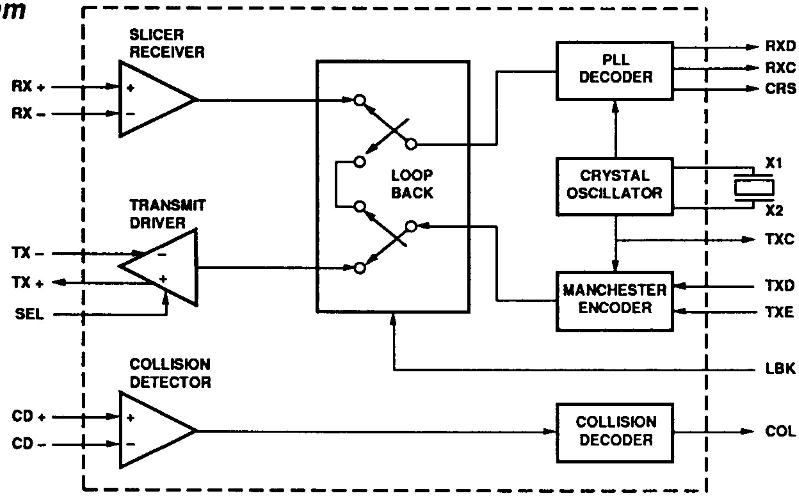
Dual-In-Line
Top View



Plastic Leaded Chip Carrier (PLCC)
Top View



Block Diagram



Pin Descriptions

Name	Pin No.	PLCC Pin No.	I/O	Pin Description
COL	1	1	O	COLLISION DETECT OUTPUT: It is HIGH when 10 MHz collision signal is detected
RXD	2	2	O	RECEIVE DATA OUTPUT: NRZ data output from the PLL. This signal must be sampled on the rising edge of receive clock.
CRS	3	3	O	CARRY SENSE: Asserted on the first valid high-to-low transition in receive data. Remains active until 1.5 bit times after the last bit in data.
RXC	4	4	O	RECEIVER CLOCK: The receive clock from the Manchester data after the PLL has locked. Remains active 5 bit times after desserting CRS.
SEL	5	5	I	MODE SELECT: When high TX+ and TX– are the same voltage in the idle state. When low, TX+ is positive with repsect to TX– in the idle state at the transformer's primary.
GND	6	7, 8, 9	G	GROUND PIN.
LBK	7	10	I	LOOPBACK CONTROL: When high, the loopback mode is enabled.
X1	8	11	I	CRYSTAL or EXTERNAL CLOCK INPUT.
X2	9	12	O	CRYSTAL FEEDBACK OUTPUT: Used in crystal connection only. Left open when using an external clock.
TXD	10	13	I	TRANSMIT DATA INPUT: NZR data input from the controller. TXD is sampled on the riding edge of the transmit clock.

Pin Description (Continued)

Name	Pin No.	PLCC Pin No.	I/O	Pin Description
TXC	11	14	O	TRANSMIT CLOCK: The 10 MHz clock derived from the 20 MHz oscillator
TXE	12	15	I	Transmit Enable: When high, the ERA will allow encoding of Manchester data from TXD to TX+/TX–.
TX– TX+	13 14	16 17	O	TRANSMIT OUTPUT: Differential line driver which sends the encoded data to the transceiver. The outputs are source followers which require 270 Ohms pull down resistors.
TEST	17	19	I	TEST INPUT: Used to check the chip's internal function. May be tied low or tied through a 0.01 micro Farady capacitor to ground
V_{DD}	18, 19	20-23	P	5V POWER connection.
RX– RX+	21 22	25 26	I	RECEIVE INPUT: Differential receive input pair from the transceiver
CD– CD+	23 24	27 28	I	COLLISION INPUT: Differential collision input pair from the transceiver
NC	15, 16, 20	6, 18, 24		NO CONNECTION

The 83C91 is a functionally complete Manchester encoder/decoder including a balanced driver and receiver, 20 MHz crystal oscillator, collision signal translator, and a diagnostic loop back feature.

The 83C91 is fabricated using SEEQ's CMOS process and typically consumes less than 50 mA of current. It is pin-to-pin compatible with the NS DP83910.

Functional Description

The 83C91 includes five main functional blocks.

(1) The 20 MHz crystal oscillator which generates the 10 MHz transmit clock signal for system timing.
(2) The transmitter/encoder functional block.
(3) The receiver/decoder functional block.
(4) The collision detector functional block.
(5) The loopback functional block.

(1) Oscillator

The oscillator is controlled by a 20 MHz parallel resonant crystal connected between X1 and X2. The 20 MHz output of the oscillator is divided by 2 to generate the 10 MHz transmit clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits. It is recommended that a crystal meeting the following specifications be used.

Resonant Frequency .... 20 MHz
Tolerance .... ± 0.001% at 25°C
Stability .... ± 0.005% at 0°C to 70°C
Type .... AT CUT
Circuit .... Series or Parallel Resonance

For best operation, the total crystal capacitance load should not exceed 20 pF. An external 20 MHz oscillator may be applied to pin X1 while pin X2 is left floating.

(2) Manchester Encoder

This block converts the NRZ data to the Manchester data. It begins operation when the TXE input pin goes high. For the duration of TXE remaining high, the transmitted data (TXD) is encoded for the transmit driver pair (TX±). TXD must be valid on the rising edge of the transmit clock (TXC). Transmission ends when TXE goes low. The last transition is always positive.

The differential transmit pair from the secondary of the isolation transformer drives up to 50 meters of twisted pair

AUI cable. These outputs are source followers which require two 270 ohms pull-down resistors to ground.

The 83C91 allows both half-step and full-step to be compatible with Ethernet I and IEEE 802.3. With the SEL pin low (for Ethernet I), TX+ is positive with respect to TX– during idle; with SEL high (for IEEE 802.3), TX+ and TX– are equal in the idle state.

(3) Manchester Decoder

The decoder consists of a slicer circuit and a PLL circuit to recover the receiver clock and data. The differential input must be externally terminated with two 39 ohms resistors connected in series if the standard 78 Ohms transceiver drop cable is used; in thin Ethernet applications these resistors are optional.

To prevent noise from false triggering the decoder, a squelch circuit at the input rejects signals with pulse width less than 30 ns at –300 mV, or signals with level less than –175 mV. Signals more negative than –300 mV and a duration greater than 30 ns are decoded. Once the input signal exceeds the squelch requirements, carrier sense (CRS) is asserted. Receive data (RXD) and receive clock (RXC) become valid typically within 5 bit times. The 83C91 may tolerate bit jitter up to 20 ns in the received data. The decoder detects the end of a frame when no more midbit transitions are detected. Within 1.5 bit times after the last bit, CRS is deasserted. Receive clock stays active for 5 more bit times after CRS goes low to guarantee the receive timings of the 83C90 EDLC.

Absolute Maximum Ratings

Supply Voltage V_{CC} .... –0.5 to 7V
DC Input Voltage .... 5V to V_{CC} –0.5V
Differential Input Voltage .... –5.5 to 16V
Differential Output Voltage .... 0V to 16V
Operating Temperature .... 0°C to 70°C
Storage Temperature .... –50°C to 150°C

(4) Collision Detector

A transceiver detects collision on the network and generates a 10 MHz signal at the CD± input. When these inputs are over the squelch requirements (same as the receiver/decoder), the 83C91 translates the 10 MHz signal to an active high level (COL) for the controller.

(5) Loopback Function

When the loopback input (LBK) is asserted high, the 83C91 redirects its transmitted data back into its receive path. This feature provides a convenient method for testing both chip and system level integrity. The transmit driver and receive input circuit are disabled in loopback mode.

*Comments
Stresses above those listed under * Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V = 5%, T_A = 0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Units
Digital Interface Pins (COL, RXD, CRS, RXC, SEL, LBK, TXD, TXE, TEST, X1 and X2)					
X1 Input High Voltage	V_{IHX}	X1 is connected to an oscillator, and X2 is floating.	2.4		V
X1 Input Low Voltage	V_{ILX}	X1 is connected to an oscillator, and X2 is floating.		0.8	V
X1 Input Current	I_{OSC}	X1 is connected to an oscillator and X2 is floating. V_{IN} = V_{CC} or GND	–2	+2	mA

DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Max.	Units
Input High Voltage	V_{IH}		2.0		V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage	V_{IN}	$V_{IN} = V_{CC}$ or GND	–1	1	µA
Output High Voltage	V_{OH}	I_{OH} = 2 mA (TTL) I_{OH} = 20 µA (CMOS)	3.5 V_{CC} – 0.1		V V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA (TTL) I_{OL} = 20 µA (CMOS)		0.4 0.1	V V
Operation V_{CC} Supply Current[1]	I_{CCO}	10 Mbit/Sec		70	mA
Stand By V_{CC} Supply Current [2]	I_{CCS}	10 Mbit/sec		60	mA
Differential Pins (TX+/TX–, RX+/RX–, CD+/CD–)					
Differential Output Voltage (TX±)	V_{OD}	78 ohm Termination, and 270 ohm from each to GND	+550	–1200	mV
Differential Output Voltage Imbalance (TX±)	V_{OB}	78 ohm Termination, and 270 ohm from each to GND		40	mV
Undershoot Voltage (TX±)	V_U	78 ohm Termination, and 270 ohm from each to GND		100	mV
Differential Squelch Threshold (RX± and CD±)	V_{DS}		–175	–300	mV
Differential Input Common Mode Voltage (RX± and CD±)[3]	V_{CM}		0	5.5	V

Notes:

1. This measurement was made while the 83C91 was undergoing transmission, reception, and collision. The value was not measurement instantaneously, but averaged over a span of several milliseconds.
2. This measurement was made while the 83C91 was sitting ilde with TXE low. Also this value was measured as note 1.

MANCHESTER CODE CONVERTERS

AC Electrical Characteristics

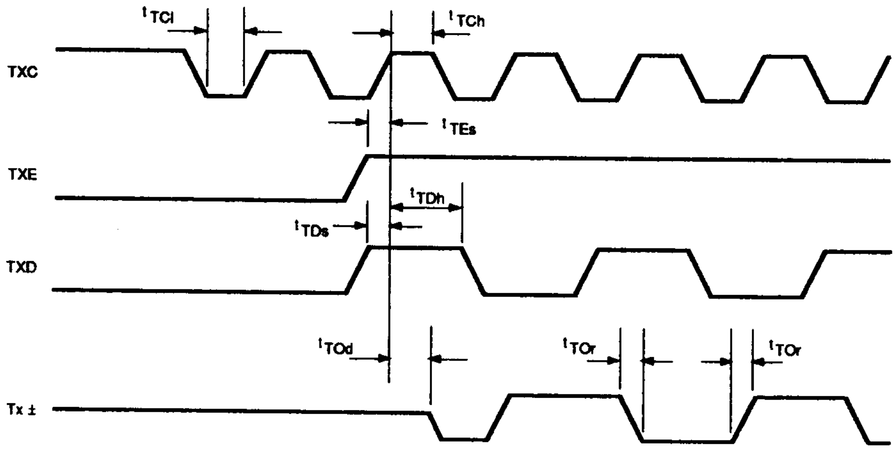
Oscillator Specifications

Parameter	Symbol	Min.	Max.	Units
X1 to Transmit Clock High	T_{XTH}	5		ns
X1 to Transmiit Clock Low	T_{XTL}	5		ns

Transmit Specifications (Start of Packet)

Parameter	Symbol	Min.	Max.	Units
Transmit Clock High Time	T_{TCh}	40	60	ns
Transmit Clock Low Time	T_{TCl}	40		ns
Transmit Clock Cycle Time	T_{TCc}	99.99	100.01	ns
Trasnmit Clock Rise Time (20% to 80%)	T_{TCr}		8	ns
Transmit Clock Fall Time (80% to 20%)	T_{TCf}		8	ns
Transmit Enable Setup Time to Rising Edge of TXC	T_{TEs}	30		ns
Transmit Data Setup Time from Rising Edge of TXC	T_{TDs}	30		ns
Transmit Data Hold Time form Rising Edge of TXC	T_{TDh}	0		ns
Transmit Output Delay Time from Rising Edge of TXC	T_{TOd}		65	ns
Transmit Output Rise Time (20% to 80%)	T_{TOr}		8	ns
Transmit Output Fall Time (80% to 20%)	T_{TOf}		8	ns
Transmit Output Jitter	T_{TOj}		2	ns

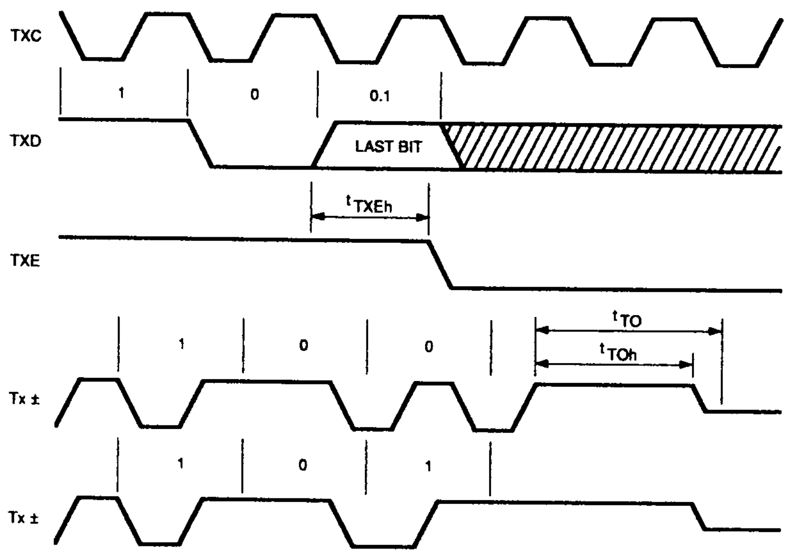
Transmit Start Timing



Transmit Specifications (End of Packet)

Parameter	Symbol	Min.	Max.	Units
Transmit Enable Hold Time from Rising Edge of TXC	T_{TXEh}	0		ns
Transmit Output High Before Idle (Half Step)	T_{TOh}	200		ns
Transmit Output Idle Time (Half Step)	T_{TOi}		8000	ns

Transmit End Timing

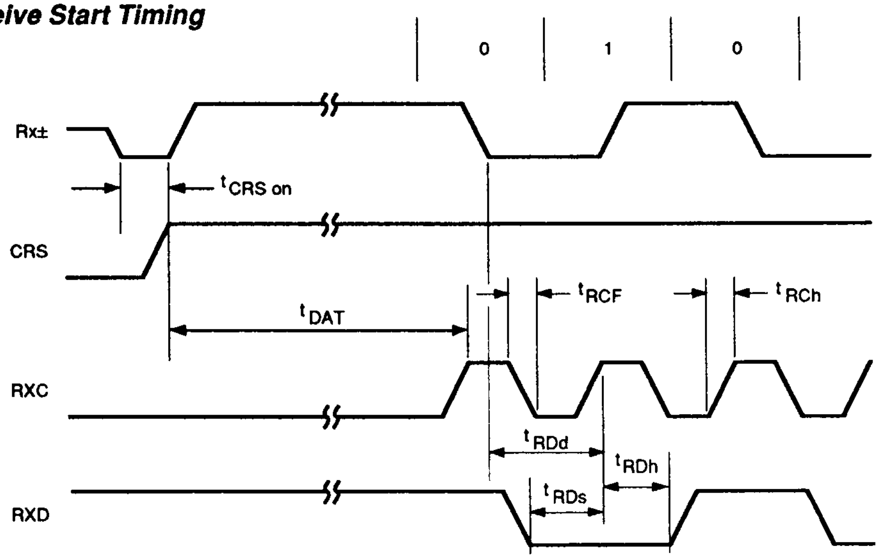


Receive Specifications (Start of Packet)

Parameter	Symbol	Min.	Max.	Units
Receive Clock Duty Cycle	T_{RCd}	40	60	%
Receive Clock Rise Time (20% to 80%)	T_{RCr}		8	ns
Receive Clock Fall Time (80% to 20%)	T_{RCf}		8	ns
Receive Data Output Delay	T_{RDd}		160	ns
Receive Data Output Setup from Rising Edge of RXC	T_{RDs}	40		ns
Receive Data Output Hold from Rising Edge of RXC	T_{RDh}	40		ns
Carrier Sense Turn On Delay	T_{CRSon}		80	ns
Decoder Acquisition Time	T_{DAT}		700	ns
Differential Input Rejection Pulse [1]	T_{DREJ}	8	40	ns

Note: 1. This parameter was characterized with a differential input of –300 mV on the receive pair inputs.

Receive Start Timing

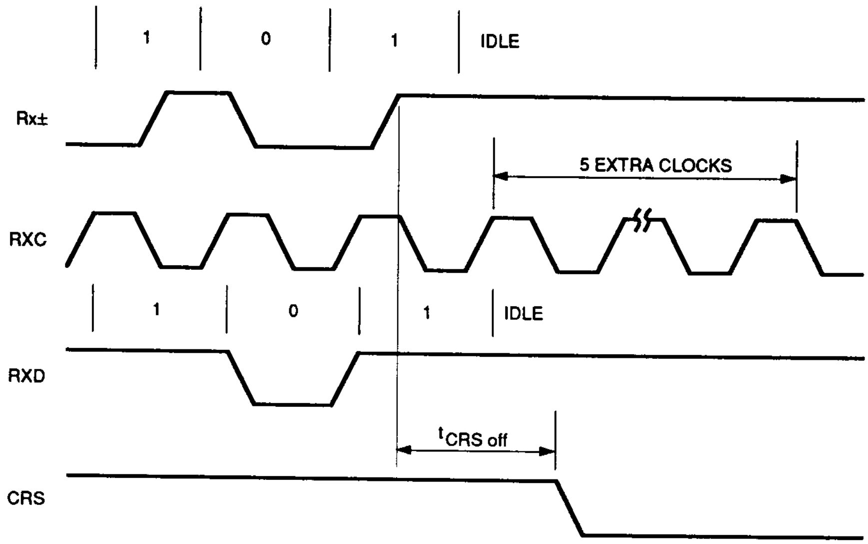


Receive Specifications (End of Packet)

Parameter	Symbol	Min.	Max.	Units
Carrier Sense Turn off Delay [1]	T_{CRSoff}		160	ns
Minimum Number of RXCs After CRS Low [2]	T_{RXCh}	5		Bit Times

Notes:
1. When CRS goes low, it will go low a minimum of 2 receive clocks.
2. The 83C90 EDLC requires a minimum of 5 receive clocks after CRS goes low to function properly.

Receive End Timing

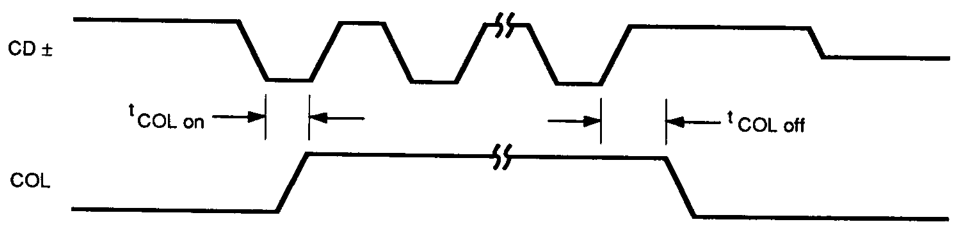


Collision Specifications

Parameter	Symbol	Min.	Max.	Units
Collision Turn on Delay	T_{COLon}		60	ns
Collision Turn off Delay	T_{COLoff}		350	ns
Differential Input Rejection Pulse[1]	T_{DREJ}	8	40	ns

Note: 1. This parameter was characterized with a differential input of –300 mV on the receive pair inputs.

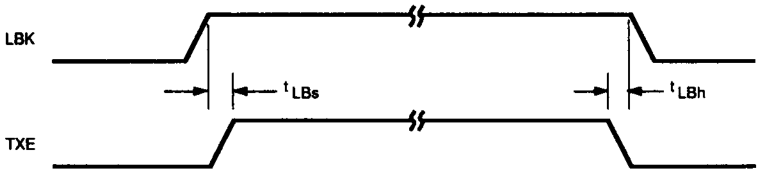
Collision Timing



Loopback Specifications

Parameter	Symbol	Min.	Max.	Units
Loopback Setup Time	T_{LBs}	50		ns
Loopback Hold Time	T_{LBh}	100		ns

Loopback Timing



AC Timing Test Conditions

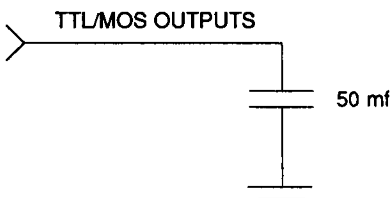
All specifications are valid only if the mandatory isolation is employed and all differential signals are taken to be at the AUI side of the pulse transformer.

Input pulse level .... GND to 3V

Input rise and fall time .... 5 ns

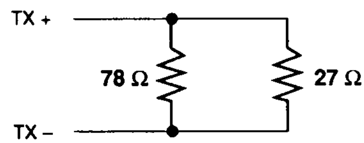
Input and output reference level (TTL/MOS) 1.3V

Input and output reference level (Diff.) .... 50% of the differential

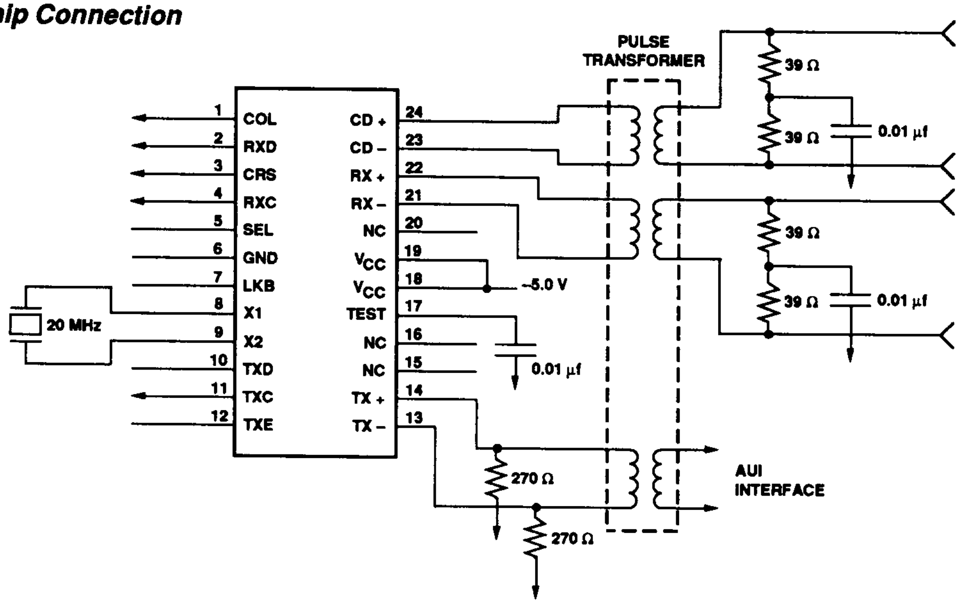


Capacitance $T_A = 25°C$, f = 1 MHz

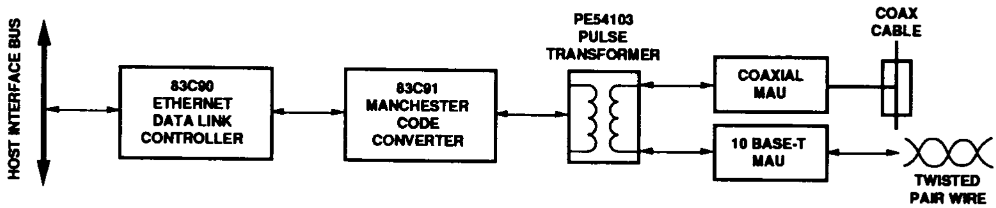
Parameter	Symbol	Typ.	Units
Input Capacitance	C_{in}	7	pF
Output Capacitance	C_{out}	7	pF



Appication Circuit
Chip Connection



System Application



Ordering Information

P Q 83C91

PACKAGE TYPE
P = Plastic Dip
N = Plastic Leaded Chip Carrier

TEMPERATURE RANGE
Q = 0° to 70°

PART TYPE
83C91 = Manchester Code Converter