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LCD CONTROLLER DRIVER

S-4562A

The S-4562A is a 17 or 33 common, 60 segment output character LCD driver with built-in interfaces for serial and 8-bit CPUs. The S-4562A incorporates CGROM, making character display possible. It displays this independently of the CPU through the use of an internal oscillating circuit or clock input. It has a wide variety of command instructions which minimize the load of the CPU. It also features a wide voltage range, low power consumption, and a power save function, making the S-4562A a suitable display for system applications in portable electronics.

■ Features

- Display Area
  5-dot font
  12 columns 4 lines (+4 columns) ,
  24 columns 2 lines (+8 columns) ,
  12 columns 2 lines (+4 columns)
  6-dot font
  10 columns 4 lines (+6 columns) ,
  20 columns 2 lines (+12 columns) ,
  10 columns 2 lines (+6 columns)
  Values in parentheses indicate the number of columns outside the display area.
- Icon Display
  Max. 60 icons
  Icons can be displayed upper and lower panel.
- Fonts; Both 5-dot font/6-dot font display are possible.
- Interface
  8-bit high-speed CPU interface
  Serial interface
- Driver Output
  60 segments
  16 common+ Icon common: Command Setting
  32 common+ Icon common: Default
- Character Generator ROM (CGROM)
  9600 bits Character font 5×7 bits 240 characters
- Character Generator RAM (CGRAM)
  8 character×5×8=320 bits
- Display Data RAM (DDRAM)
  4 lines×16 characters=4×16×8=512 bits
  (4 characters are outside the display area)
- Display Clock
  Either internal CR oscillating circuit or external clock input is available:
  CR oscillation: 1/17 duty cycle=31 kHz,
  1/33 duty cycle=60 kHz
- Duty Cycle
  1/17: Command Setting
  1/33: Default
- Internal LCD Bias Voltage Generator
  Internal bias resistor: Command selection
  1/6.7, 1/5, or 1/4 bias
  External bias resistor: Free setting of 1/2 bias or more
- Interface Command
  Display Clear, Cursor Home, Display ON/OFF, Display Character Blink, Cursor Shift, Display Shift, Cursor ON/OFF
- Expanded Interface
  Contrast Adjustment, Smooth Scrolling Control, Icon Control, Icon Blinking, Bias Resistor Selection, Change of Number of Display Columns, Power Save, Only Icon Display, Boosting Frequency Selection
- Internal Booster Circuit: Dual/Triple Booster
- Power Supply voltage range
  Logic Power: -2.4 V to -5.5 V
  LCD Drive Power: -2.7 V to -11.0 V
- Low Current Consumption: T.B.D. max
  Approximately 0 μA (during power save operation)
- Shipment Form: Gold bump bare chip, TCP

■ Block Diagram

1. Block Overview

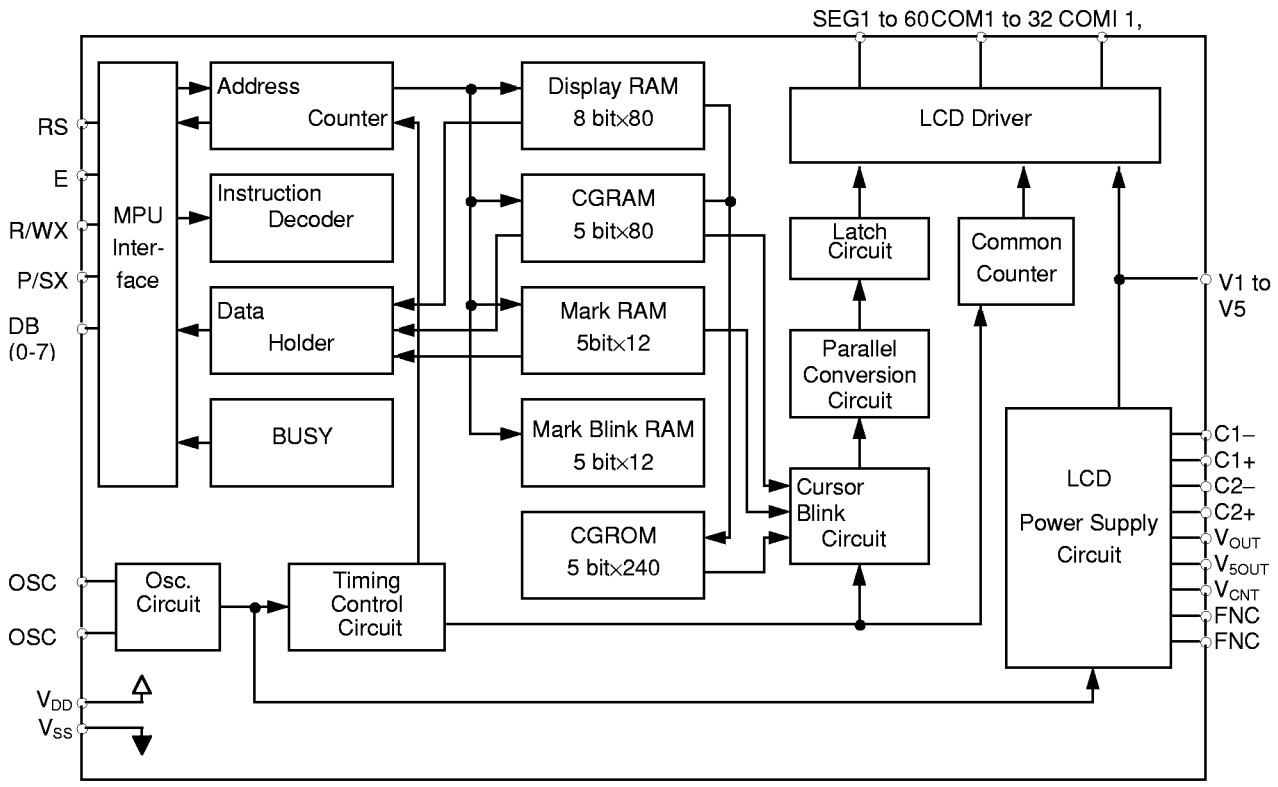


Figure 1

2. LCD Power Supply Circuit

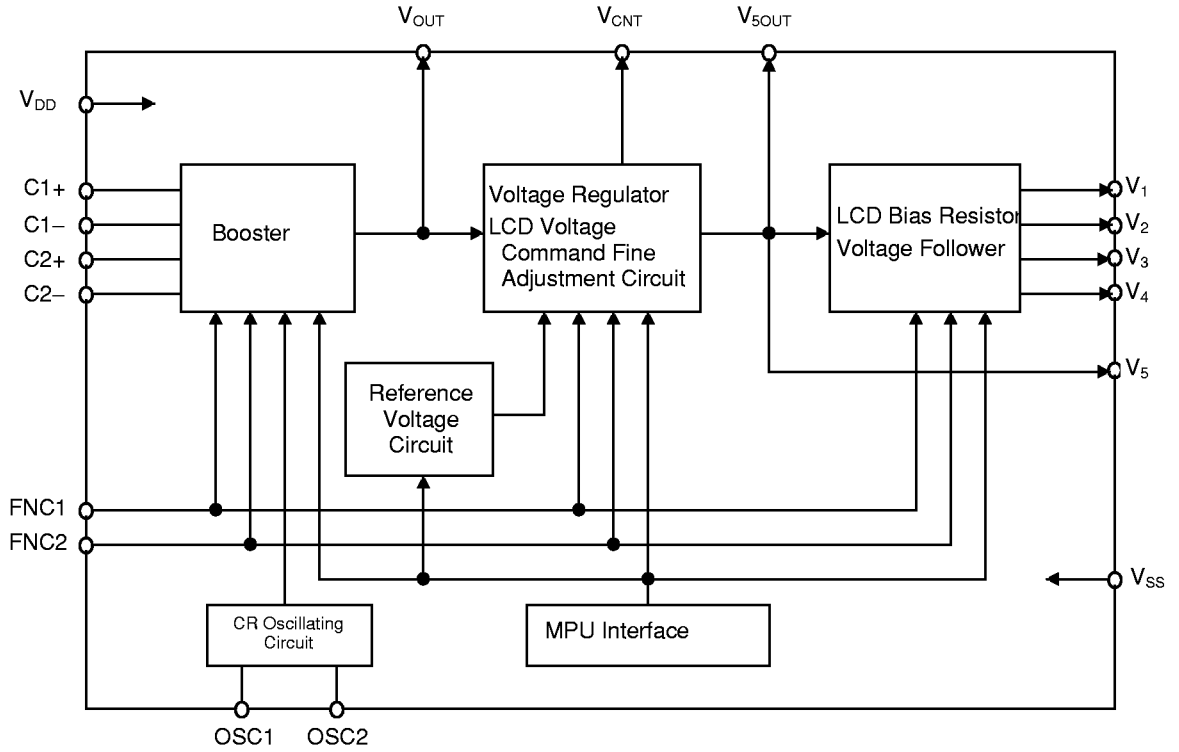


Figure 2

■ INSTRUCTION LIST

1. Normal Instructions

Table 1

Command	Code										Functions	Execution Time VDD=3V
	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
****	0	0	0	0	0	0	0	0	0	0		
Display Clear	0	0	0	0	0	0	0	0	0	0	Writes the space code in the entire DDRAM.	OSC 67 Clock
Cursor Home	0	0	0	0	0	0	0	0	1	CH	CH: 1/0= Cursor Return/Cursor Home	1μsec or less
Entry Mode	0	0	0	0	0	0	0	1	ID	S	ID:1/0= Address Counter Increment/Decrement S: 1/0= Display Shift during DDRAM write	1μsec or less
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D: 1/0= Display ON/OFF C: 1/0= Cursor Display ON/OFF B: 1/0= Cursor Position Blink ON/OFF	1μsec or less
Cursor Display Shift	0	0	0	0	0	1	SC	RL	-	-	SC: 1/0= Whole Display Shift/Cursor Shift RL: 1/0= Cursor, Display Right /Left Shift	1μsec or less
Function Set	0	0	0	0	1	H	N	MS	DT	TC	H: 2 lines 12 columns select N: 2 lines 24 columns /4 lines 12 columns MS: 1/0= Expanded/Normal Interface DT: 1/0= 6-dot / 5-dot font TC: 1/0= Zig-Zag/Normal Common Output	1μsec or less
CGRAM Address	0	0	0	1	CGRAM Address						CGRAM Address Setting	1μsec or less
DDRAM Address	0	0	1	-	DDRAM Address						DDRAM Address Setting	1μsec or less
BUSY Address Read	0	1	BF	Address Counter							BF:BUSY Output Address Counter Setting	1μsec or less
Data Write	1	0	Write Data								Write Data	1μsec or less
Data Read	1	1	Data Read								Data Read	1μsec or less

-:don't care

2. Expanded Instruction list

Table 3

Command	Code										Functions	Execution Time VDD=3V
	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Power Save Setting	0	0	0	0	0	0	-	-	-	PS	PS : 1/0= Power Save Operation/Normal Display	1µsec or less
Icon Only Display, Boosting Frequency Selection	0	0	0	0	0	1	-	MD	DC1	DC0	MD : 1/0= Icon Only Display/Normal Entire Display DC1, DC0: Boosting Frequency Selection	1µsec or less
Bias Select	0	0	0	1	0	0	-	-	BS1	BS0	BS1 BS0 0 0 1/6.7 Bias 0 1 1/5 Bias 1 0 1/4 Bias 1 1 Bias/External Setting	1µsec or less
Blink Select	0	0	0	1	0	1	-	-	BK1	BK0	BK1 BK0 0 0 Black Blinking 0 1 White Blinking 1 0 Cursor Blinking 1 1 Black/White Inverse Blinking	1µsec or less
Smooth Scroll Dot Shift	0	0	1	0	0	0	-	Dot Shift Amount			Dot Shift Amount : Setting and Operation of the Dot Shift Amount in the Smooth Scroll Select lines.	1µsec or less
Scroll Line Setting	0	0	1	0	0	1	L4	L3	L2	L1	L1: Selects the first line to Smooth Scroll line. L2: Select the second line to the Smooth Scroll line. L3: Select the third line to the Smooth Scroll line. L4: Select the forth line to the Smooth Scroll line.	1µsec or less
Smooth Scroll Character Shift	0	0	1	0	1	Character Shift Amount					Character Shift Amount: Setting and Operation of the Character Shift Amount in the Smooth Scroll Select lines.	1µsec or less
Icon RAM Address Setting	0	0	1	1	0	0	Icon RAM Address				Icon RAM Address Assignment	1µsec or less
Icon Blinking RAM Address Setting	0	0	1	1	0	1	Icon Blinking RAM Address				Icon Blinking RAM Address Assignment/ Sets the mark to blink.	1µsec or less
Contrast Adjustment	0	0	1	1	1	0	Contrast Amount				LCD Contrast Adjustment Data Setting	1µsec or less
Reference Volatage Temparature Coefficient Selection	0	0	1	1	1	1	-	-	-	DV0	DV0 0 -0.13%/ C, 1.6V 1 +0.01%/ C, 2.2V	1µsec or less
Function Set	0	0	0	0	1	H	N	MS	DT	TC	H: 1/0= 2 lines 12 columns Select/ N Valid N: 1/0= 2 lines 24 columns /4 lines 12 columns MS: 1/0= Expanded / Normal Instruction DT : 1/0=6-dot font/5-dot font TC : 1/0=Zig-Zag / Normal Common Output	1µsec or less
BUSY Address Read	0	1	BF	Address Counter							BF : BUSY Output Address Counter Setting	1µsec or less
Data Write	1	1	Write Data								Write Data	1µsec or less
Data Read	1	1	Read Data								Read Data	1µsec or less

-:don't care

IMPORTANT: Commands for the Function Set, BUSY Address Read, Data Write, and Data Read are common to Normal and Expanded Instructions.

■ Function Explanation

1. Interface

Two interfaces for serial and 8-bit parallel connections, which can be changed by the P/SX terminal, are built in. The CPU interfaces with instruction code and several kinds of data via an instruction decoder and a data holder.
Data is read from memory via the Data Holder. Through the memory's Address Set Command, the contents of the memory are read at one time into the Data Holder, and output through the Read Instruction. Then, the next data is read into the Data Holder.
Parallel interface and serial interface execute all instructions within the ENABLE CYCLE or the CLOCK CYCLE specified according to timing characteristics. Because BUSY is cleared within the CYCLE, the execution of successive instructions is possible without having to confirm BUSY.

1.1 Parallel Interface

Parallel interface is engaged when the P/SX terminal is "H" Connect the P/SX terminal to VDD. The reading of instruction is carried out at the falling edge of ENABLE (E), and the reading of data and of addresses is carried out when ENABLE is "H"

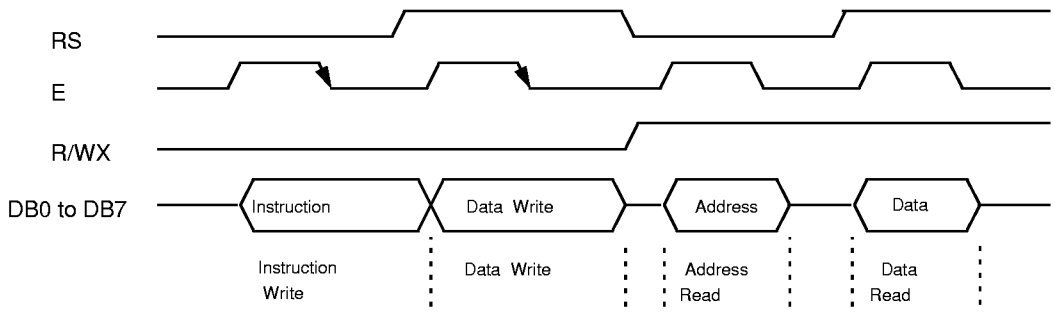


Figure 3

1.2 Serial Interface

Serial interface is engaged when the P/SX terminal is "L" The instruction code is read at the rising edge of Serial Lock (SCLK). Serial data is input in numeric order from DB0 through DB7. The instruction code is the same as that of the parallel data. Connect the P/SX terminal to VSS. Set the R/WX terminal to OPEN.

P/SX: "L" Serial Interface Operation/Connect it to VSS.
RS: Write in the "L"Instruction Register
Write in the "H" Data Register.
E: "L" Active
DB0: Serial Data Input Terminal (SDI)
DB1: Serial Clock Input Terminal (SCLK)
DB2 to DB7: OPEN
R/WX: OPEN

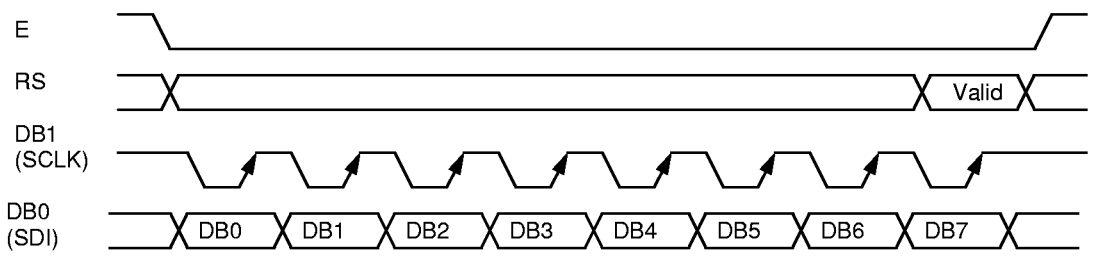


Figure 4

•œ 1 Line 24 Character Display

•œ No Display Shift

	COM1 to COM8												COM17 to COM24												Rear Character								
Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									DDRAM
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	Address

•œ Display Left Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									DDRAM
1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00	Address

•œ Display Right Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									DDRAM
1st line	1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	Address

•œ 2 Line 24 Character Display

•œ No Display Shift

	COM1 to COM16												COM17 to COM32												Rear Character								
Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	DDRAM
2nd line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	Address

•œ Display Left Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									
1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00	DDRAM
2nd line	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	20	Address

•œ Display Right Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24									
1st line	1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	DDRAM
2nd line	3F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	Address

•œ 4 Line 12 Character Display

•œ No Display Shift

	COM1 to COM32												Rear Character				
Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	DDRAM
3rd line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	Address
4th line	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	

•œ Display Left Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00	
2nd line	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	DDRAM
3rd line	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	20	Address
4th line	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	30	

•œ Display Right Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	
2nd line	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	DDRAM
3rd line	2F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	Address
4th line	3F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	

•œ 2 Line 12 Character Display

•œ No Display Shift

	COM1 to COM16 and COM17 to COM32												Rear Character				
Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DDRAM
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	Address

•œ Display Left Shift

Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00	DDRAM
2nd line	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	Address

•œ Display Right Shift

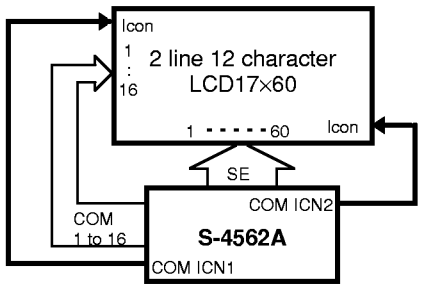
Position	1	2	3	4	5	6	7	8	9	10	11	12					
1st line	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DDRAM
2nd line	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	Address

DDRAM Addresses and Positions

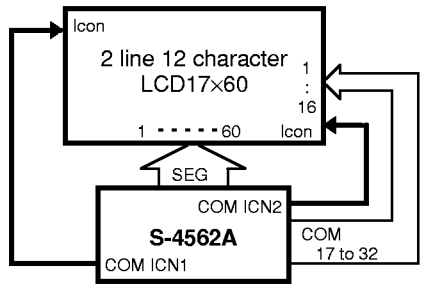
■ EXAMPLES OF CONNECTION TO LCD PANEL

1. 2-line 12-character 1/17 duty cycle 17×60 panel
In case of the 2- line 12-character display, common output of chip's right and left side is the same phase.

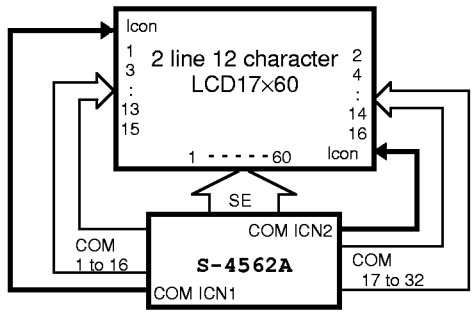
• Using COM1 to 16



• Using COM17 to 32



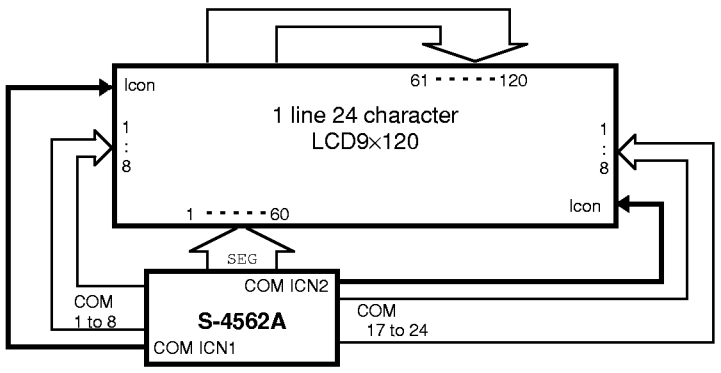
Odd numbered commons



Even numbered commons

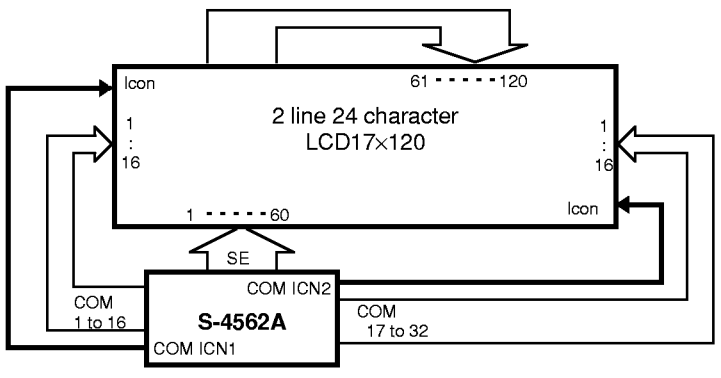
2. 1- line 24- character 1/33 duty cycle 9×120 panel

• Normal Common Output



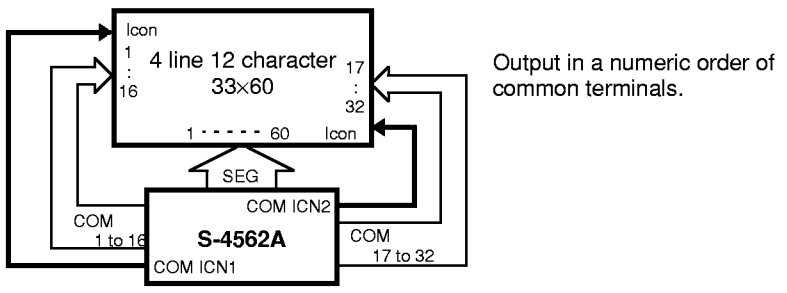
3. 2- line 24- character 1/33 duty cycle 17×120 panel

• Normal Common Output



4. 4- line 12- character 1/33 duty cycle 33×60 panel

- Normal Common Output



- Common Right and Left Alternate Output

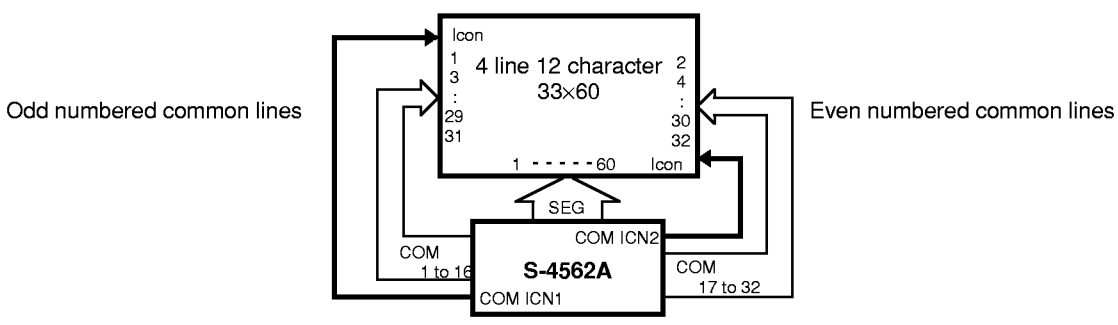


Figure 5 Connection to the LCD panel

■ DC Characteristics

1. ELECTRICAL CHARACTERISTICS

Table 3

(Unless otherwise specified: V_{DD}=0 V, V_{SS}=–5.0±0.5 V, Ta=–30 to 85 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Op. Voltage	V_{SS}		–5.5	-	–2.4	V	Note1
LCD Drive Voltage	V_5	When using an external LCD power supply	–11.0	-	–3.5	V	Note2
	V_1, V_2		V_5	-	V_{DD}	V	
	V_3, V_4						
High Level Input Voltage	V_{IH}	V_{SS}=-2.4 to -4.5 V	0.2×V_{SS}	-	V_{DD}	V	Note3
		V_{SS}=-5.0±0.5 V	0.3×V_{SS}	-	V_{DD}		
Low Level Input Voltage	V_{IL}	V_{SS}=-2.4 to -4.5 V	V_{SS}	-	0.8×V_{SS}	V	Note3
		V_{SS}=-5.0±0.5 V	V_{SS}	-	0.7×V_{SS}		
High Level Output Voltage	V_{OH1}	I_{OH}=-0.5mA, V_{SS}=-2.4 to -4.5V	0.2×V_{SS}	-	-	V	Note4
		I_{OH}=-1.0 mA	0.2×V_{SS}	-	-		
	V_{OH2}	I_{OH}=-50μA, V_{SS}=-2.4 to -4.5 V	0.2×V_{SS}	-	-	V	OSC_2
		I_{OH}=-120 μA	0.2×V_{SS}	-	-		
Low Level Output Voltage	V_{OL1}	I_{OL}=0.5mA, VSS=-2.4 to -4.5 V	-	-	0.8×V_{SS}	V	Note4
		I_{OL}=1.0mA	-	-	0.8×V_{SS}		
	V_{OL2}	I_{OL}=50μA VSS=-2.4 to -4.5 V	-	-	0.8×V_{SS}	V	OSC_2
		I_{OL}=120μA	-	-	0.8×V_{SS}		
Input Leak Current	I_{ILEAK}	V_{SS}=-2.4 to -5.5 V	–1.0	-	1.0	μA	Note5
Output Leak Current	I_{OLEAK}	V_{SS}=-2.4 to -5.5 V	–3.0	-	3.0	μA	Note6
LCD Driver ON Resistance	R_{ON}	Ta=25 °C, V5=-8.0 V 1/5 Bias	-	3.0	5.0	kΩ	Note7
Current Consumption at Stationary Status	I_S		-	0.05	5.0	μA	Note8
Current Consumption During Operation	I_{SS}	When using an external LCD power During display V5=-8.0 V Rf=** Ω	-	T.B.D	T.B.D	μA	Note9
Oscillating Frequency	f_{OSC}	R_f=** MΩ V_{SS}=–3.0 V	T.B.D	T.B.D	T.B.D	kHz	Note10
		R_f=** MΩ V_{SS}=–5.0 V	T.B.D	60	T.B.D		
Wait Time	t_R	fosc=60KHz	T.B.D	-	-	μs	Note11

2. Electrical Characteristics of LCD Power Supply Circuit

Table 4
(Unless otherwise specified, VDD=0 V, VSS=-2.4 to -5.5V, Ta=-30 to 85 °C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Note
Op. Voltage	V_{SS}			–5.5	-	–2.4	V	Note12
Boosting Output Voltage	V_5	Triple Boost:Up to V_{SS}=-3.6 V Dual Boost: Up to V_{SS}=-5.5V		–11.0	-		V	
LCD Power Supply Circuit Op. Voltage	V_{IH}	1/4 Bias		–11.0	-	-4.0		
		1/5 Bias		–11.0	-	-4.5	V	Note13
		1/6.7 Bias		–11.0	-	-5.5		
LCD Drive Circuit Op. Voltage	V_{LCD}			–11.0	-	-2.7	V	Note14
Internal LCD Power Supply Circuit Current Consumption	I_{SSL}	V_{OUT}=-10.0 V Double Boost V_{SS}=-5.0 V V5=-8.0 V 1/5 Bias Oscillating Frequency=60 kHz			T.B.D	T.B.D	µA	Note15
LCD Driver Current Consumption	IV_5	V5=-8.0 V 1/5 Bias			T.B.D	T.B.D	µA	Note16
Standard Voltage	V_{REF}	Ta=25 °C	+0.01%/ °C	-2.4	-2.2	-2.0	V	Note17
			-0.13%/ °C	-1.8	-1.6	-1.4		

3. References

Table 5 References

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25 °C	-	5	8	pF	Note 3

Note 1 Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
If you change the level of the supply voltage intentionally, a malfunction may occur. NEVER CHANGE the level of the supply voltage.

Note 2 $V_{DD} \geq V1, V2, V3, V4 \geq V5$. There is no limitation for determining the voltage level of V1, V2, V3, and V4.

Note 3 Pins RS, E, R/WX, P/S, OSC1, FNC1 and FNC2.
Pins DB0 to DB7 during display data write and command input.
Fully swing the levels V_{IH} and V_{IL} of the input signal within the range of power supply voltage so that the state is $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$. When the level of V_{IH} and V_{IL} is the middle level of the supply voltage, the through current flowing through the input pin and the current consumption may be increased.

Note 4 Pin s DB0 to DB7 during read.

Note 5 Pins RS, E, R/WX, P/S, OSC1, FNC1 and FNC2.

Note 6 Pins D0 to D7 during write and high-impedance.

Note 7 ON resistance between LCD drive output pins (SEG1 to SEG60, COM1 to 31, COMICN1, and 2) and LCD drive bias voltage pins (V1, V2, V3, V4). Using the external LCD power supply, measure the resistance at a 0.1-V difference from the LCD drive output pin after applying 1/2 voltage of V5 to the LCD drive bias voltage pin.

Note 8 Power save state.

Note 9 Shows the current consumption during display including CR oscillation.
It does not include the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the external LCD power supply. The LCD drive output pin is no load. The current consumed by the LCD panel and wiring capacitor is not included. Measure it without access from the MPU. The current consumed by the external LCD power supply and external bias resistor and other is not included.

Note 10 For a 2-line x 12-column display, set the oscillating frequency to 31 kHz when Rf=**kΩ. Refer to the graph showing the oscillating frequency vs Rf dependency.

Note 11 Shows the wait time from when the power voltage rises to 80% of the specified voltage to when the command input is available. This is applicable when fosc = 60 kHz and is proportional to the reciprocal of fosc.

Note 12 The operating voltage range of the booster.

Note 13 Shows the operating voltage range of the LCD voltage adjustment circuit, voltage follower, and LCD bias resistor. The operating voltage range differs depending upon each bias setting value. To adjust V5 with the LCD voltage adjustment circuit, it is necessary to set the voltage within the bias voltage.

Note 14 The operating voltage range of the LCD driver after the voltage follower functions. Also, it shows the voltage range of V1 to V5 supplied from the external LCD power supply circuit.

Note 15 Shows the value of the current consumed by the booster, LCD voltage adjustment circuit, voltage follower, LCD bias resistor. It does not include the value IRREG=V5/(R1+R2+R3) of the current flowing through external resistors R1, R2, and R3. Current consumption of the IC during display is ISSL+IDD1+IRREG.

Note 16 Shows the value of the current consumed by the voltage follower and LCD driver.
The built-in circuit uses the external power supply to generate the bias voltage when the booster and LCD power supply voltage adjustment circuits stop.
Current consumption of the IC during display is IVF+IDD1.
When using the external power supply, stop the built-in LCD power supply circuit. Shorting of the internal and external power supply can damage the IC.

Note 17 The reference voltage differs depending upon the reference voltage temperature coefficient selected with the corresponding command. V_{DD}=0V