TOSHIBA BiCD Integrated Circuit Silicon Monolithic

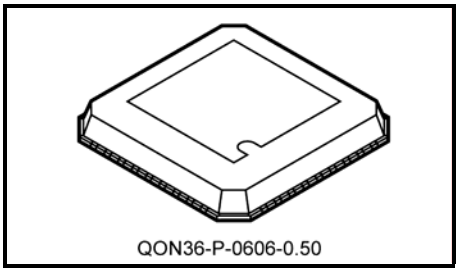
TB6609FLG

DC and Stepping Motor Driver IC

The TB6609FLG is a DC motor driver IC using LDMOS output transistors with low ON-resistance.

The TB6609FLG incorporates two PWM-constant-current H-bridge drivers and four direct-PWM-controlled H-bridge drivers. The TB6609FLG is best suited to control various lens actuators in digital still cameras.

The three-wire serial interface provides control over the drivers, thus reducing the number of lines required for interfacing with the control IC.



Weight: 0.08 g (typ.)

Features

- Motor power supply voltage: $V_M \leq 15$ V (max)
- Control power supply voltage: V_{CC} = 3 to 6 V
- Output current: $I_{OUT} \leq 0.8$ A (max)
- Complementary P- and N-channel LDMOS output transistors
- Output ON-resistance: Ron (upper and lower sum) = 1.5 Ω (typ.: VM = 5V)

Channel A, B, C, and D

- Four H-bridge drivers (channel A, B, C, and D) for direct PWM control.
  (Capable of controlling up to two 2-phase bipolar stepping motors or four actuators.)

Channel E

- High-speed PWM control at several hundred kHz
- Motor control method can be selected from the following two with the serial data inputs:
  1. Controls motor speed by using both a frequency-locked-loop (FLL) speed discriminator that compares the FG and typical speed, and an integrator (external constant number: C, R).
     (Typical speed = Between 100 Hz and 1650 Hz in 32 steps per 50 Hz.)
  2. Controls H-bridge by using a direct PWM input.
- One power switching transistor for optical encoder and two comparators which can change Vref and hysteresis.

Channel F

- PWM constant-current drivers
- Current ramp-up rate control for improving the dependency of a current ramp-up rate on supply voltage change at startup and also for improving its reproducibility.
  (Increases current in up to 32 steps by using the internal CLK, which is derived by dividing CLK by 1 to 32.)

Other Features

- Two 6-bit DACs provide reference values for each constant-current limiters
- Two comparators with a latch function for optical encoder (Vref can be set between 0.125 to 2 V in 16 steps.)
- Dedicated standby (power-save) pin
- Thermal shutdown (TSD)
- Under voltage lockout (UVLO): Resets and disables the internal circuitry when V_{CC} falls below 1.9 V (typ.)
- Small QON36 package (0.5-mm lead pitch)

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

The following conditions apply to solderability:

About solderability, following conditions were confirmed

- Solderability

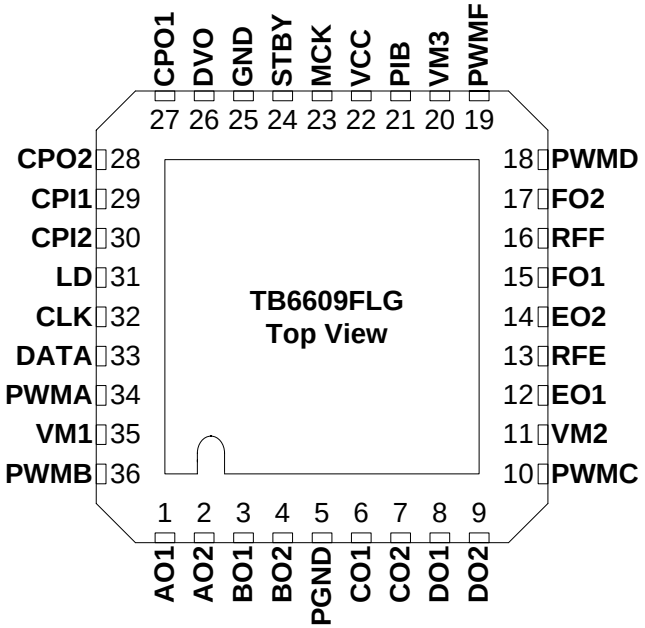
  (1) Use of Sn-37Pb solder Bath
  - · solder bath temperature: 230℃
  - · dipping time: 5 seconds
  - · the number of times: once
  - · use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - · solder bath temperature: 245℃
  - · dipping time: 5 seconds
  - · the number of times: once
  - · use of R-type flux

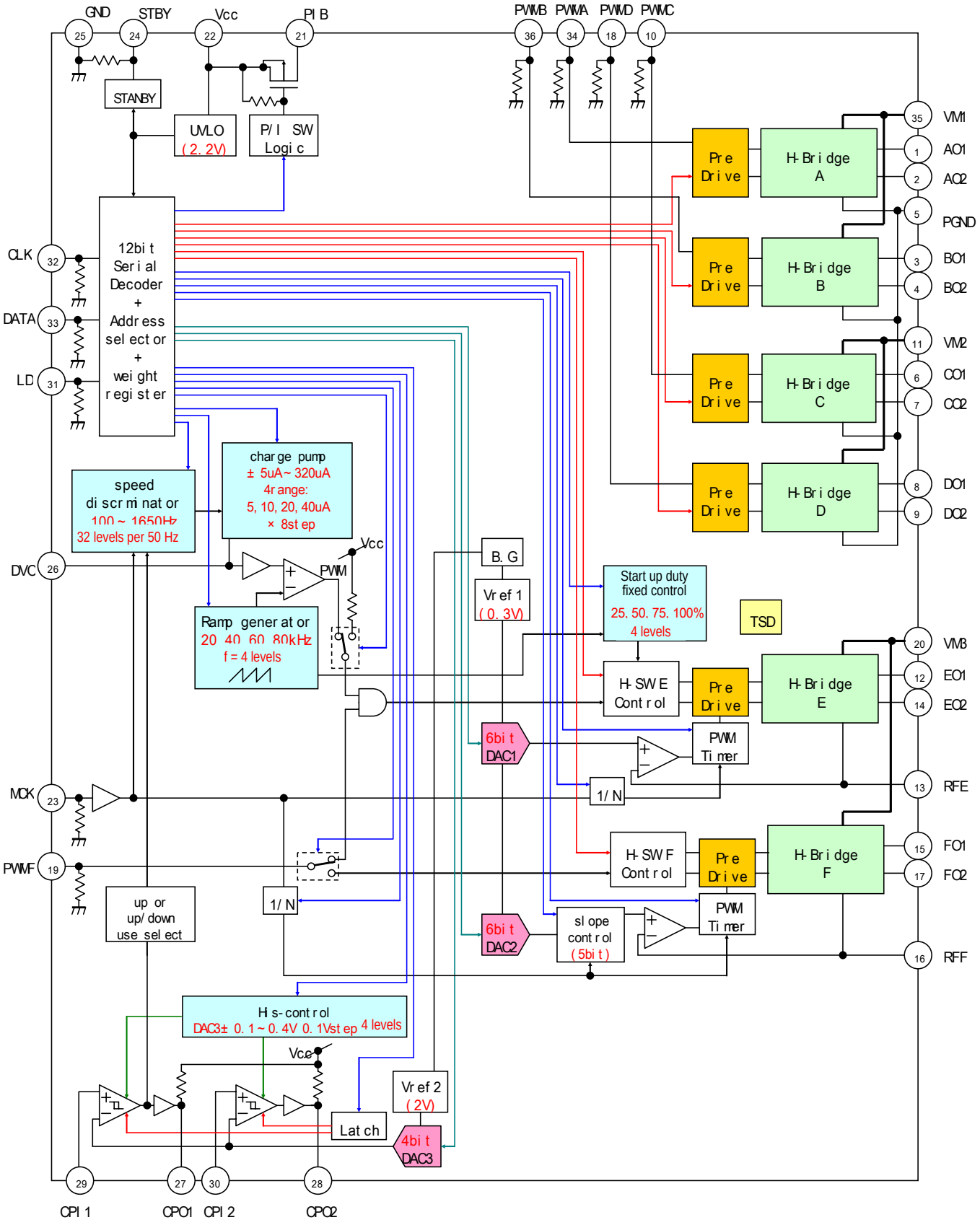
Pin description

No	Pin name	I/O	function	No	Pin name	I/O	function
1	AO1	O	Channel A output pin 1	19	PWMF	I	Input pin of PWM signal (Channel F)
2	AO2	O	Channel A output pin 2	20	VM3	-	Motor power supply pin 3
3	BO1	O	Channel B output pin 1	21	PIB	O	Sw output pin for optical encoder
4	BO2	O	Channel B output pin 2	22	VCC	-	Supply voltage pin
5	PGND	-	Ground pin for motor supply	23	MCK	I	Clock input pin for channel E and F
6	CO1	O	Channel C output pin 1	24	STBY	I	Input pin of standby signal
7	CO2	O	Channel C output pin 2	25	GND	-	Ground pin
8	DO1	O	Channel D output pin 1	26	DVO	-	Connecting pin of external integrator for channel E speed control
9	DO2	O	Channel D output pin 2	27	CPO1	O	Output pin of comparator 1 with latch for optical encoder
10	PWMC	I	Input pin of PWM signal (Channel C)	28	CPO2	O	Output pin of comparator 2 with latch for optical encoder
11	VM2	-	Motor power supply pin 2	29	CPI1	I	Input pin of comparator 1 with latch for optical encoder
12	EO1	O	Channel E output pin 1	30	CPI2	I	Input pin of comparator 2 with latch for optical encoder
13	RFE	-	Connecting pin of resistance for channel E current detection	31	LD	I	Input pin of serial data loading signal
14	EO2	O	Channel E output pin 2	32	CLK	I	Input pin of serial data clock signal
15	FO1	O	Channel F output pin 1	33	DATA	I	Input pin of serial data
16	RFF	-	Connecting pin of resistance for channel F current detection	34	PWMA	I	Input pin (Channel A) of PWM signal
17	FO2	O	Channel F output pin 2	35	VM1	-	Motor power supply pin 1
18	PWMD	I	Input pin of PWM signal (Channel D)	36	PWMB	I	Input pin (Channel B) of PWM signal

Pin assignment (Top view)



Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Remarks
Supply voltage		V_{CC}	6	V	V_{CC}
Motor supply voltage		V_M	15	V	V_M
Output voltage		V_{OUT}	-0.2 to 15	V	Channel. A to F
Output current	H-SW	I_{OUT}	0.8	A	
	PI SW Tr.	I_D	0.1		PIB
Input voltage		V_{IN}	−0.2 to 6	V	Control input pins
Power dissipation		P_D	0.6	W	IC only
			1.04		(Note)
Operating temperature		T_{opr}	−20 to 85	°C	
Storage temperature		T_{stg}	−55 to 150	°C	

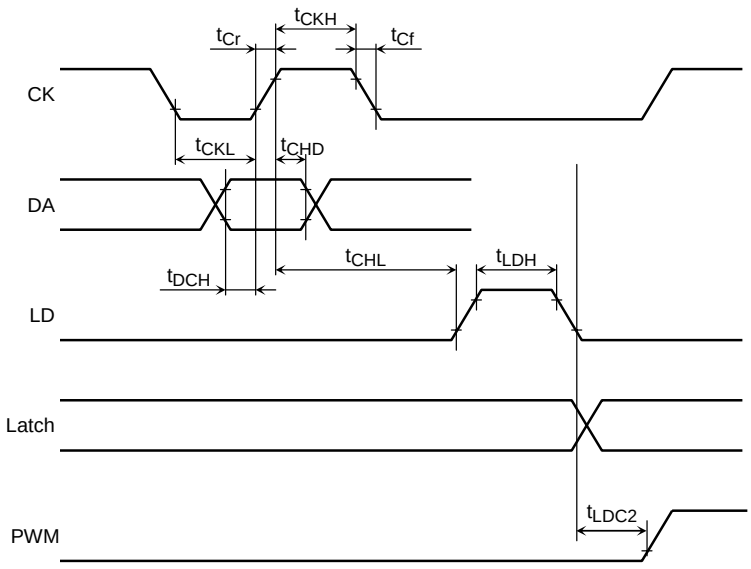
Note: When mounted on a glass epoxy single-sided PCB (size: 50 mm × 50 mm × 1.6 mm) with a 40% dissipating copper surface.

Operating Ranges (Ta = –20 to 85°C)

Characteristics		Symbol	Rating			Unit	Remarks
			Min	Typ.	Max		
Supply voltage for small-signal circuitry		V_{CC}	3	3.3	5.5	V	
Motor supply voltage		V_M	2.5	—	13.5	V	
Output current	H-SW	I_{OUT}	—	—	600	mA	V_M ≧5 V
			—	—	250		2.5 V ≦ V_M <4 V
	PI SW Transistors	I_D	—	—	30		PIB
PWM frequency (Channels A to E)		f_{PWM}	—	—	100	kHz	
CLK driver frequency		f_{CLK}	—	1	5	MHz	

Operating Ranges: Serial Data Controller (Ta = –20 to 85°C)

Characteristics	Symbol	Rating		Unit
		Min	Max	
Clock pulse width Low	t_{CKL}	200	—	ns
Clock pulse width High	t_{CKH}	200	—	
Clock rise time	t_{Cr}	—	50	
Clock fall time	t_{Cf}	—	50	
Data setup time	t_{DCH}	30	—	
Data hold time	t_{CHD}	60	—	
CK to LD rising edge	t_{CHL}	200	—	
LD hold time	t_{LDC}	200	—	
LD to PWM delay	t_{LDC2}	100	—	
Load pulse width High	t_{LDH}	2	—	μs
CK (clock pulse) frequency	f_{CLK}	—	2.5	MHz



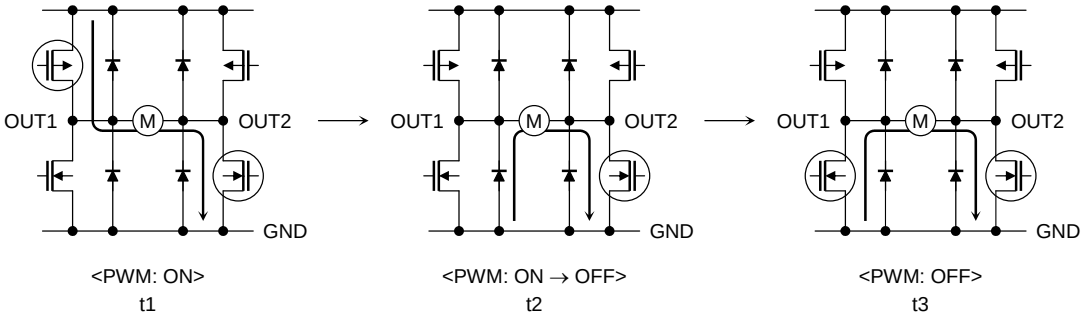
Principle of Operation

Bridge Outputs: Basic operation of channels A through E

PWM Control

In PWM constant-current mode, the PWM chopper circuit alternates between on (t1, t5) and short brake (t3).

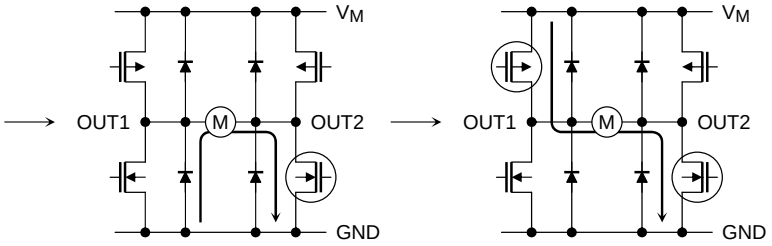
(To eliminate shoot-through current, a dead time (t2, t4) (design target = 100ns) is inserted when the PWM is turned on and off.)



<PWM: ON>
t1

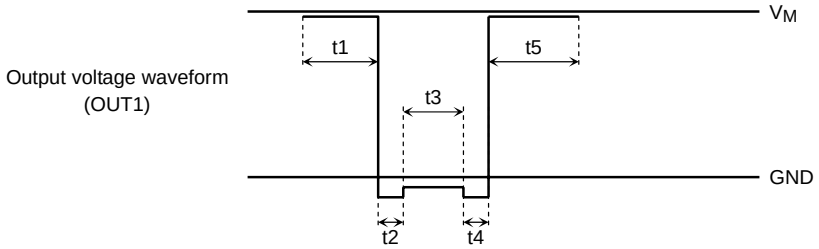
<PWM: ON → OFF>
t2

<PWM: OFF>
t3



<PWM: OFF → ON>
t4

<PWM: ON>
t5



Constant-Current Bridge Driver (Channel E): Off time fixed. PWM constant-current choppers

The TB6609FLG has PWM choppers with a constant turn-off period.

The turn-off period is measured by counting the number of rising edges of an internal clock signal, which is generated by dividing the external CLK signal. The turn-off period can be adjusted by changing either the CLK frequency or the number of its rising edges counted (Count of 2, 4, 6, or 8 is selected).

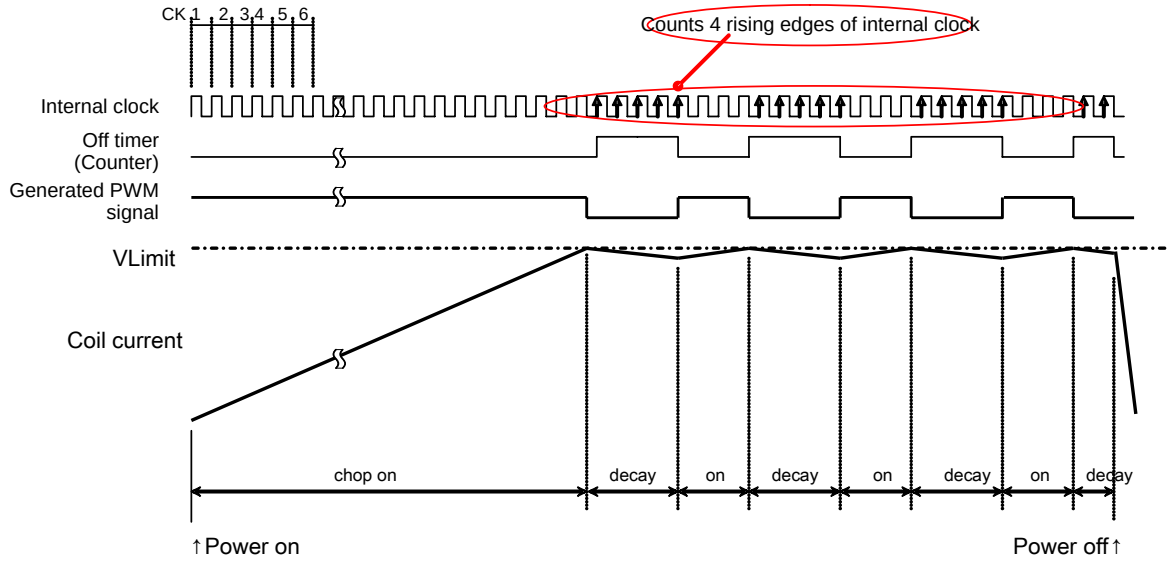
(Example) In case of counts 4 bit clock

Turning on the power supply causes a current to flow into the motor coils. The peak current through the winding is sensed via an external current-sensing resistor. As the current increases, a voltage (VRF) develops across the resistor, which is fed back to the internal comparator. At the predetermined reference voltage (Vlimit: current limiting voltage), the comparator turns off (chops) the power supply.

When output transistors are turned off and the operation moves to the short break mode, the TB6609FLG, by default, counts four rising edges of the internal clock signal as a turn-off period. (The counter resets at the fifth rising edge of the clock.)

Based on this turn-off period, the TB6609FLG generates a PWM signal that turns on and off the output transistors.

Timing Diagram of the PWM Constant-Current Chopper Circuit with the Default Turn-Off Period



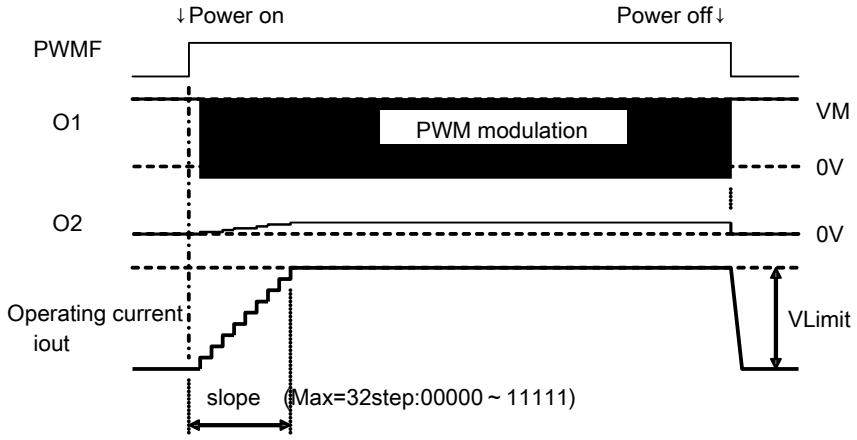
(The upper limit of the coil current (IO peak) can be calculated as: IO = V_{limit}/RNF.)

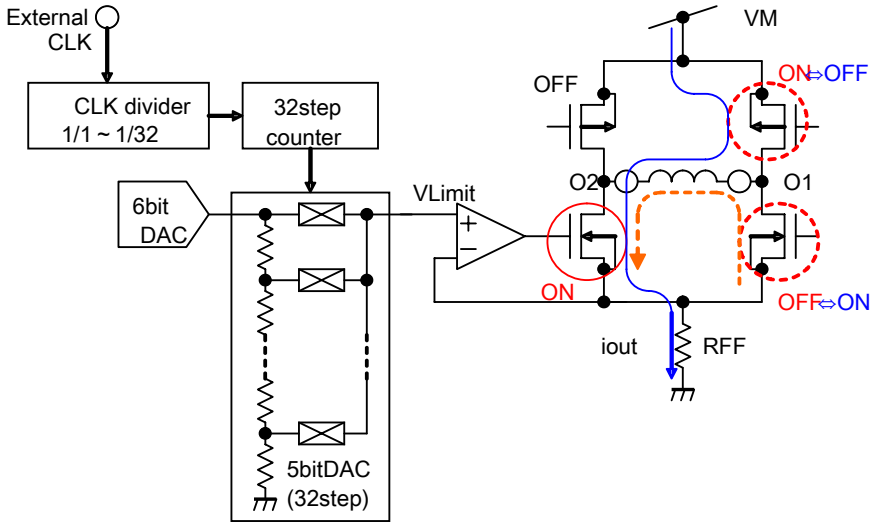
Current ramp-up rate control: Channel F

This bridge driver circuit is tuned on and off by setting the PEMF pin High and Low, respectively.

The driver output current is converted to a voltage through the external resistor RFF and fed back to a comparator, thus driving with PWM modulated signal. This enables the constant-current drive using the low-side driver.

The constant-current value is adjusted by changing the V_{Limit} of the comparator, which is specified by an internal 6-bit DAC (max = 0.3 V). (Ramp-up rate control works only under the conditions of the function table 1 or 2.)





*Current ramp-up rate controller:

To improve the dependency of a current ramp-up rate on supply voltage change at startup and its reproducibility according to the time constant of the coil, the reference voltage for the comparator is increased using a 5-bit DAC (in 32 steps) up to the current limit. This can stabilize the reproducibility of a current ramp-up rate. The current ramp-up rate is specified by dividing an external CLK. The frequency divider ratio can be selected from 32 options by using 5-bit serial data inputs.

PWM constant current control :(It is available in the modes of ramp-up rate control and constant current flat drive.)

PWM constant current control has a system of fixing the turn-off period as channel E.

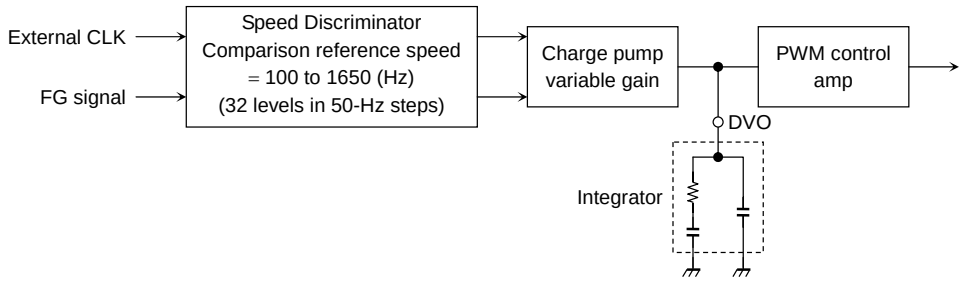
Turn-off period counts the driving CLK input from outside internally.

To change the turn-off period, change the driving CLK frequency or the number of internal counts which can be selected from 1 to 15 counts).

Example) Setting 3 counts → After the peak current is detected, it is turned on at the third rising edge of the external clock. Setting 10 counts → After the peak current is detected, it is turned on at the 10th rising edge of the external clock.

(Note) Channel E is turned on at the clock of specified count plus one. Channel F is turned on at the specified clock.

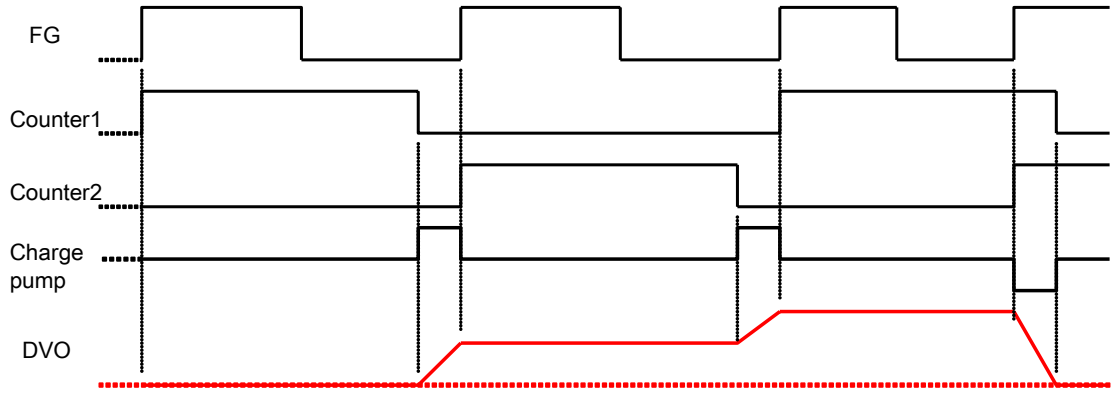
Speed Control



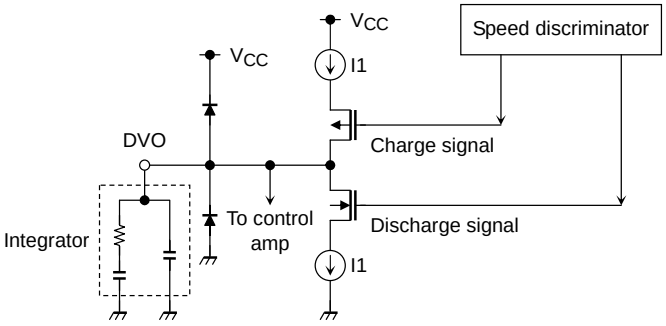
- The FLL speed discriminator compares the FG signal against the reference speed which is derived from an external CLK.
- The speed discriminator has two counters that alternately count one cycle of the FG signal. It then generates error pulses (charge and discharge) according to the frequency difference. Based on these pulses, the integrator (set by an external RC) and the PWM control amplifier generates a motor drive output signal to control the motor rotational speed.
- The reference speed of the speed discriminator is selectable from 32 levels between 100 and 1650 Hz in 50-Hz steps. (It is selected by serial data inputs.)
- The motor rotation speed (N) is calculated by the following equation:

  N (rpm) = Target speed (Comparison reference speed: Hz) × 60(sec) / Z

  Z: Number of FG pulses per rotor rotation



Charge Pump Circuit



- Consisting of CMOS transistors, this charge pump achieves a high resolution of the speed control signal.
- The gain of the speed discriminator can be internally selected from eight combinations×four ranges of charging and discharging current values.

  ①±5 μA to 40μA: 8 levels / 5 μA

  ②±10 μA to 80μA: 8 levels / 10 μA

  ③±20 μA to 160μA : 8 levels / 20 μA

  ④±40 μA to 320μA : 8 levels / 40 μA

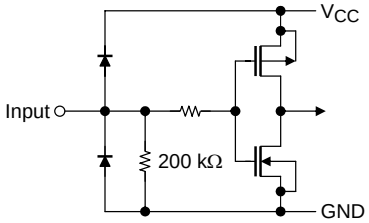
  And the total control gain is determined by adjusting the charge pump current and the time constant of the external integrator.
- When the motor is not rotating, this circuit remains in discharge mode (–40 μA). Thus, the amount of charge stored in a capacitor of the external integrator becomes zero resetting the analog control value.
- Since the FG signal is not generated immediately after the PWME drive signal assertion due to the stationary motor, forced control (arbitrary duty of 25, 50, 75, and 100 %) is possible by arbitrary set time.

  * The motor startup time can be selected in 2.048-ms by a 6-bit (0 to 127ms) command. (Available only in table 1)
- For powering off, the motor operation can be selected from the brake and the reverse-plus-brake modes by arbitrary set time.

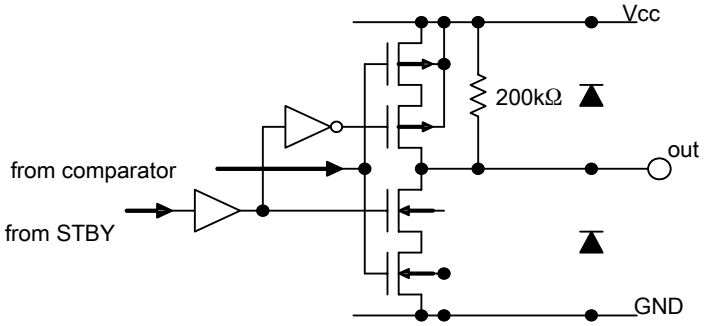
  * The reverse rotation time can be selected in 2.048-ms by a 6-bit (0 to 127ms) command.

Input Pins:

All input pins (CK, DATA, LD, PWMA, PWMB, PWMC, PWMD, PWMF, STBY, and CLK) have a pull-down resistor of about 200 kΩ.

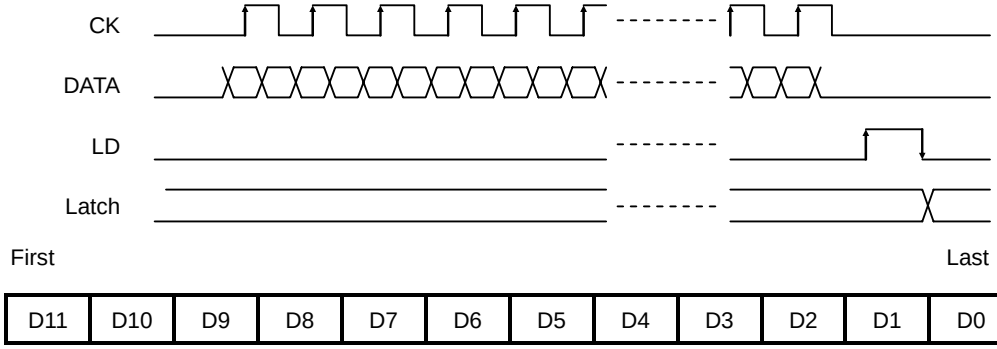


CPO1 and CPO2 pins have a pull-up resistor of about 200kΩ for Vcc. When STBY is low, output gate is turned off (HZ).



Serial Data Format

12 bit serial data / format



Resister mode

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
0	0	0	0	p2a	p2b	mod2	pm2	p1a	p1b	mod1	pm1	0
0	0	0	1	p4a	p4b	mod4	pm4	p3a	p3b	mod3	pm3	1
0	0	1	0	p5a	p5b	mod5	pm5	pms	lat	par	sw	2
0	0	1	1	Target speed (5bit)					PWM-Duty		If5	3
0	1	0	0	cpr1	cpr0	Charge pump (3bit)			-	Career frequency		4
0	1	0	1	Reverse brake time (0 to 127 ms : 6bit)						Vc	disc	5
0	1	1	0	Conducting time for start up (0 to 127 ms : 6bit)						-	-	6
0	1	1	1	DAC1(6bit) <Set the current level for channel. E)						Off time		7
1	0	0	0	p6a	p6b	If6	Constant-current ramp-up rate for channel F (5bit)					8
1	0	0	1	Mod6	pm6	DAC2(6bit) <Set the current level for channel F>						9
1	0	1	0	Off time in ramp-up rate mode				Off time in constant-current mode				10
1	0	1	1	DAC3(4bit)				TH(2bit)		TL(2bit)		11
1	1	0	0	-	-	-	-	-	-	-	-	12
1	1	0	1	-	-	-	-	-	-	-	-	13
1	1	1	0	-	-	-	-	-	-	-	-	14
1	1	1	1	-	-	-	-	-	-	-	-	15

Ifx : Current control for channels E and F (0 = Enable; 1 = Disable)
pms : Channel switching of the PMW input (0 = channel E; 1 = channel F)
off : channel E off time (Chop-off count) set (0 = 2CLK / 1 = 4CLK / 2 = 6CLK / 3 = 8CLK)
sw : PIB sw control (0 = off / 1 = on)
lat : Internal comparator output mode (0 = Latch / 1 = Through)
vc : Channel E control mode (0 = External PWM control / 1 = Internal FLL speed control)
par : Channel F (according to the table 4) and other channels (Channel A to channel E) can be controlled at the same timing (6 channels can be controlled at the same time : par = "1")
Reverse brake : Sets the reverse brake time to be 2.048 ms × specified value (6bit).
disc : Selects the edge count system of speed discriminator (0 = both edges of up and down / 1 = up edge only)
Duty for fixing start up time : Sets the duty to be 2.048ms×specified value (6bit). Conducts at the fixed duty set by PWM-Duty from start up.
PWM-Duty : Sets fixed Duty for start up (2bit:4 levels, 0 = 25% / 1 = 50% / 3 = 75% / 4 = 100%)
cpr0,cpr1 : Specifies the range of reference current for gain of the charge pump.

cpr1	cpr0	Current step	Current range
0	0	5 μA	①5 to 40 μA
0	1	10 μA	②10 to 80 μA
1	0	20 μA	③20 to 160 μA
1	1	40 μA	④40 to 320 μA

Charge pump : These 3 bits specify the gain of the charge pump. (Eight levels per reference current value set with cpr0 and cpr1)
①±5μA to 40 μA, ②±10μA to 80μA, ③±20μA to 160μA, ④±40μA to 320μA

Career frequency : These 2 bits specify the triangular wave frequency (Four steps: 0 = 20 kHz / 1 = 40kHz / 2 = 60kHz / 3 = 80kHz)

Speed target : These 5 bits specify the speed target value (encoder converted) to any of the 32 speed between 100 Hz to 1650 Hz in 50-Hz steps.

Ramp-up rate : Controls the constant-current ramp-up rate for channel F by changing the number of CLK counts. (0 to 31 cycles: Steps up of 1 LSB the DAC output voltage at the number of setting counts).

Off time in ramp-up : These 4 bits specify the number of chop off counts in ramp-up for channel F (1 = 1CLK, 2 = 2CLK, …15 = 15CLK count) (note)

Off time in constant-current mode : These 4 bits specify the number of chop off counts in constant-current control mode for channel F (1 = 1CLK, 2 = 2CLK…15 = 15CLK count) (note)

(note : In case of setting zero CLK count, the constant-current control is invalid.)

DAC1 : Sets constant-current for channel E (MSB = 0.3V / 6bit)

DAC2 : Sets constant-current for channel F (MSB = 0.3V / 6bit)

DAC3 : Sets slesh level of comparator 1 and 2 for P/I encoder. (MSB = 2V / 4 bit)

TH : Sets upper hysteresis of comparator 1 and 2. (DAC 3 + 0.1 V to 0.4 V / 0.1 V per 4 steps:2 bit)

TL : Sets lower hysteresis of comparator 1 and 2. (DAC 3 - 0.1 V to 0.4 V / - 0.1 V per 4 steps:2bit)

Driver function table

(table1)

modx=0 pmx=0 vc=X par=0

pxa	pxb	IC pin			mode
		PWMx	outxA	outxB	
0	0	X	Z	Z	STOP
0	1	L	L	L	Short brake
0	1	H	L	H	CCW
1	0	L	L	L	Short brake
1	0	H	H	L	CW
	1	X	L	L	Short brake

*Only valid for channel E (reverse brake function) : (Logic function is only in valid in the table1.)

・ When short brake mode is selected when mod5 , pm5 , and par are set zero, the motor operation is controlled in the following sequence.

Reverse brake → Short brake

・ The reverse brake time is specified by serial data.
(When the reverse brake time is zero, the TB6609FLG does not enter reverse brake mode.)

・ The operating mode cannot be changed during forced start up operation or reverse brake operation.

・ When pmx input changes during the short brake operation at modx = 0, the operating mode changes according to the pxa and pxb inputs as shown in the above table. (Direct PWM control)

(table2)

modx=0 pmx=1 vc=X par=0

pxa	pxb	IC pin			Mode
		PWMx	outxA	outxB	
0	0	X	Z	Z	STOP
0	1	L	L	H	CCW
0	1	H	L	L	Short brake
1	0	L	H	L	CW
1	0	H	L	L	Short brake
1	1	X	L	L	Short brake

(table3)

modx=1 pmx=X vc=X par=0

pxa	pxb	IC pin			Mode
		PWMx	outxA	outxB	
0	X	X	Z	Z	STOP
1	0	L	H	L	CW
1	0	H	L	H	CCW
1	1	X	L	L	Short brake

(table4) : It is only in valid for channel F in the case that six channels are controlled at the same timing. (Channel A to E can be controlled in the table1, 2, and 3.)

mod6=X pm6=X vc=X par=1

p6a	p6b	IC pin			Mode
		PWMF	FO1	FO2	
0	0	X	Z	Z	STOP
1	0	X	H	L	CW
0	1	X	L	H	CCW
1	1	X	L	L	Short brake

Electrical Characteristics (unless otherwise specified, V_{CC} = 3.3 V, V_M = 5 V, T_a = 25°C)

Characteristics			Symbol	Test Condition	Min	Typ.	Max	Unit
Supply current			I_{CC}	All 6 channels in Forward mode	—	2.2	4	mA
			$I_{CC\ (STB)}$	Standby mode (STBY = 0 V)	—	0.1	10	μA
			$I_{M\ (STB)}$		—	0	1	
Serial, STBY, PWM and CLK inputs	Input voltage		V_{INH}		Vcc-0.8	—	Vcc+0.2	V
			V_{INL}		−0.2	—	0.4	
	Input current		I_{INH}	V_{IH} = 3 V	5	15	25	μA
			I_{INL}	V_{IL} = 0 V	—	—	1	
Output saturation voltage (Channels A to F)			$V_{sat\ (U+L)}$	I_O = 0.2 A	—	0.3	0.4	V
				I_O = 0.6 A	—	0.9	1.2	
Output leakage current (Channels A to F)			$I_{L\ (U)}$	V_M = 15V	—	—	1	μA
			$I_{L\ (L)}$		—	—	1	
Output diode forward voltage			$V_{F\ (U)}$	I_F = 0.6 A (Design value)	—	1	—	V
			$V_{F\ (L)}$		—	1	—	
Control current for limiter (Channel E)			I_{lim}	Vref=0.1V (DAC=h15 setting)	0.17	0.2	0.23	A
Offset voltage for constant-current detection comparator (Channel F)			Comp ofs	RFF = 0.5 Ω, V_{ref} = 0.1 V (including DAC)	−12	-2	8	mV
Comparator for encoder	Vref reference voltage	Min.	V_{comp} Min	DAC3 (Design target only)	0.34	0.39	0.43	V
		Max.	V_{comp} Max		1.8	2	2.2	
		Step	V_{comp} step		—	0.125	—	
	Hysteresis voltage	Min.	V_{hys} Min	(Design target only)	±85	±100	±115	mV
		Max.	V_{hys} Max		±340	±400	±460	
		Step	V_{hys} step		—	±100	—	
	Output voltage H		PIC VOH	I_o=-50μA	Vcc-0.2	—	—	V
	Output voltage L		PIC VOL	I_o=50μA	—	—	0.2	
	Output pull-up resistance		R pullup	V_{cc}=3V,Vout=0V,STBY=L	-25	-15	-5	μA
Speed control charge pump	Charge current 1	Min.	I_{CHG1} Min	Small range mode VDO=0V (Design target only)	3.5	5	7.5	μA
		Max.	I_{CHG1} Max		28	40	60	
		Step	I_{CHG1} step		3.5	5	7.5	
	Charge current 2	Min.	I_{CHG2} Min	Large range mode VDO=0V (Design target only)	28	40	60	
		Max.	I_{CHG2} Max		224	320	480	
		Step	I_{CHG2} step		28	40	60	
	Discharge current 1	Min.	I_{DIS1} Min	Small range mode VDO=1V (Design target only)	-7.5	-5	-3.5	
		Max.	I_{DIS1} Max		-60	-40	-28	
		Step	I_{DIS1} step		-7.5	-5	-3.5	
	Discharge current 2	Min.	I_{DIS2} Min	Large range mode VDO=1V (Design target only)	-60	-40	-28	
		Max.	I_{DIS2} Max		-480	-320	-224	
		Step	I_{DIS2} step		-60	-40	-28	

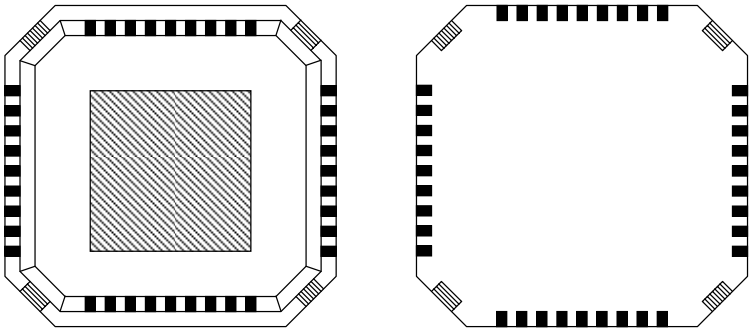
Electrical Characteristics (unless otherwise specified, V_{CC} = 3.3 V, V_M = 5 V, T_a = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Speed control	Minimum speed	FLL Min	(Design target only)	—	100	—	Hz
	Maximum speed	FLL Max		—	1650	—	
	Speed step	FLL step		—	50	—	
Triangular wave carrier	Minimum frequency	FLL Max	(Design target only)	11.5	23	35	kHz
	Maximum frequency	FLL step		44	89	134	
	Frequency step	Ftrig step		11.5	23	35	
Speed control Reverse brake	Minimum control time	Tmin	(Design target only)	—	0	—	ms
	Maximum control time	Tmax		—	128	—	
	Control time step	T step		—	2.048	—	
Speed control Forced start up	Start up Duty	Dduty Min	Sets triangle wave career(= 23 kHz) (Design target only)	15	25	35	%
		Dduty Max		—	100	—	
		Dduty step		15	25	35	
6bit DAC	Nonlinearity	LB	Channel E and F	−3	—	3	LSB
	Differential linearity error	DLB		−2	—	2	
Current ramp-up rate control	Minimum ramp-up time	Slope Min	CLK=1MHz	—	31	—	μs
	Maximum ramp-up time	Slope Max		—	961	—	
P/I SW Tr.	Output saturation voltage	Vsat	ID=20mA	—	0.1	0.2	V
	Output leakage current	IDSS	VDS=6V	—	—	1	μA
Thermal shutdown threshold		TSD	(Design target only)	—	170	—	°C
Thermal shutdown hysteresis		ΔTSD		—	20	—	

QON Package Considerations

Package Appearances

(Top view) (Bottom view)



Please follow the following guidelines for the QON package.

Guidelines:

(1) The solder plated pads at the four corners of the package (shaded areas in the bottom view) should not be soldered for the purpose of improving the mechanical strength of solder joints.

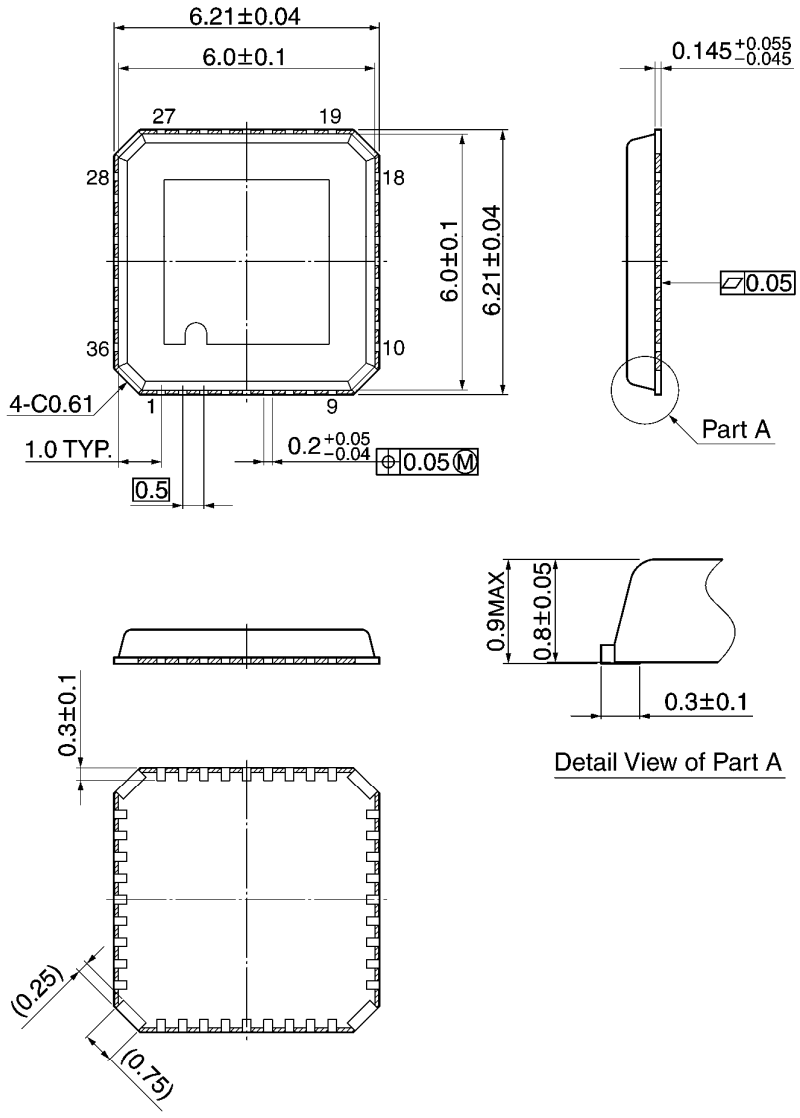
(2) When using the TB6609FLG, it should be ensured that the thermal pad and solder plated pads (shaded areas in the top and bottom views) are electrically insulated (Note).

Note: Care should be taken in the board design to prevent solder for through-hole joints from flowing to the solder plated pads on the bottom of the package (shaded areas in the bottom view).

- When mounting or soldering this package, care must be taken to avoid electrostatic discharge or electrical overstress to the IC. (This is to avoid electrical leakage and a buildup of electrostatic charge in the end product.)
- It should be ensured that no voltage is directly applied to the solder plated pads when designing the PC board.

Package Dimensions

QON36-P-0606-0.50 Unit: mm



Note 1: The solder-plated parts at the four corners of the package should not be used as external pins.

Note 2: The four corners of the package should not be soldered.

Note 3: Shaded areas: Resin surfaces

Weight: 0.08 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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