ML4431

Servo Demodulator

GENERAL DESCRIPTION

The ML4431 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

The ML4431 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

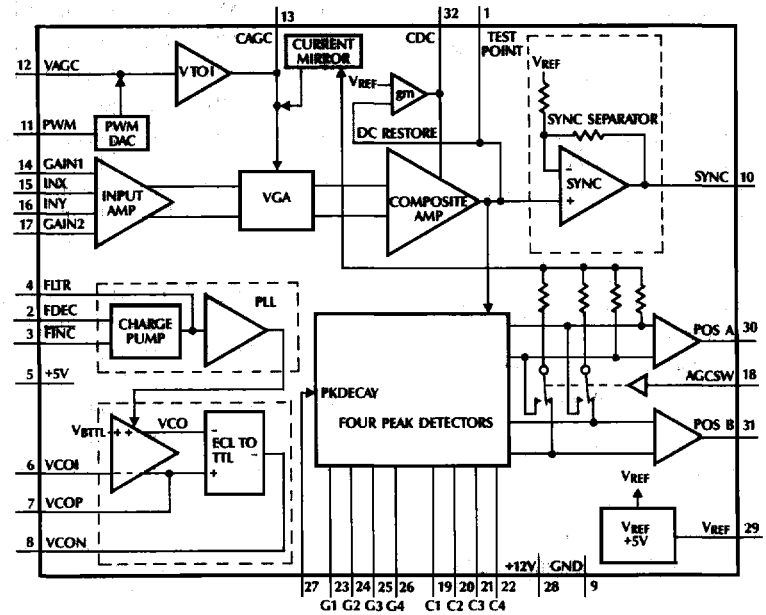
The ML4431 has an ECL-type VCO, with an internal ECL-to-TTL converter for simplified interfacing.

The ML4431, when combined with the ML4402 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

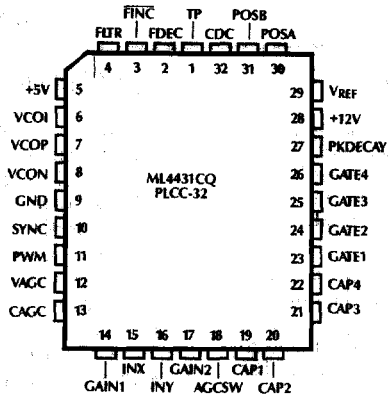
- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 5V and 12V power supplies
- Programmable Peak Detector Discharge Current
- Digitally-controlled AGC set point
- TTL output VCO
- AGC Sense switchable to "POSA only" or both "POSA and POSB"
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402 Servo Driver and ML4404 Trajectory Generator

BLOCK DIAGRAM



PIN CONNECTIONS

ML4431 32-Pin PCC



PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	TP	Composite test point, normally left unconnected.
2	FDEC	Charge pump frequency decrement input.
3	$\overline{\text{FINC}}$	Charge pump frequency increment input.
4	FLTR	PLL loop compensation terminal.
5	+5V	+5V supply.
6	VCOI	VCO input.
7	VCOP	VCO positive output, for capacitive feedback to VCOI.
8	VCON	VCO negative output, drives resistive feedback to VCOI.
9	GND	Ground.
10	SYNC	SYNC pulse output.
11	PWM	PWM DAC input to adjust AGC set point.
12	VAGC	AGC gain reference voltage input.
13	CAGC	External capacitor to set AGC response.
14	GAIN1	Input amplifier gain adjusting RC terminal 1
15	INX	X input into input amplifier.
16	INY	Y input into input amplifier.
17	GAIN2	Input amplifier gain adjusting RC terminal 2.
18	AGCSW	Selects between "POSA only" or "POSA and POSB" AGC sense operation. Logic "0" selects "POSA only" operation. Logic "1" selects "POSA and POSB" operation.
19	CAP1	Peak detector 1 capacitor.
20	CAP2	Peak detector 2 capacitor.
21	CAP3	Peak detector 3 capacitor.
22	CAP4	Peak detector 4 capacitor.
23	GATE1	Peak detector 1 gate input (TTL) Logic "1" enabled, "0" disabled.
24	GATE2	Peak detector 2 gate input (TTL) Logic "1" enabled, "0" disabled.
25	GATE3	Peak detector 3 gate input (TTL) Logic "1" enabled, "0" disabled.
26	GATE4	Peak detector 4 gate input (TTL) Logic "1" enabled, "0" disabled.
27	PKDECAY	Sets peak detector discharge current.
28	+12V	+12V supply.
29	V_{REF}	Voltage reference output.
30	POSA	Position output A. POSA = Peak Detector 1 – Peak Detector 2
31	POSB	Position output B. POSA = Peak Detector 3 – Peak Detector 4
32	CDC	External capacitor terminal to set DC restore response.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage Range, V_{CC} 14V
Input Voltages:
- GAIN1, GAIN2 ..... -0.3 to 8V
- C_{AGC} ..... -0.3 to 7.0V
- V_{AGC}, PWM, VCOI ..... -0.3 to 5.3V
- CAP1, CAP2, CAP3, CAP4 ..... -0.3 to 10V
- GATE1, GATE2, GATE3, GATE4, VCOP ..... -0.3 to 7.5V
- INX, INY, VCON, $\overline{FINC}$, FDEC, C_{DC}, C_{AGC}, FLTR ..... -0.3 to V_{CC} +0.3V

θ_{JA} for PLCC-32 ..... ≈60°C/Watt
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage $V_{(+12V)}$ ..... $12V_{DC}$ ± 10%
Supply Voltage $V_{(+5V)}$ ..... $5V_{DC}$ ± 10%
Input Coupling Capacitance (C_I) 0.01µF
Input Amp Gain Capacitance (C_G) 0.047µF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.018µF
Composite DC Restore Capacitance (C_D) 0.018µF
PLL Compensation Components:
- C_{CP1} 0.1µF
- C_{CP2} 1µF
- R_{CP} 910Ω

VCO Components:
- C_V 39pF
- R_V 1500Ω
- RL 680Ω

Peak Detector Capacitance (CAP1 thru CAP4) 270pF
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) ..... ≈2.4V
R_{SET} 330KΩ

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{VAGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
I_{+12}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		73	51	mA
I_{+5}	Supply Current	V_{+12} = 12V, V_{+5} = 5V		37	47	mA
TTL Inputs $\overline{FINC}$, FDEC, GATE1, GATE2, GATE3, GATE4, PWM, AGCSW						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V	-1		30	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V	-20		1	µA
SYNC Output						
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0	0.35	0.5	V
V_{THR}	Positive going input threshold			V_{REF}+0.9		V
V_{THF}	Negative going input threshold			V_{REF}		V
$t_{PD}\pm$	Propagation Delay Rising, Falling	RL = 2k, C_L = 15pF		50		ns
VCON Output						
V_{OH}	High Level Output Voltage	I_{OH} = 50µA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	20	50	µA
I_{CH}, I_{DIS}	FLTR Charge and Discharge Current		330	450	590	µA
I_{CH}/I_{DIS}	FLTR Charge/Discharge Ratio		0.95	1.00	1.05	µA/µA
I_{OFF}	FLTR OFF State Current	$\overline{FINC}$ = 2.0, FDEC = 0.8	0	25	50	nA
F_{MAX}	MAX VCO Frequency to Maintain + and - 5% Control Range (Note 3)		20			MHz
V_{QH} (FLTR)	Charge Pump Maximum Voltage			$V_{(+12V)}$-1.2V		V
V_{QL} (FLTR)	Charge Pump Minimum Voltage			1.0		V

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of T_A = 0°C to 70°C, $V_{(+12V)}$ = 10.8 to 13.2V, $V_{(+5V)}$ = 4.5 to 5.5V, V_{AGC} = 4.0V, and external components as recommended above, unless otherwise specified (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{VCO}	VCO Frequency Range (Note 3)	T_A = 25°C, V_{+5} = 5V, V_{FLTR} = 6V, C_V = 30pF, R_V = 3.74KΩ, see figure 1	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7	10	14	kΩ
$I_{GAIN1,2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
R_{INAGC}	V_{AGC} Input Resistance		7	10	13	kΩ
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite (Note 4)		10	15		MHz
GMDCR	DC Restore Transconductance			500		μMHOS
Peak Detectors						
I_{CH}	Charge Current		5			mA
I_{DIS}	Discharge Current	T_A = 25°C, R_{SET} = 330K	10	15	20	μA
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25°C	4.75	5.00	5.25	V
TC	Tempco			50		ppm/°C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1-4 = 6V	-10	0	10	mV
A_V	Gain		1.15	1.20	1.25	V/V
A_{VA}/A_{VB}	Gain Tracking		-3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		3			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3dB Gain Bandwidth			3		MHz

Note 1: 0°C to 70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25°C.

Note 3: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).
2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

INPUT AMPLIFIER

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normally desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi(R_G + 60\Omega)C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2
R_G = External series resistance between pins GAIN1 and GAIN2

AUTOMATIC GAIN CONTROL (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P-P\ (Composite\ Position\ Pulses)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65
K2 = .13 * V_{REF}

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: K = 2.8×10^{-4}
V_{VAGC} = External reference voltage at pin V_{AGC}
C_A = External capacitance at pin C_{AGC}

PWM CONTROL OF AGC SET POINT

The PWM input (pin 10) accepts a variable duty-cycle input to control the AGC set point. The relationship between duty-cycle and set point is:

100% duty-cycle ..... AGC set point is equal to V_{REF}.

0% duty-cycle ..... AGC set point equal to 0.6 × V_{REF}.

A filter capacitor from pin 11 to ground is required to filter the PWM signal. This capacitor should be sufficiently large relative to the 10KΩ nominal internal termination resistance at pin 11.

The AGC set point may be set manually via direct voltage control of pin 12 if desired. Pin 11 should be grounded in this case.

SWITCHING THE AGC SENSE RESISTORS

The AGCSW input (pin 17) allows selection of the AGC sense. The choices are:

AGCSW low ..... AGC senses POS A peak detector outputs only.

AGCSW high ..... AGC senses POS A and POS B peak detector outputs.

COMPOSITE AMPLIFIER

The input amplifier and AGC circuit of the ML4431 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF}. The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: gm = $\frac{1}{2K\Omega}$
C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 750Ω resistor is connected in series with pin TP internally.

SYNCHRONIZATION PULSE SEPARATOR

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic. Active pull-up differs from ML4401 SYNC.

PEAK DETECTOR

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1–CAP4 and current out of PKDECAY) determines the maximum track crossing rate during an access operation. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.20 (CAP1 – CAP2) + V_{REF}
POSB = 1.20 (CAP3 – CAP4) + V_{REF}

PEAK DETECTOR DECAY RATE CONTROL

The decay rate of the peak detector can be programmed by changing the external resistor R_{SET} (pin 26, see connection diagram). The decay rate is determined by the discharge current for the hold capacitors C1 – C4. The relationship between the discharge current and R_{SET} is:

$$I_{DISCHARGE} = \frac{V_{REF}}{R_{SET}}$$

VOLTAGE CONTROLLED OSCILLATOR AND CHARGE PUMP

The VCO and external phase compare logic provide a time base for peak detector gate synchronization. Inputs FINC and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The FINC and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 1000Ω, Too low of a value will result in excessive power dissipation. RL should be about 680Ω.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin FLTR to ground. Components R_{CP} and C_{CP2} are also connected in series from pin FLTR to ground to provide VCO loop compensation.

INTERNAL VOLTAGE REFERENCE

V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

EXTERNAL LOGIC

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3pF.

TYPICAL PERFORMANCE CHARACTERISTICS

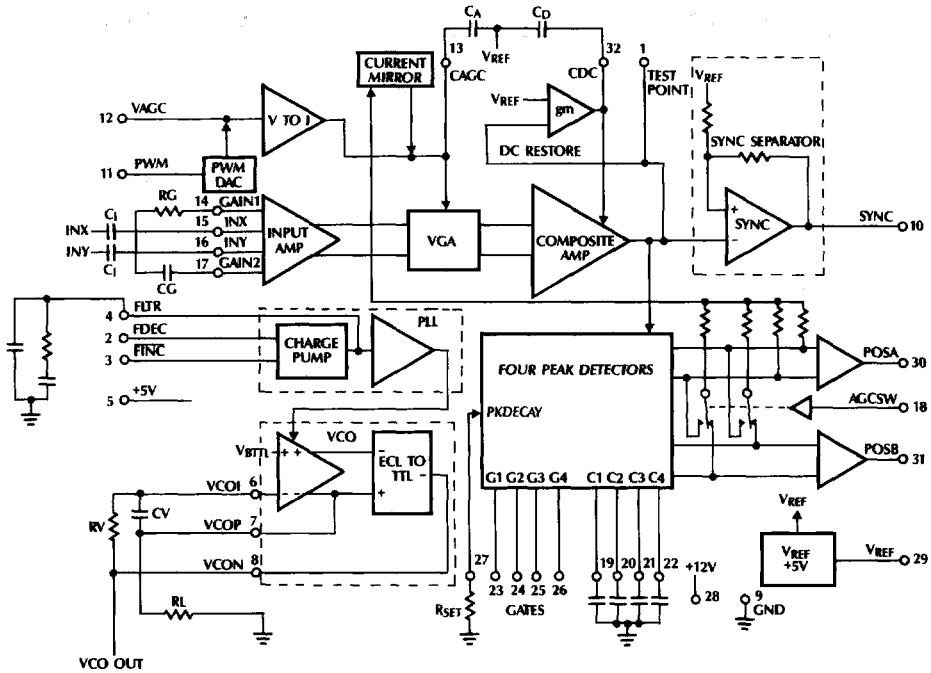
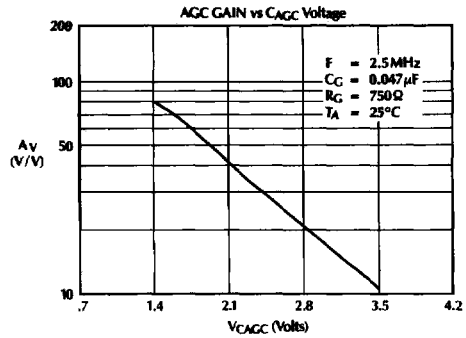


Figure 1. ML4431 Connection Diagram



ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML4431CQ	0°C to +70°C	MOLDED PCC (Q32)