T7570 Programmable PCM Codec with Hybrid-Balance Filter

Features

- Programmable internal hybrid-balance network
- Programmable transmit gain
  — 19.4 dB range, 0.1 dB step size
- Programmable receive gain
  — 19.4 dB range, 0.1 dB step size
- Dual-programmable PCM interface
  — Up to 64 time slots per frame
  — Variable data rate (64 kHz to 4.096 MHz)
  — Two timing modes
- Programmable μ-law or A-law companding
- 300 Ω drive receive amplifier
- Analog and digital loopbacks
- On-chip sample-and-hold, autozero, and precision voltage reference
- Single 5 V power supply
- Latch-up free, low-power CMOS technology
  — 70 mW typical operating power dissipation
  — 1.5 mW typical standby power dissipation
- Serial microprocessor-control interface
- 6-pin parallel I/O latch
- TTL- and CMOS-compatible digital I/O
- Meets or exceeds D3/D4 (as per Legerity PUB 43801), ITU-T (formerly CCITT) G.711—G.712, and LSSGR requirements
- Operating temperature range: –40 °C to +85 °C

Description

The Legerity's T7570 programmable PCM Codec with hybrid-balance filter is a programmable PCM codec with an internal hybrid-balance network filter. It provides analog-to-digital and digital-to-analog conversion, as well as the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed (TDM) system. Programmable features include transmit gain setting over a 19.4 dB range and receive gain setting over a 19.4 dB range. An internal filter can be programmed to provide hybrid balancing over a wide range of loop impedances for both active and transformer subscriber line interface circuits (SLIC).

The device is programmed over a low pin-count, standard, serial, microprocessor-control interface. A 6-pin parallel input/output latch is provided to control interface circuits. Each of these pins can be individually programmed to be an input or an output.

The T7570 is fabricated by using a low-power CMOS technology, requires a single 5 V supply, and is available in a 28-pin PLCC package for surface mounting.

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Description (continued)

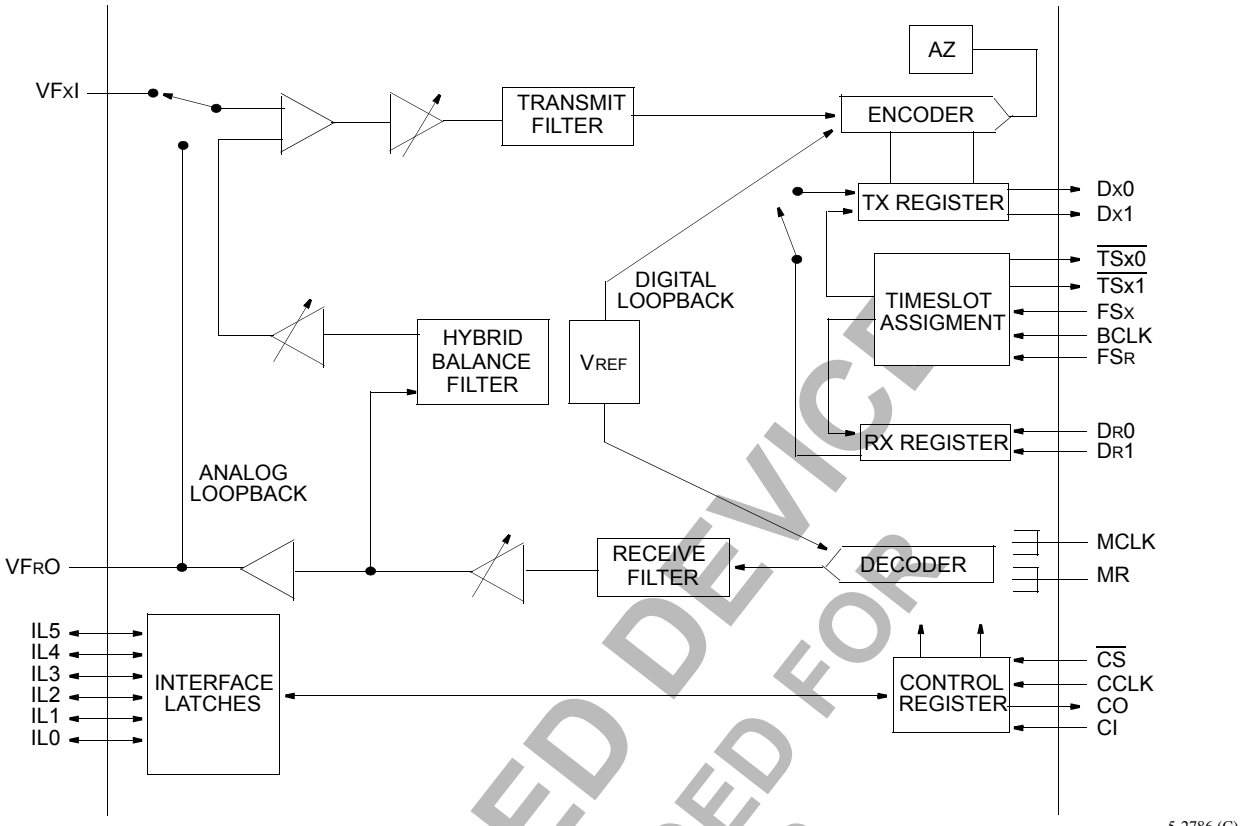


Figure 1. Block Diagram

Pin Information

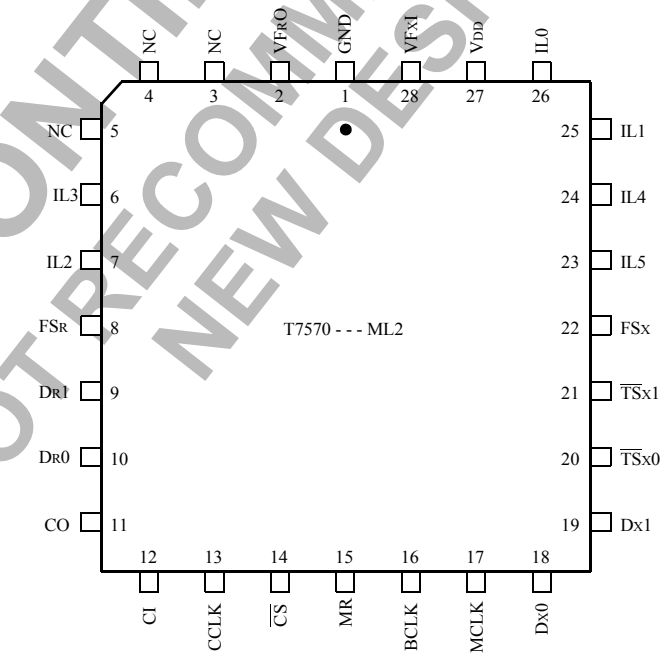


Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Description

Pin	Symbol	Type	Name/Description
1	GND	—	**Ground**. All analog and digital signals are referenced to this pin.
2	VFRO	O	**Receive Analog Power Amplifier Output.** This pin can drive load impedances as low as 300 Ω. PCM data received on the assigned DR pin is decoded and appears at this output as a voice-frequency signal.
3	NC	—	**No Connect.** Connections may be made to or traces may be routed through this pin.
4 5	NC	—	**No Connects.** Do not make connections to or route traces through pins 4 and 5.
6 7	IL3 IL2	I/O I/O	**Interface Latch I/O.** These pins can be individually programmed as inputs or outputs as determined by the state of the corresponding bits in the latch direction register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the interface latch register (ILR) whenever control data is written to the T7570, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
8	FSR	I	**Receive Frame-Sync Input.** A pulse or square-wave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (nondelayed frame mode), or the start of the receive frame (delayed frame mode using the internal time-slot assignment counter).
9 10	DR1 DR0	I I	**Receive PCM Inputs.** These receive data input(s) are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
11	CO	O	**Control Output.** Serial control information is shifted out from the T7570 on this pin when $\overline{CS}$ is low. It can be connected to CI if required.
12	CI	I	**Control Input.** Serial control information is shifted into the T7570 on this pin when $\overline{CS}$ is low. It can be connected to CO if required.
13	CCLK	I	**Control Clock.** This clock shifts serial control information into CI or out from CO when the $\overline{CS}$ is low, depending on the current instruction. CCLK can be asynchronous with the other system clocks.
14	$\overline{CS}$	I	**Chip Select (Active-Low).** When this pin is low, control information can be written into or read from the T7570 via the CI and CO pins.
15	MR	I	**Master Reset.** This logic input must be pulled low for normal operation of the T7570. When pulled momentarily high (at least 1 µs), all programmable registers in the device are reset to the states specified under powerup initialization.
16	BCLK	I	**Bit Clock Input.** This pin shifts PCM data into and out of the DR and DX pins. BCLK can vary from 64 kHz to 4.096 MHz in 8 kHz increments and must be synchronous with MCLK at the start of each frame. MCLK can be used as BCLK.
17	MCLK	I	**Master Clock.** The master-clock input is used by the switched capacitor filters and the encoder and decoder sequencing logic. It must be 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK at the start of each frame.
18 19	DX0 DX1	O O	**Transmit PCM Output.** These transmit-data, high-impedance state outputs remain in the high-impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
20 21	$\overline{TS}$X0 $\overline{TS}$X1	O O	**Backplane Line Driver Enable (Active-Low).** Normally, these open-drain outputs are floating in a high-impedance state. When a time slot is active on one of the DX outputs, the appropriate $\overline{TS}$X output pulls low to enable a backplane line driver.

Pin Information (continued)

Table 1. Pin Description (continued)

Pin	Symbol	Type	Name/Description
22	FSx	I	**Transmit Frame-Sync Input.** A pulse or square-wave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (nondelayed frame mode) or the start of the transmit frame (delayed frame mode using the internal time-slot assignment counter). If only the receive channel is being used, it is still necessary to apply the transmit frame-sync every frame.
23 24 25 26	IL5 IL4 IL1 IL0	I/O I/O I/O I/O	**Interface Latch.** See pin 6.
27	VDD	—	**5 V ± 5% Power Supply.**
28	VFxI	I	**Transmit Analog High-Impedance Input.** Voice-frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and are shifted out on the selected Dx pin.

Functional Description

Powerup Initialization

When power is first applied, powerup reset circuitry initializes the T7570 and puts it into the powerdown state. The gain control registers for the transmit and receive gain sections are programmed to off, the hybrid-balance circuit is turned off, the power amp is disabled, and the device is in the nondelayed timing mode. The latch direction register (LDR) is preset with all IL pins programmed as inputs, placing the interface pins in a high-impedance state. The CI is ready for the first control byte of the initialization sequence. Other initial states in the control register are indicated in the Control Register Instruction section under Programmable Functions.

A reset to these same initial conditions can also be forced by driving the MR pin momentarily high for at least 1 μs. This can be done either on powerup or powerdown. For normal operation, this pin must be pulled low.

The desired modes for all programmable functions can be initialized via the serial control port prior to a powerup command.

Powerdown State

Following a period of activity in the powerup state, the powerdown state can be entered by writing any of the control instructions into the serial control port with the P bit set to 1, as indicated in Table 2.

The powerdown instruction can be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the powerdown state, all nonessential circuitry is de-activated and the Dx0 and Dx1 outputs are in the high-impedance condition.

The coefficients stored in the hybrid-balance circuit and the gain control registers, the data in the LDR and ILR, and all control bits remain unchanged in the powerdown state unless changed by writing new data via the serial control port, which remains active. The outputs of the interface latches also remain active, maintaining the ability to monitor and control interface circuits like a SLIC.

Transmit Filter and Encoder

The transmit section input, VFxI, provides a high-impedance load to the line-interface circuit. The input signal is summed with the internal hybrid cancellation signal. The resulting signal is the input to a programmable gain or attenuation amplifier that is controlled by the contents of the transmit gain register (see Programmable Functions section). The signal is then passed through an antialiasing filter followed by a fifth-order, low-pass and third-order, high-pass, switched-capacitor filter. After the filter, the A/D converter translates the signal into PCM data for transmission. The A/D

Functional Description (continued)

Transmit Filter and Encoder (continued)

converter has a compressing characteristic according to the standard ITU-T A- or μ-coding laws selected by a control instruction (see Tables 2 and 3). A precision on-chip voltage reference helps ensure accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters, or the comparator is canceled by an internal autozero circuit.

Decoder and Receive Filter

PCM data is shifted into the decoder's receive PCM register via the DR0 or DR1 pin during the selected time slot on eight falling edges of BCLK. The decoder consists of an expanding digital-to-analog convertor with either A- or μ-law decoding characteristic, which is selected by the same control instruction used to select the encode law. Following the decoder is a fifth-order, low-pass, switched-capacitor filter with Sin(x)/x correction for the 8 kHz sample and hold. A programmable gain amplifier that is set by writing to the receive gain register is included, followed by a power amplifier capable of driving a 300 Ω load to 4.0 V peak to peak.

PCM Interface

The FSX and FSR frame-sync inputs determine the beginning of the 8-bit transmit and receive time slots, respectively. They can have any duration from a single cycle of BCLK high to one MCLK period low. Two different relationships can be established between the frame-sync inputs and the actual time slots on the PCM buses by setting bit 3 in the control register (see
Table 3). Nondelayed data mode is similar to long-frame timing of other codecs for which time slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use delayed-data mode in which each FS input must be high at least a half-cycle of BCLK earlier than the time slot. The time-slot assignment circuit on the device can only be used with delayed-data timing.

The time-slot assignment capability of this device is a subset of the Legerity concentration highway interface. The beginning of the first time slot in a frame is identified by the appropriate FS input. The actual transmit and receive time slots are then determined by the internal time-slot assignment counters.

Transmit and receive frames and time slots can be skewed from each other by any number of BCLK cycles by offsetting FSR and FSX. During each assigned transmit time slot, the selected DX0/1 output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}$X0 (or $\overline{TS}$X1 as appropriate) also pulls low for the first 7.5 bit times of the time slot to control the high-impedance state enable of a backplane line driver. Serial PCM data is shifted into the selected DR0/1 input during each assigned receive time slot on the falling edges of BCLK. DX0 or DX1 and DR0 or DR1 are selectable on the T7570 (see the Port Selection section under Programmable Functions).

Serial Control Port

Programmable register instructions (Table 2) are written into or read back from the T7570 via the serial control port consisting of the control clock (CCLK), the serial data input (CI) and output (CO), and the chip-select input ($\overline{CS}$) (see Figure 6). All instructions require 2 bytes, with the exception of a single-byte powerup/powerdown command. The bits in byte 1 are defined as follows: bit 7 specifies powerup or powerdown; bits 6, 5, 4, and 3 specify the register address; bit 2 specifies whether the instruction is a read or a write; bit 1 specifies a one-byte or two-byte instruction; and bit 0 is not used.

Prior to the initial register write, after powerup or master reset, CCLK must be cycled a minimum of one time.

To shift control data into the T7570, CCLK must be pulsed high eight times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded and can indicate that a second byte of control data follows. This second byte can either be defined by a second byte wide $\overline{CS}$ pulse or can follow the first contiguously; it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes.

At the end of the eighth CCLK pulse in the second control byte, the data is loaded into the appropriate programmable register. $\overline{CS}$ can remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To read back interface latch data or status information from the T7570, the first byte of the appropriate instruction, as defined in Table 2, is strobed in during the first $\overline{CS}$ pulse. $\overline{CS}$ must then be taken low for a further eight CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When $\overline{CS}$ is high, the CO pin is in the high-impedance state, enabling the CO pins of many devices to be multiplexed together.

Functional Description (continued)

Programmable Functions

Any of the programmable registers can be modified while the device is powered up or down.

Powerup/Powerdown Control

Following powerup initialization, powerup and powerdown control can be accomplished by writing any of the control instructions listed in Table 2 into the T7570, with the P bit set to 0 for powerup or 1 for powerdown. Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power-state control can then be included with the last programming instruction or in a separate single-byte instruction. When the powerup or powerdown control is entered as a single-byte instruction, bit 1 must be 0.

When a powerup command is given, all deactivated circuits are activated, but the PCM outputs, Dx0 and Dx1, remain in the high-impedance state until the second FSx pulse after powerup.

Control Register Instruction

The first byte of a read or write instruction to the control register is as shown in Table 2. The second byte has the bit functions shown in Tables 3, 5, 6, 7, 8, and 9.

Table 2. Programmable Register Instructions

Function	Byte 1								Byte 2
	PDN	Address				R/W	P2	X	
	7	6	5	4	3	2	1	0	DATA
Single-byte Powerup/Powerdown	P	X	X	X	X	X	0	X	None
Write Control Register	P	0	0	0	0	0	1	X	See Table 3.
Read Control Register	P	0	0	0	0	1	1	X	
Write Interface Latch Register	P	0	0	0	1	0	1	X	See Table 6.
Read Interface Latch Register	P	0	0	0	1	1	1	X	
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table 5.
Read Latch Direction Register	P	0	0	1	0	1	1	X	
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table 9.
Read Receive Gain Register	P	0	1	0	0	1	1	X	
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table 8.
Read Transmit Gain Register	P	0	1	0	1	1	1	X	
Write Hybrid-balance Register 1	P	0	1	1	0	0	1	X	These bits are defined by the Legerity T7570 hybrid-balance software program. Contact your Legerity account representative for a copy of this software.
Read Hybrid-balance Register 1	P	0	1	1	0	1	1	X	
Write Hybrid-balance Register 2	P	0	1	1	1	0	1	X	
Read Hybrid-balance Register 2	P	0	1	1	1	1	1	X	
Write Hybrid-balance Register 3	P	1	0	0	0	0	1	X	
Read Hybrid-balance Register 3	P	1	0	0	0	1	1	X	
Write Receive Time Slot/Port	P	1	0	0	1	0	1	X	See Table 7.
Read Receive Time Slot/Port	P	1	0	0	1	1	1	X	(receive instruction)
Write Transmit Time Slot/Port	P	1	0	1	0	0	1	X	See Table 7.
Read Transmit Time Slot/Port	P	1	0	1	0	1	1	X	(transmit instruction)

Notes:
Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI and CO pins. X = don't care.

P is the powerup/down control bit (0 = powerup, 1 = powerdown); see Powerup/Powerdown Control section.

Other register address codes are invalid and should not be used.

Functional Description (continued)

Programmable Functions (continued)

Control Register Instruction (continued)

Table 3. Control Register Byte 2 Functions

Bit Number and Name								Function
7	6	5	4	3	2	1	0	
F_1	F_0	MA	IA	DN	DL	AL	PP	
0	0	—	—	—	—	—	—	Reserved
0	1	—	—	—	—	—	—	MCLK = 1.536 MHz or 1.544 MHz
1	0	—	—	—	—	—	—	MCLK = 2.048 MHz*
1	1	—	—	—	—	—	—	MCLK = 4.096 MHz
—	—	0	X	—	—	—	—	μ-law*
—	—	1	0	—	—	—	—	A-law, Including Even Bit Inversion
—	—	1	1	—	—	—	—	A-law, No Even Bit Inversion
—	—	—	—	0	—	—	—	Delayed Data Timing
—	—	—	—	1	—	—	—	Nondelayed Data Timing*
—	—	—	—	—	0	0	—	Normal Operation*
—	—	—	—	—	1	X	—	Digital Loopback
—	—	—	—	—	0	1	—	Analog Loopback
—	—	—	—	—	—	—	0	Power Amp Enabled in Powerdown
—	—	—	—	—	—	—	1	Power Amp Disabled in Powerdown*

* State at powerup initialization (bit 4 = 0).

Table 4. Coding Law Conventions

V_{IN}	μ-Law MSB LSB	True A-Law With Even Bit Inversion MSB LSB	A-Law Without Even Bit Inversion MSB LSB
V_{IN} = + Full Scale	10000000	10101010	11111111
V_{IN} = 0 V	11111111	11010101	10000000
V_{IN} = – Full Scale	00000000	00101010	01111111

Note: The MSB is always the first PCM bit shifted in or out of the T7570.

Master Clock Frequency Selection

A master clock must be provided to the T7570 for operation of the filter and coding/decoding functions. The MCLK frequency must be either 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK at the start of each frame. Bits F_0 and F_1 (see Table 3) must be set during initialization to select the correct internal divider.

Coding Law Selection

Bits MA and IA in Table 3 permit the selection of μ-law coding or A-law coding, with or without even bit inversion.

Analog Loopback

The analog loopback mode is entered by setting the AL and DL bits in the control register as shown in Table 3. In the analog loopback mode, the transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the receive PCM register back to the transmit PCM register. The VF_RO pin remains active, and the programmed settings of the transmit and receive gains remain unchanged; therefore, care must be taken to ensure that overload levels are not exceeded anywhere in the loop. It is recommended that the hybrid-balance filter be disabled during analog loopback.

Functional Description (continued)

Programmable Functions (continued)

Digital Loopback

The digital loopback mode is entered by setting the AL and DL bits in the control register as shown in Table 3. This mode provides another stage of path verification by enabling data written into the receive PCM register to be read back from that register in any transmit time slot at DX0/1. In digital loopback mode, the decoder remains functional and outputs a signal at VFRO. If this is undesirable, the receive output can be disabled by programming the receive gain register to all 0s.

Interface Latch Directions

Immediately following powerup, all interface latches assume they are inputs and, therefore, all IL pins are in a high-impedance state. Each IL pin can be individually programmed as a logic input or output by writing the appropriate instruction to the LDR (see Tables 2 and 5). For minimum power dissipation, unconnected latch pins should be programmed as outputs.

Bits L5—L0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows.

Table 5. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L0	L1	L2	L3	L4	L5	X	X

Note: X = don't care.

Ln Bit	IL Direction
0	Input
1	Output

Interface Latch States

Interface latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the interface latch register (ILR) as shown in Tables 2 and 6. Latches configured as inputs sense the state applied by an external source, such as the off-hook detect output of a SLIC. All bits of the ILR, i.e., sensed inputs and the programmed state of outputs, can be read back in the second byte of a read of the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first, followed immediately by the LDR.

Table 6. Interface Latch Data Bit Order Bit Number

Bit Number							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D0	D1	D2	D3	D4	D5	X	X

Time-Slot Assignment

The T7570 can operate in either fixed time-slot or time-slot assignment mode for selecting the transmit and receive PCM time slots. Following powerup, the device is automatically in nondelayed timing mode, in which the time slot always begins with the leading (rising) edge of frame-sync inputs FSX and FSR. Time-slot assignment can only be used with delayed-data timing (see Figure 5). FSX and FSR can have any phase relationship with each other in BCLK period increments. Alternatively, the internal time-slot assignment counters and comparators can be used to access any time slot in a frame by using the frame-sync inputs as marker pulses for the beginning of transmit and receive time slots of 8 bits each. A time slot is assigned by a 2-byte instruction as shown in Tables 2 and 7. The last 6 bits of the second byte indicate the selected time slot from 0 to 63 using straight binary notation. A new assignment becomes active on the second frame following the end of the $\overline{CS}$ for the second control byte. The EN bit allows the PCM inputs, DR0/1, or outputs, DX0/1, as appropriate, to be enabled or disabled. Time-slot assignment mode requires that the FSX and FSR pulses must conform to the delayed-data timing format shown in Figure 5.

Port Selection

Two transmit serial PCM ports, DX0 and DX1, and two receive serial PCM ports, DR0 and DR1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the PS bit in the second byte. Port selection can only be used in delayed-data timing mode.

Table 7 shows the format of the second byte of both transmit and receive time-slot and port assignment instructions.

Functional Description (continued)

Programmable Functions (continued)

Table 7. Time-Slot and Port Assignment Instruction

Bit Number and Name								Function
7 EN	6 PS	5 T_5*	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	0	X	X	X	X	X	X	Disable D_X0 Output (transmit instruction) Disable D_R0 Input (receive instruction)
0	1	X	X	X	X	X	X	Disable D_X1 Output (transmit instruction) Disable D_R1 Input (receive instruction)
1	0	Assign One Binary-coded Time Slot from 0—63						Enable D_X0 Output (transmit instruction) Enable D_R0 Input (receive instruction)
1	1	Assign One Binary-coded Time Slot from 0—63						Enable D_X1 Output (transmit instruction) Enable D_R1 Input (receive instruction)

* T_5 is the MSB of the time-slot assignment.

Transmit Gain Instruction Byte 2

The transmit gain can be programmed in 0.1 dB steps from –0.4 dB to +19.0 dB by writing to the transmit gain register as defined in Tables 2 and 8. This corresponds to a range of 0 dBm0 levels at VF_XI between 0.811 Vrms and 0.087 Vrms (equivalent to +0.4 dBm to –19.0 dBm into 600 Ω).

To set transmit gain, determine the gain required of the codec in order to achieve the overall desired transmission level point (TLP) at the PCM interface (usually 0 dBm or –2 dBm).

In order for the internal hybrid-balance circuitry to be effective, the portion of VF_RO returned to the codec analog input must be between –2.5 dB to –10.25 dB of the VF_RO output. For instance, if a SLIC presents a –6 dBm signal to VF_XI when VF_RO produces 0 dBm, good hybrid balance can be achieved. If the returned signal requires amplification to satisfy this requirement, then an additional op amp in the transmit path would be required. The T7570 will accommodate the phase inversion. A spare op amp is provided in some Legerity SLICs.

Once the codec gain is chosen, determine what signal level at VF_XI would provide the desired TLP output at Dx. For our example of +6 dB gain (Gx) providing a 0 dBm TLP and working backwards from Dx, take the antilog of minus 6 dB divided by 20 and multiply by the 0.7746 reference level to obtain the signal level at VF_XI in Vrms. As follows:

(1) $\text{antilog}_{10}(-Gx / 20) * 0.7746 = \text{Vrms}$

Finally, convert the signal level to a decimal number (n) using the following formula:

(2) $200 * \log_{10}(\text{Vrms} / 0.08592) = n$

Round n to the nearest integer and convert to binary. This is the code required by byte 2 of this instruction. Some examples are given in Table 8.

Table 8. Byte 2 of Transmit Gain Instructions

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_XI
0 0 0 0 0 0 0 0	No Output
0 0 0 0 0 0 0 1	0.087
0 0 0 0 0 0 1 0	0.088
—	—
1 0 1 1 1 1 1 1*	0.7746
—	—
1 1 0 0 0 0 1 0	0.802
1 1 0 0 0 0 1 1†	0.811

* 0 dB path gain setting.
† Programming values greater than those listed in this table are permitted. However, large signals may cause overload.

Receive Gain Instruction Byte 2

The receive gain can be programmed in 0.1 dB steps from –17.3 dB to +2.1 dB by writing to the receive gain register as defined in Tables 2 and 9. This corresponds to a range of 0 dBm0 levels at VF_RO between 0.987 Vrms and 0.106 Vrms (equivalent to +2.1 dBm to –17.3 dBm into 600 Ω).

Functional Description (continued)

Programmable Functions (continued)

To set receive gain, first determine the gain required of the codec. For line card use, determine the codec's allocation to set the overall transmission level point (TLP) at Tip\Ring accordingly (usually 0 dBm or –4 dBm).

Once the codec gain is chosen, determine the signal level that would be delivered to VFRO when the reference TLP appears at DR. Take the antilog of the gain in dB (GR) divided by 20 and multiply by the 0.7746 reference level to obtain the signal level at VFRO in Vrms. As follows:

(3) $\text{antilog}_{10}(G_R / 20) * 0.7746 = \text{Vrms}$

Finally, convert the signal level output to a decimal number (n) using the following formula:

(4) $200 * \log_{10}(\text{Vrms} / 0.1045) = n$

Round n to the nearest integer and convert to binary. This is the code required by byte 2 of this instruction. Some examples are given in Table 9.

Table 9. Byte 2 of Receive Gain Instructions

Bit Number	0 dBm0 Test Level (Vrms)
7 6 5 4 3 2 1 0	**at VFRI**
0 0 0 0 0 0 0 0	No Output (low Z to GND)
0 0 0 0 0 0 0 1	0.106
0 0 0 0 0 0 1 0	0.107
—	—
1 0 1 0 1 1 1 0*	0.7746
—	—
1 1 0 0 0 0 1 0	0.975
1 1 0 0 0 0 1 1†	0.987

* 0 dB path gain setting.
† Programming values greater than those listed in this table are permitted. However, large signals may cause overload.

Hybrid-Balance Filter

The hybrid-balance filter on the T7570 is a programmable filter consisting of a second-order section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180° inverting stage is included to compensate for interface circuits that invert the transmit input relative to the receive output signal. The second-order section is intended mainly to balance low-frequency signals across a transformer SLIC, and the first-order section is intended to balance midrange to higher audio-frequency signals.

As a second-order section, Hybal1 has a pair of low-frequency zeros and a pair of complex conjugate poles. When configuring the Hybal1, matching the phase of the hybrid at low- to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The second-order mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 H or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low-frequency pole and zero. In this mode, the pole/zero frequency can be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 filter only, in which case the Hybal2 filter should be deselected to bypass it.

Hybal2, the higher-frequency first-order section, is provided for balancing an electronic SLIC and is also helpful with a transformer SLIC in providing additional phase correction for mid- and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and nonloaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Figure 3 shows a simplified diagram of the local echo-path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VFXI, are a function of the termination impedance ZT, the line transformer, and the impedance of the two-wire loop, ZL. If the impedance reflected back into the transformer primary is expressed as ZL', then the echo path transfer function from VFRO to VFXI is the following:

(5) $H(W) = Z_{L'} / (Z_T + Z_{L'})$

The signal level returned at VFXI must be between –2.5 dB to –10.25 dB over the voice band, relative to the output at VFRO, in order for the hybrid balance function to be effective. Signals outside this range exceed the range of programmability of the hybrid path, and the software will provide unacceptable hybrid balance performance over the voice band.

Functional Description (continued)

Hybrid-Balance Filter (continued)

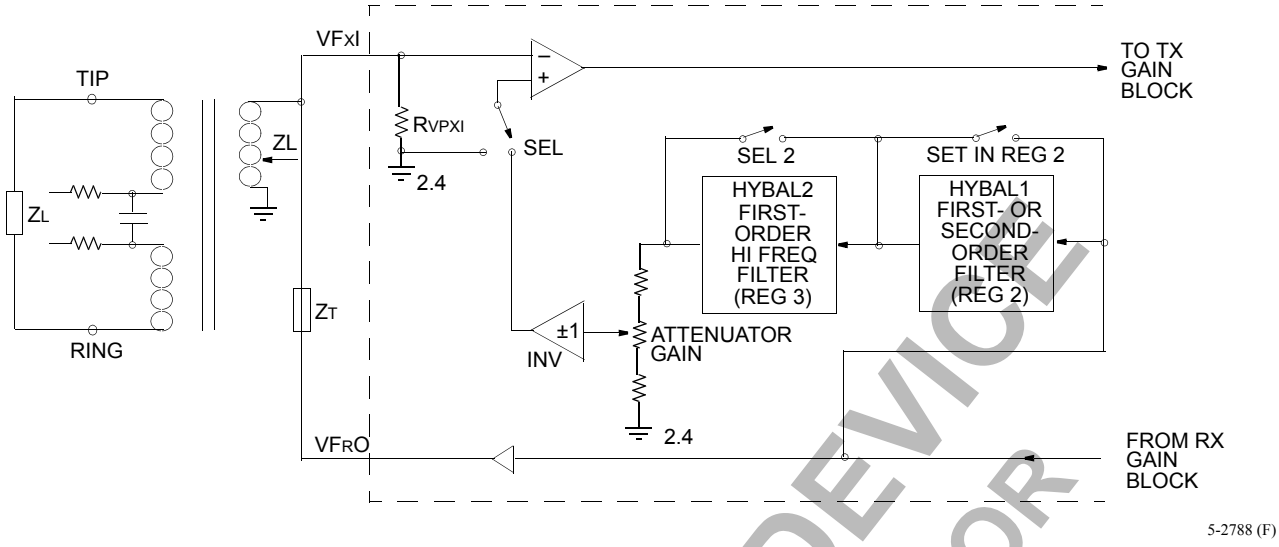


Figure 3. Block Diagram Hybrid-Balance Filter Network

Programming the Filter

On initial powerup, the hybrid-balance filter is disabled. Before the hybrid-balance filter can be programmed, it is necessary to design the transformer and termination impedance to meet system 2-wire input return loss specifications, which are normally measured against a fixed test impedance (600 Ω or 900 Ω in most countries). Only then can the echo path be modeled and the hybrid-balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national telecommunication administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in Figure 3. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, $D_R0/1$, to the PCM digital output, Dx0/1, either by digital test signal analysis or by conversion back to analog by a PCM codec/filter.

Three registers must be programmed in the T7570 to fully configure the hybrid-balance filter (refer to Table 2 for Byte 1 addressing):

Register 1: Select/deselect hybrid-balance filter; invert/noninvert cancellation signal; select/deselect Hybal2 filter section; set attenuator.

Byte 2 of Register 1							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEL	INV	SEL2	GAIN (All 0 = MAX)				

Register 2: Select/deselect Hybal1 filter; set Hybal1 to biquad or first order; select pole and zero frequency.

Register 3: Program pole frequency in Hybal2 filter; program zero frequency in Hybal2 filter.

Standard filter design techniques can be used to model the echo path (see Equation 5) and design a matching hybrid-balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid-balance filter designed to replicate it.

T7570 hybrid-balance software is available from your Legerity account representative to aid in selecting the best balance filter register settings.

Functional Description (continued)

Hybrid-Balance Filter (continued)

Power Supply

While the pins of the T7570 devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed-circuit card can be plugged into a hot socket with power and clocks already present, an extra-long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the device GND pin to prevent the interaction of ground return currents flowing through a common-bus impedance. A power-supply decoupling capacitor of 0.1 µF should be connected from this common point to V_{DD}, as close to the device pins as possible. The power supply should also be decoupled with a low, effective series resistance capacitor of at least 10 µF, located near the card edge connector.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage	V_{DD}	—	6.5	V
Voltage on Any Pin with Respect to Ground	—	–0.5	0.5 + V_{DD}	V
Maximum Power Dissipation (package limit)	P_{DISS}	—	600	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Legerity employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Table 10. Human-Body Model ESD Threshold

Device	Voltage
T7570	≥2000 V

Electrical Characteristics

For all tests, T_A = –40 °C to +85 °C, V_{DD} = 5 V ± 5%, and GND = 0 V, unless otherwise noted. Typical values are for T_A = 25 °C and nominal supply values.

dc Characteristics

Table 11. Digital Interface

Parameter		Symbol	Test Conditions	T_A (°C)	Min	Max	Unit
Input Voltage	Low	V_{IL}	All digital inputs	—	—	0.7	V
	High	V_{IH}	All digital inputs	—	2.0	—	V
Output Voltage	Low	V_{OL}	DX0, DX1, CO, I_L = 3.2 mA	—	—	0.4	V
			All other digital outputs, I_L = –1 mA	—	—	0.4	V
	High	V_{OH}	DX0, DX1, CO, I_L = 3.2 mA	—	2.4	—	V
			All other digital outputs except $\overline{TSX}$, I_L = –1 mA	—	2.4	—	V
			All digital outputs, I_L = –100 µA	—	V_{CC} – 0.5	—	V
Input Current	Low	I_{IL}	Any digital input, GND < V_{IN} < V_{IL}	—	–10	10	µA
	High	I_{IH}	Any digital input except MR, V_{IH} < V_{IN} < V_{CC}	—	–10	10	µA
			MR only	—	–10	100	µA
Output Current in High-impedance State	—	I_{OZ}	DX0, DX1, CO, IL5—IL0 when selected as inputs, GND < V_{OUT} < V_{CC}	–40 to 0	–30	30	µA
				0 to 85	–10	10	µA

Table 12. Power Dissipation

Parameter	Symbol	Test Conditions	Typ	Max	Unit
Powerdown Current	$I_{DD}0$	CCLK, CI, CO = 0.4 V, $\overline{CS}$ = 2.4 V, interface latches set as outputs with no load, all other inputs active, power amp enabled	0.3	0.9	mA
Powerup Current	$I_{DD}1$	CCLK, CI, CO = 0.4 V, $\overline{CS}$ = 2.4 V, no load on power amp, interface latches set as outputs with no load	14.0	20.0	mA
Powerdown Current	$I_{DD}2$	CCLK, CI, CO = 0.4 V, $\overline{CS}$ = 2.4 V, interface latches set as outputs with no load, all other inputs active, power amp enabled, no load on power amp	4.0	6.0	mA

Transmission Characteristics

Table 13. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Resistance	R_{VFXI}	0.25 V < VFxI < 4.75 V	390	585	—	kΩ
Input Offset Voltage at VFxI	VOS_X	—	2.3	—	2.5	V
Load Resistance	RL_{VFRO}	—	300	—	—	Ω
Load Capacitance	CL_{VFRO}	$RL_{VFRO} \geq 300\ \Omega$ CL_{VFRO} from VFRO to GND	—	—	200	pF
Output Resistance	RO_{VFRO}	Steady zero PCM code applied to DR0 or DR1	—	1.6	3.0	Ω
Output Offset Voltage at VFRO	VOS_R	Alternating ± zero PCM code applied to DR0 or DR1, maximum receive gain	2.3	—	2.5	V
Output Offset Voltage at VFRO, Powerdown	VOS_{RPD}	Control register byte 2, bit 7 = 0	2.3	—	2.5	V
Output Voltage Swing	V_{SWR}	RL = 300 Ω, maximum receive gain	4.01	—	—	V_{PP}

Table 14. Gain and Dynamic Range

Parameter	Symbol	Test Conditions	TA (°C)	Min	Typ	Max	Unit
Absolute Levels	G_{AL}	Maximum 0 dBm0 levels:					
		VFxI (gain set to 11000011)	—	—	0.811	—	Vrms
		VFRO (gain set to 11000011)	—	—	0.987	—	Vrms
		Minimum 0 dBm0 levels:					
		VFxI (gain set to 00000001)	—	—	87.0	—	mVrms
		VFRO (gain set to 00000001)	—	—	106.0	—	mVrms
Transmit Gain Absolute Accuracy	G_{XA}	Transmit gain programmed for maximum 0 dBm0 test level, measured deviation of digital code from ideal 0 dBm0 PCM code at Dx0/1, TA = 25 °C	—	–0.15	—	0.15	dB
Transmit Gain Variation with Temperature	G_{XAT}	Measured relative to G_{XA}, V_{DD} = 5 V, minimum gain < GX < maximum gain	–40 to 0	–0.15	—	0.15	dB
			0 to 85	–0.1	—	0.1	dB
Transmit Gain Variation with Programmed Gain	G_{XAG}	Measured transmit gain over the range from maximum to minimum, calculated the deviation from the programmed gain relative to G_{XA} (i.e., G_{XAF} = Gactual – Gprog – G_{XA}), TA = 25 °C, V_{DD} = 5 V	—	–0.1	—	0.1	dB

Transmission Characteristics (continued)

Table 14. Gain and Dynamic Range (continued)

Parameter	Symbol	Test Conditions	T_A (°C)	Min	Typ	Max	Unit
Transmit Gain Variation with Frequency	G_{XAF}	Relative to 1020 Hz, minimum gain < G_X < maximum gain, D_{R0} or D_{R1} = 0 dBm0 code:					
		f = 16.67 Hz	—	—	–35	–30	dB
		f = 50 Hz	—	—	–33	–30	dB
		f = 60 Hz	—	—	–40	–30	dB
		f = 200 Hz	—	–1.8	–0.5	0	dB
		f = 300 Hz to 3000 Hz	—	–0.125	±0.04	0.125	dB
		f = 3140 Hz	—	–0.57	0.01	0.125	dB
		f = 3380 Hz	—	–0.885	–0.6	0.012	dB
		f = 3860 Hz	—	—	–9.9	–8.98	dB
		f ≥ 4600 Hz (measured response at alias frequency from 0 kHz to 4 kHz)	—	—	—	–32	dB
Transmit Gain Variation with Signal Level	G_{XAL}	Sinusoidal test method, reference level = 0 dBm0:					
		VF_{XI} = –40 dBm0 to +3 dBm0	—	–0.2	—	0.2	dB
		VF_{XI} = –50 dBm0 to –40 dBm0	—	–0.4	—	0.4	dB
		VF_{XI} = –55 dBm0 to –50 dBm0	—	–1.2	—	1.2	dB
Receive Gain Absolute Accuracy	G_{RA}	Receive gain programmed for maximum 0 dBm0 test level, applied 0 dBm0 PCM code to D_{R0} or D_{R1}, measured VF_{RO}, T_A = 25 °C, load = 10 kΩ	—	–0.15	—	0.15	dB
Receive Gain Variation with Temperature	G_{RAT}	Measured relative to G_{RA}, V_{DD} = 5 V, minimum gain < G_R < maximum gain	–40 to 0	–0.15	—	0.15	dB
			0 to 85	–0.1	—	0.1	dB
Receive Gain Variation with Programmed Gain	G_{RAG}	Measured receive gain over the range from maximum to minimum setting, calculated the deviation from the programmed gain relative to G_{RA}, i.e., $G_{RAG} = G_{actual} – G_{prog} – G_{RA}$, T_A = 25 °C, V_{DD} = 5 V	—	–0.1	—	0.1	dB

Transmission Characteristics (continued)

Table 14. Gain and Dynamic Range (continued)

Parameter	Symbol	Test Conditions	T_A (°C)	Min	Typ	Max	Unit
Receive Gain Variation with Frequency	G_{RAF}	Relative to 1020 Hz, D_{R0} or D_{R1} = 0 dBm0 code, minimum gain < G_R < maximum gain:					
		f ≤ 3000 Hz	—	–0.125	±0.04	0.125	dB
		f = 3140 Hz	—	–0.57	0.01	0.125	dB
		f = 3380 Hz	—	–0.885	–0.58	+0.012	dB
		f = 3860 Hz	—	—	–10.7	–8.98	dB
		f ≥ 4600 Hz	—	—	—	–28	dB
Receive Gain Variation with Signal Level	G_{RAL}	Sinusoidal test method, reference level = 0 dBm0:					
		D_{R0} = –40 dBm0 to +3 dBm0	—	–0.2	—	0.2	dB
		D_{R0} = –50 dBm0 to –40 dBm0	—	–0.4	—	0.4	dB
		D_{R0} = –55 dBm0 to –50 dBm0	—	–1.2	—	1.2	dB

Table 15. Envelope Delay Distortion

Parameter	Symbol	Test Conditions	Min	Max	Unit
Tx Delay, Absolute	D_{XA}	f = 1600 Hz	—	315	µs
Tx Delay, Relative to 1600 Hz	D_{XR}	f = 500 Hz—600 Hz	—	220	µs
		f = 600 Hz—800 Hz	—	145	µs
		f = 800 Hz—1000 Hz	—	75	µs
		f = 1000 Hz—1600 Hz	—	40	µs
		f = 1600 Hz—2600 Hz	—	75	µs
		f = 2600 Hz—2800 Hz	—	105	µs
		f = 2800 Hz—3000 Hz	—	155	µs
Rx Delay, Absolute	D_{RA}	f = 1600 Hz	—	200	µs
Rx Delay, Relative to 1600 Hz	D_{RR}	f = 500 Hz—1000 Hz	–40	—	µs
		f = 1000 Hz—1600 Hz	–30	—	µs
		f = 1600 Hz—2600 Hz	—	90	µs
		f = 2600 Hz—2800 Hz	—	125	µs
		f = 2800 Hz—3000 Hz	—	175	µs

Transmission Characteristics (continued)

Table 16. Noise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Noise, C Message Weighted, μ-law Selected	NXC	All 1s in gain register	—	—	15	dBrnC0
Transmit Noise, P Message Weighted, A-law Selected	NXP	All 1s in gain register	—	—	–67	dBm0p
Receive Noise, C Message Weighted, μ-law Selected	NRC	PCM code is alternating positive and negative zeros	—	—	13	dBrnC0
Receive Noise, P Message Weighted, A-law Selected	NRP	PCM code equals positive one LSB	—	—	–79	dBm0p
Noise, Single Frequency	NRS	f = 0 kHz—100 kHz, analog to analog measurement (DX0 is externally connected to DR0), VFXI = 0 Vrms	—	—	–53	dBm0
Power Supply Rejection, Transmit	PPSRX	VDD = 5.0 Vdc + 100 mVrms:				
		f = 0 kHz—4 kHz*	36	—	—	dBC
		f = 4 kHz—50 kHz	30	—	—	dBC
Power Supply Rejection, Receive	PPSRR	PCM code equals positive one LSB, VDD = 5.0 + 100 mVrms, measured VFRO:				
		f = 0 Hz—4000 Hz	36	—	—	dBC
		f = 4 kHz—25 kHz	40	—	—	dB
		f = 25 kHz—50 kHz	36	—	—	dB
Spurious Out-of-Band Signals at the Channel Output	SOS	0 dBm0, 300 Hz—3400 Hz input PCM code applied at DR0 (or DR1):				
		4600 Hz—7600 Hz	—	—	–30	dB
		7600 Hz—8400 Hz	—	—	–40	dB
		8400 Hz—50,000 Hz	—	—	–30	dB

* PPSRX is measured with a –50 dBm0 activation signal applied to VFXI.

Transmission Characteristics (continued)

Table 17. Distortion

Parameter	Symbol	Test Conditions	Min	Max	Unit
Signal to Total Distortion Transmit or Receive Half-channel, μ-law Selected	STDX STDR	Sinusoidal test method level: 3.0 dBm0 0 dBm0 to –30 dBm0 –40 dBm0 –45 dBm0	 33 36 30 25	 — — — —	 dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFDX	—	—	–46	dB
Single Frequency Distortion, Receive	SFDR	—	—	–46	dB
Intermodulation Distortion	IMD	Transmit or receive two frequencies in the range (300 Hz—3400 Hz)	—	–41	dB

Table 18. Crosstalk

Parameter	Symbol	Test Conditions	Typ	Max	Unit
Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	CTX–R	f = 300 Hz—3400 Hz DR = steady PCM code	–90	–75	dB
Receive to Transmit Crosstalk, 0 dBm0 Receive Level	CTR–X	f = 300 Hz—3400 Hz*	–90	–70	dB

* CTR–X and PPSRX are measured with a –50 dBm0 activation signal applied to VFXI.

Timing Characteristics

A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification, the following conditions apply:

- All input signals are defined as V_{IL} = 0.4 V, V_{IH} = 2.7 V, t_R < 10 ns, t_F < 10 ns.
- t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.
- Delay times are measured from the input signal valid to the output signal valid.
- Setup times are measured from the data input valid to the clock input invalid.
- Hold times are measured from the clock signal valid to the data input invalid.
- Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Table 19. Master Clock Timing (See Figures 4 and 5.)

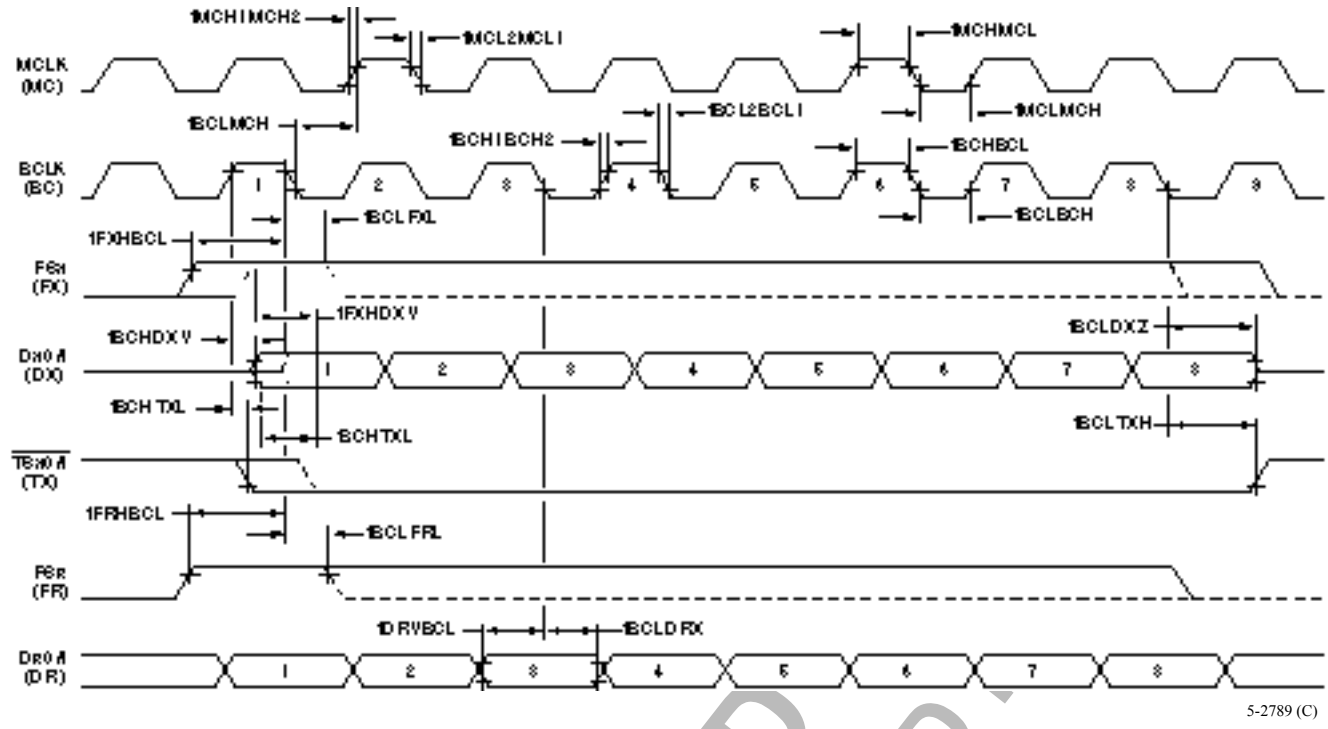
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
fMCLK	Frequency of MCLK—Selection Frequency Is Programmable (See Table 3.)	—	—	1536	—	kHz
			—	1544	—	kHz
			—	2048	—	kHz
			—	4096	—	kHz
tMCHMCL	Time of MCLK High	Measured from V_{IH} to V_{IH}	80	—	—	ns
tMCLMCH	Time of MCLK Low	Measured from V_{IL} to V_{IL}	80	—	—	ns
tMCH1MCH2	Rise Time of MCLK	Measured from V_{IL} to V_{IH}	—	—	30	ns
tMCL2MCL1	Fall Time of MCLK	Measured from V_{IH} to V_{IL}	—	—	30	ns
tBCLMCH	Hold Time, BCLK Low to MCLK High	—	50	—	—	ns
tFSLFSH	Period of FS_X or FS_R Low	Measured from V_{IL} to V_{IL}	1	—	—	MCLK Period

Timing Characteristics (continued)

Table 20. PCM Interface Timing (See Figures 4 and 5.)

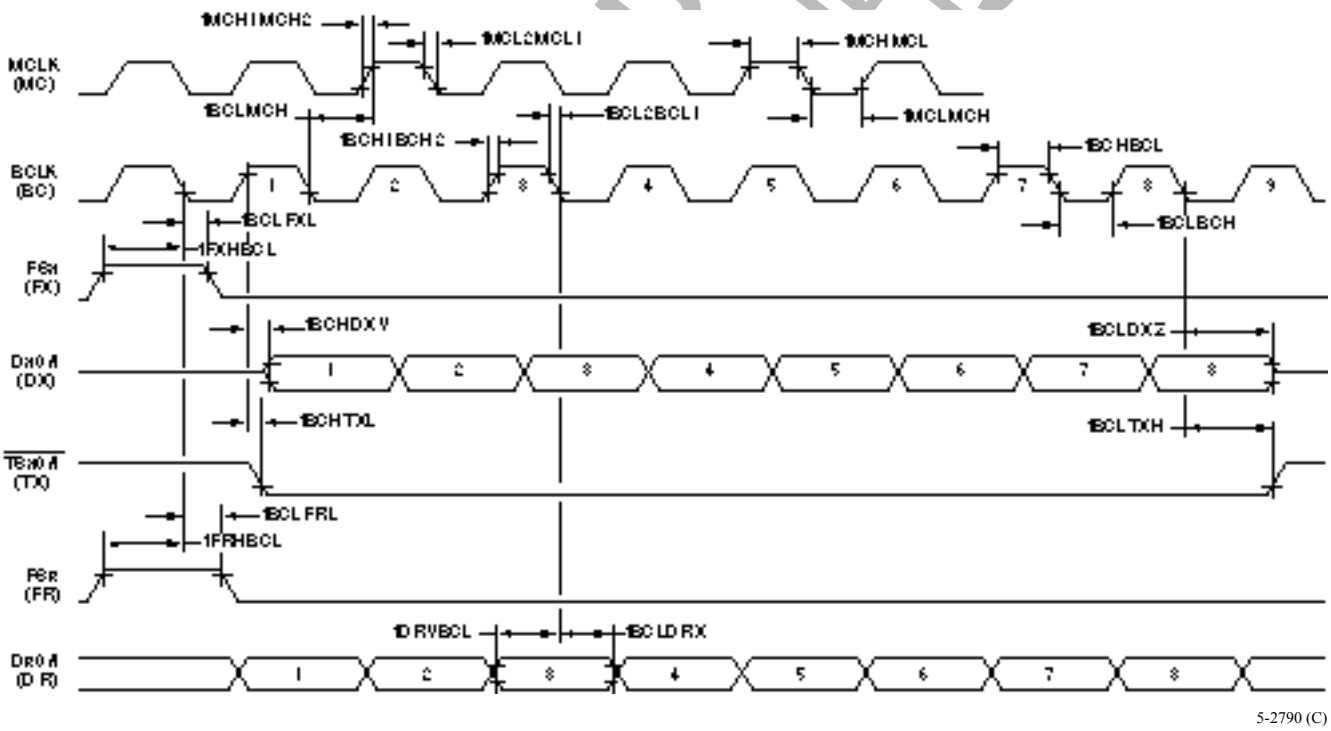
Symbol	Parameter	Test Conditions	T_A (°C)	Min	Max	Unit
fBCLK	Frequency of BCLK (can vary from 64 kHz to 4096 kHz in 8 kHz increments)	—	—	64	4096	kHz
tBCHBCL	Time of BCLK High	Measured from V_{IH} to V_{IH}	—	80	—	ns
tBCLBCH	Time of BCLK Low	Measured from V_{IL} to V_{IL}	—	80	—	ns
tBCH1BCH2	Rise Time of BCLK	Measured from V_{IL} to V_{IH}	—	—	30	ns
tBCL2BCL1	Fall Time of BCLK	Measured from V_{IH} to V_{IL}	—	—	30	ns
tBCLFXL tBCLFRL	Hold Time, BCLK Low FSX/R to High or Low	—	—	30	—	ns
tFXHBCL tFRHBCL	Setup Time FSX/R, High to BCLK Low	—	—	30	—	ns
tBCHDXV	Delay Time, BCLK High to Data Valid	Load = 100 pF plus two LSTTL loads	—	—	90	ns
tBCLDXZ	Delay Time, BCLK Low to DX0/1 Disabled if FSX Low, FSX Low to DX0/1 Disabled if Eighth BCLK Low, or BCLK High to DX0/1 Disabled if FSX High	—	–40 to 0	10	80	ns
			0 to 85	15	80	ns
tBCHTXL	Delay Time, BCLK High to $\overline{TS}$X Low if FSX High, or FSX High to $\overline{TS}$X Low if BCLK High	Load = 100 pF plus two LSTTL loads	—	—	60	ns
tBCLTXH	High-impedance Time, BCLK Low to $\overline{TS}$X High if FSX Low, or FSX BCLK High to $\overline{TS}$X High if FSX High	—	—	15	60	ns
tFXHDXV	Delay Time, FSX/R High to Data Valid	Load = 100 pF plus two LSTTL loads, applies if FSX/R rises later than BCLK rising edge in nonde-layed-data mode only	—	—	80	ns
tDRVBCL	Setup Time, DR0/1 Valid to BCLK Low	—	—	30	—	ns
tBCLDRX	Hold Time, BCLK Low to DR0/1 Invalid	—	–40 to 0	15	—	ns
			0 to 85	20	—	ns
tBCLMCH	BCLK Low to MCLK High at the End of the First Data Bit Period	—	—	50	—	ns

Timing Characteristics (continued)



Note: Bit 1 = sign bit.

Figure 4. Nondelayed-Data Timing Mode



Note: Bit 1 = sign bit.

Figure 5. Delayed-Data Timing Mode

Timing Characteristics (continued)

Table 21. Serial Control Port Timing (See Figure 6.)

Symbol	Parameter	Test Conditions	Min	Max	Unit
fCCLK	Frequency of CCLK	—	—	2048	kHz
tCCHCCL	Time of CCLK High	Measured from V_{IH} to V_{IH}	160	—	ns
tCCLCCH	Time of CCLK Low	Measured from V_{IL} to V_{IL}	160	—	ns
tCCH1CCH2	Rise Time of CCLK	Measured from V_{IL} to V_{IH}	—	50	ns
tCCL2CCL1	Fall Time of CCLK	Measured from V_{IH} to V_{IL}	—	50	ns
tCCLCSL	Hold Time, CCLK Low to $\overline{CS}$ Low	Measured from first CCLK low transition	10	—	ns
tCCLCSH	Hold Time, CCLK Low to $\overline{CS}$ High	Measured from eighth CCLK low transition	100	—	ns
tCSLCCH	Setup Time, $\overline{CS}$ Transition to CCLK Low	—	60	—	ns
tCSHCCH	Setup Time, $\overline{CS}$ Transition to CCLK High	—	50	—	ns
tCIVCCL	Setup Time, CI Data In to CCLK Low	—	50	—	ns
tCCLCIX	Hold Time, CCLK Low to CI Invalid	—	50	—	ns
tCCHCOV	Delay Time, CCLK High to CO Data Out Valid	Load = 100 pF plus 2 LSTTL loads	—	80	ns
tCSLCOV	Delay Time, $\overline{CS}$ Low to CO Valid	Applies only if separate $\overline{CS}$ used for byte 2	—	80	ns
tCSHCOZ	Delay Time, $\overline{CS}$ High to CO High Impedance	Applies when $\overline{CS}$ high occurs before ninth CCLK high	15	80	ns

Table 22. Interface Latch Timing (See Figure 6.)

Symbol	Parameter	Test Conditions	Min	Max	Unit
tILXCCL	Setup Time, IL to Eighth CCLK of Byte 1	Interface latch inputs only	100	—	ns
tCCLILX	Hold Time, IL Valid from Eighth CCLK Low (byte 1)	—	50	—	ns
tCCLILV	Delay Time CCLK 8 of Byte 2 to IL	Interface latch outputs only C_L = 50 pF	—	200	ns

Table 23. Master Reset Pin

Symbol	Parameter	Min	Max	Unit
tMRHRML	Duration of Master Reset High	1	—	µs

Timing Characteristics (continued)

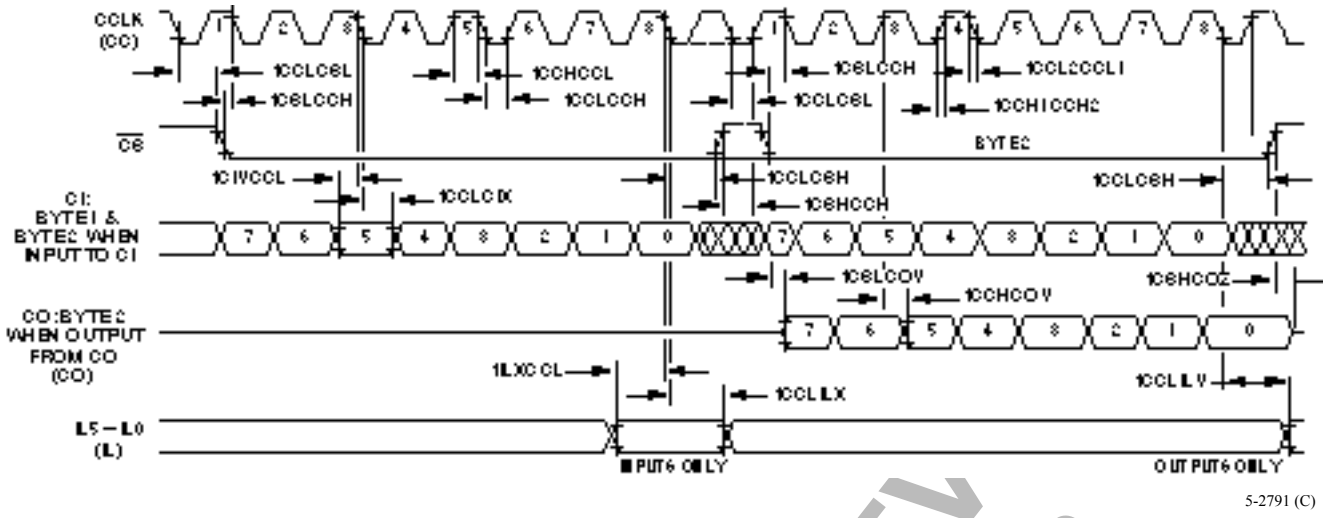


Figure 6. Serial Control Port Timing

Applications

Figure 7 illustrates a T7570 codec interfaced to a L7554 SLIC. Interface components were chosen for a basic 600 Ω resistive only termination and balance network. Overall receive path gain is 0 dB (PCM to T/R). Overall transmit path gain is –2 dB (T/R to PCM). Codec receive gain is 0 dB. The signal level returned to VFXI is –3.658 dBm. This satisfies the transmission level point requirement for hybrid cancellation. That is, the signal at VFXI relative to the output at VFRO must be within –2.5 dB to –10.25 dB. Transmit gain of the codec is set at +1.658 dB in order to achieve a transmission level point at Dx of –2 dBm.

Transmit and receive paths are capacitively coupled to accommodate different SLIC and codec bias levels. The codec's inputs are self-biased so that no additional external resistors are necessary with ac coupling. Capacitor values are sized appropriately to pass low-frequency requirements of relevant gain versus frequency templates. Resistive values were ascertained from SLIC documentation.

An optional 20 kΩ resistor from RCVN to ground and a 30 pF capacitor across RGP can be added for stability.

Gain and hybrid-balance register values are shown in hex. Gain values were obtained from Tables 8 and 9. Hybrid- balance values were obtained by removing the codec and inserting a network analyzer to measure the phase and gain returned by the loop to VFXI when a signal is injected at VFRO. Gain and phase are then measured at 14 frequencies. The results obtained from this exercise are plugged into the hybrid-balance software that provides the register settings as shown.

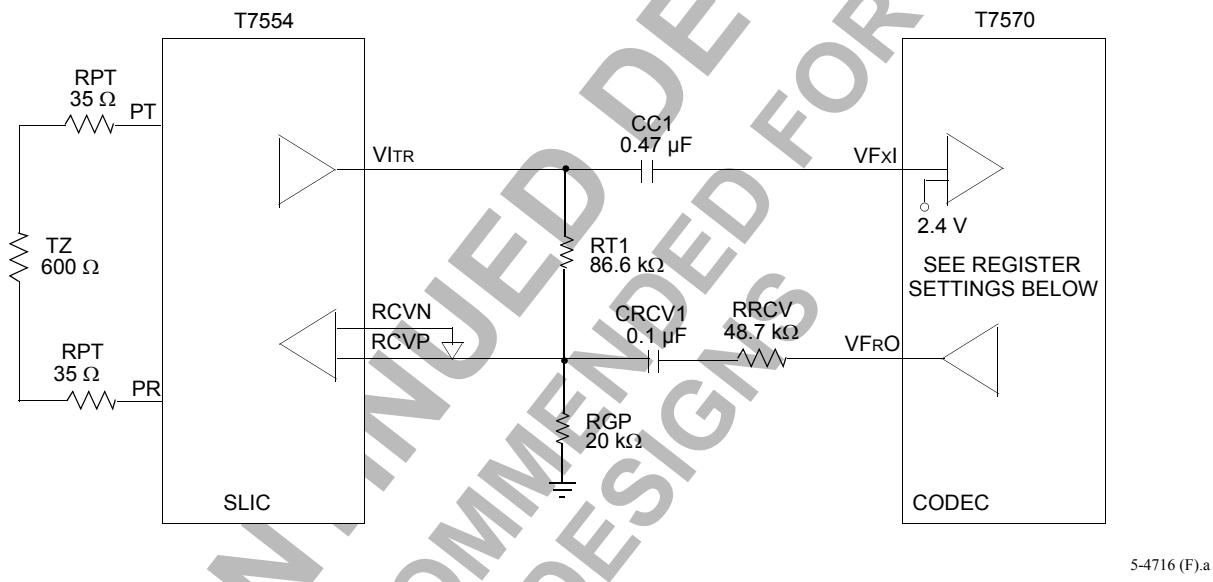


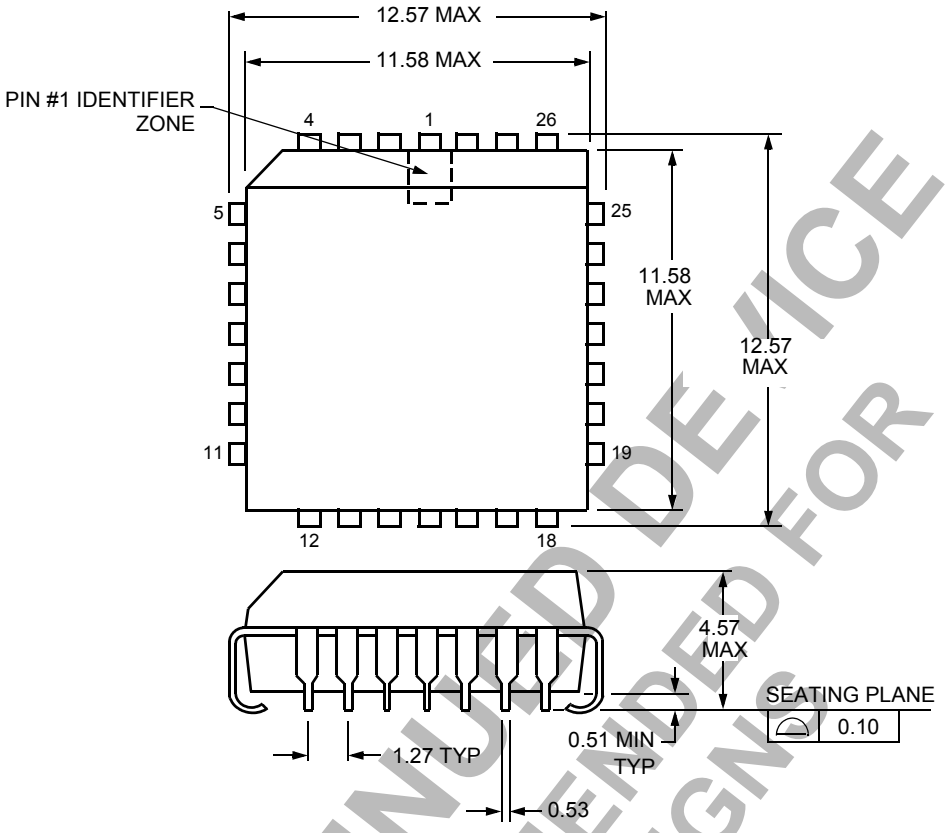
Figure 7. 600 Ω Resistive SLIC Interface

Register Settings			
Register	**Register Number**	**Value**	**Description**
RX GAIN	04	AE	0 dB
TX GAIN	05	AE	1.658 dB
HYBRID 1	06	A4	—
HYBRID 2	07	51	—
HYBRID 3	08	88	—

Outline Diagrams

28-Pin PLCC

Dimensions are shown in inches.



5-2608 (F)r.4

Ordering Information

Device Code	Package	Temperature	Comcode
T - 7570 - - - ML2	28-Pin PLCC	–40 °C to +85 °C	107055782
T - 7570 - - - ML2 -TR	28-Pin PLCC, Tape and Reel	–40 °C to +85 °C	107056525