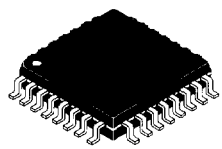
MC141624

Product Proposal

Advanced Comb Filter-I (ACF-I)

The Advanced Comb Filter–I is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signal from the NTSC composite signal. The ACF–I minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc signal. This filter allows a video signal input of an extended frequency bandwidth by using a 4xfsc clock. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–In High Speed 8–Bit Two Step A/D Converter
- One Line Memories (910 Bytes)
- Advanced Comb–I Process
- Built–In Two High Speed 8–Bit D/A Converter
- Built–In 4xfsc PLL Circuit
- Built–In Clamp Circuit
- On–Chip Reference Voltage for A/D Converter



FU SUFFIX
32– LEAD QFP
CASE 873–01

SP SUFFIX
32–LEAD SDIP
CASE TBD

ORDERING INFORMATION

MC141624FU	Quad Flat Pack (QFP)
MC141624SP	SDIP

MOTOS286

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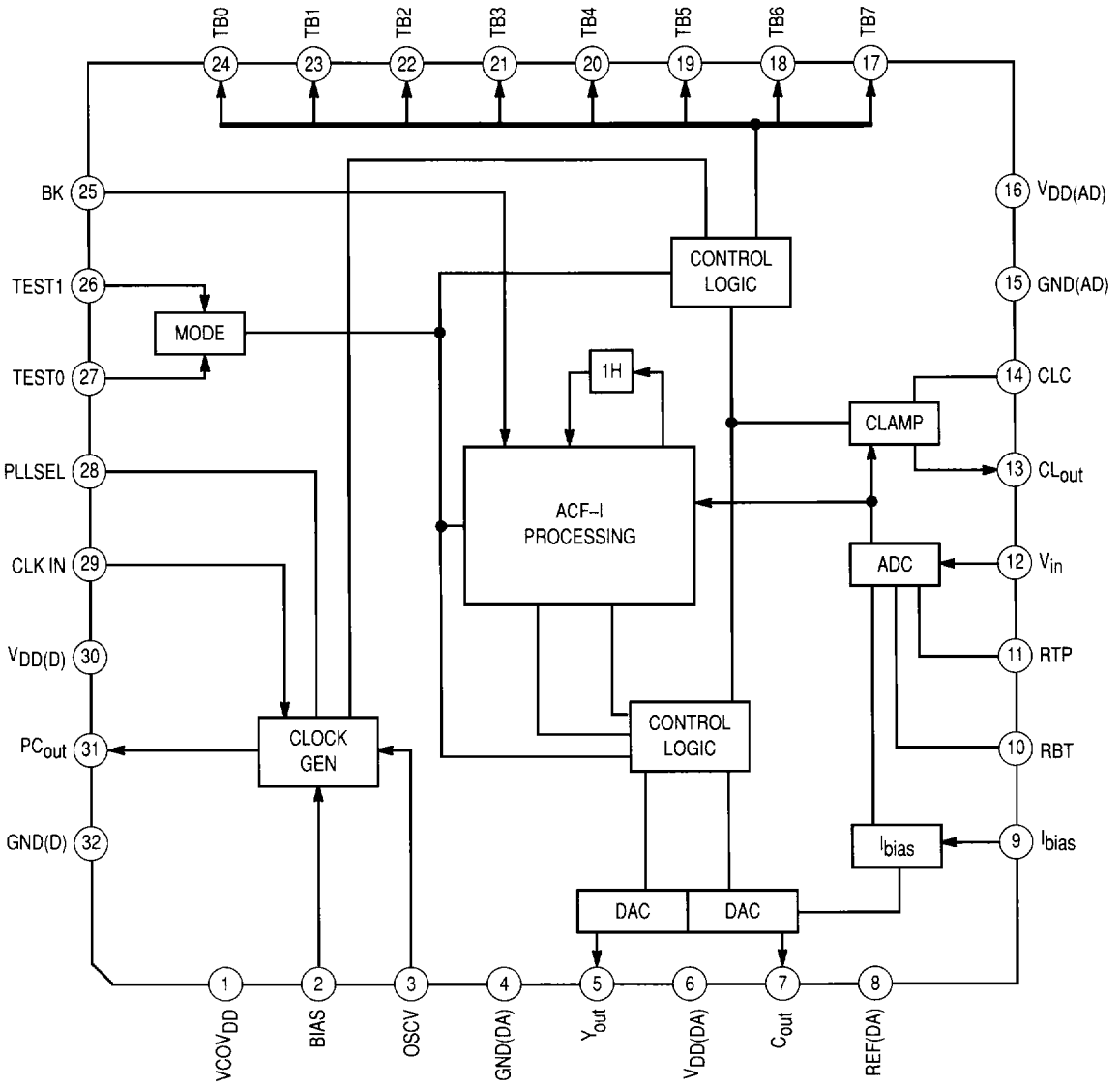
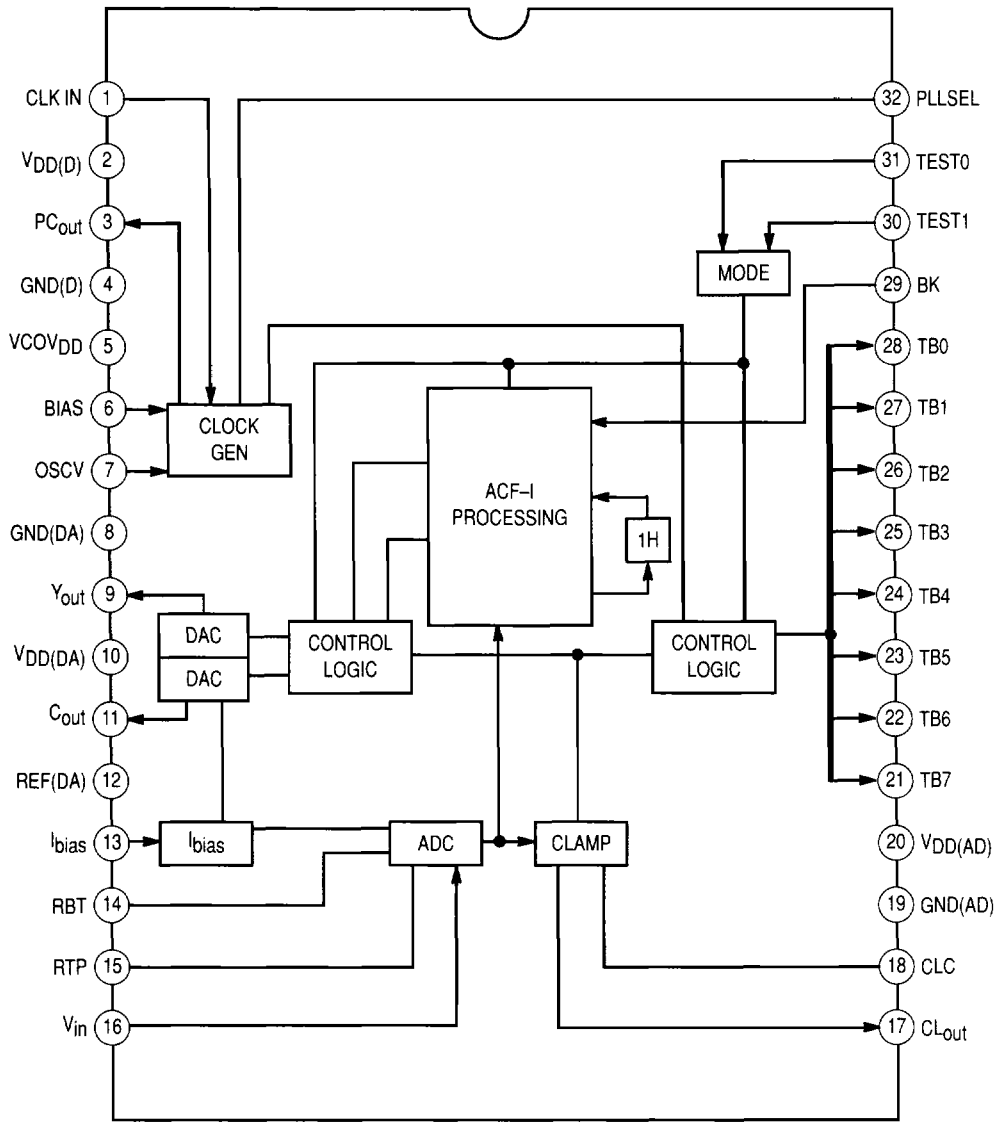
BLOCK DIAGRAM
(32 QFP)



BLOCK DIAGRAM
(32 SDIP)



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	− 0.5 to + 6.0	V
DC Input Voltage (Referenced to GND)	V_{in}	− 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	− 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{stg}	− 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V	
Operating Supply Current (at Normal Mode)	I_{CC}	—	50	60	mA	
Operating Power Dissipation (at Normal Mode)	P_D	—	250	315	mW	
Ambient Operating Temperature	T_A	− 20	—	75	°C	

* $V_{CC(AD)}$, $V_{CC(DA)}$, $V_{CC(D)}$ voltage.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Subcarrier Input Frequency		f_c	—	3.579545	—	MHz	1
Clock Frequency		CLK	—	14.31818	—	MHz	2
FSC Clock Input Level		V_{fc}	1	—	—	Vp-p	3
High Level Input Voltage	CLK	V_{ICH}	3.15	—	—	V	
Low Level Input Voltage	CLK	V_{ICL}	—	—	1.1	V	
Clock Duty Cycle	CLK	Dty	45	50	55	%	

NOTES:
1. Color subcarrier input [FSC = (455/2)fh] locked on the burst signal of the input video signal. AC coupling input by external capacitor.
2. The internal circuit operates by four times clock using FSC–pin input at normal (FSC) mode.
3. Sine wave input.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.0	± 1.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Top Reference Level	V_{TPS}	2.4	2.5	2.6	V
Bottom Reference Level	V_{BTS}	0.4	0.5	0.6	V
Maximum Analog Input Range During Self Reference	V_{ins}	1.9	2.0	2.1	Vp-p

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	TE0, TE1, BK, TB0 – TB4	V_{IH}	3.15	—	—	V
Low Level Input Voltage	TE0, TE1, BK, TB0 – TB4	V_{IL}	—	—	1.1	V
Input Leakage Current [V_{in} = $V_{CC(D)}$ or GND(D)]	TE0, TE1, BK, TB0 – TB4	I_{inl}	—	—	± 10	µA

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band-Pass Filter Bandwidth (at – 3 dB)	—	—	± 0.75	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	Vp-p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	Vp-p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

ADC – DAC GENERAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Gain		—	– 4.4	—	dB
Output Bandwidth (at – 3 dB)		5.5	5.9	6.4	MHz
Differential Gain	DG	—	—	5	%
Differential Phase	DP	—	—	5	Deg
Bias Current (at I_{bias} = 10 kohm)	I_{bias}	—	135	—	µA

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Voltage*	V_{clys}	—	0.5	—	V

* At using the internal clamp circuit when connecting V_{in} – CL_{out}.

BK CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
BK Switching Time, at Normal Mode		—	349	—	ns

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode (24.5 Clock)		—	1.711	—	µs

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	$VCOV_{CC}$	Power supply for VCO.
2	BIAS	Reference for VCO. Generally connected to GND(D) through an external resistor.
3	OSCV	VCO controlled voltage input. Generally connected to PCO through an external loop filter.
4	GND(AD)	GND for D/A converter.
5	Y_{out}	Luminance signal output.
6	$V_{DD(DA)}$	Power supply for D/A converter.
7	C_{out}	Chrominance signal output.
8	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 μF).
9	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
10	RBT	Bottom reference for A/D converter. Supplies bottom reference voltage internally.
11	RTP	Top reference for A/D converter. Supplies top reference voltage internally.
12	V_{in}	A/D converter input.
13	CL_{out}	Voltage output for clamp. Clamps an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
14	CLC	Clamp time constant setting pin.
15	GND(AD)	GND for A/D converter.
16	$V_{CC(AD)}$	Power supply for A/D converter.
17 – 24	TB7 – TB0	Digital interface 1, input/output. Generally GND(D) level.
25	BK	Non–color signal processing mode. Generally GND(D) level.
26, 27	TEST1, TEST0	Test mode input. Generally GND level.
28	PLLSEL	CLK input mode select. PLLSEL "L": 4*PLL operation.
29	CLKIN	CLK input. ac coupling input by external capacitor. PLLSEL "L": subcarrier, PLLSEL "H": 4*subcarrier.
30	$V_{DD(D)}$	Power supply for digital circuit.
31	PC_{out}	Phase comparator output.
32	GND(D)	GND for digital circuit.

DEVICE DESCRIPTION

INTRODUCTION

The Advanced Comb Filter–I (ACF–I) is a high–performance HCMOS digital filter with built–in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–I minimizes the problems often generated by Y/C separation such as dot–crawl and cross–color. It uses a 14.3 MHz clock that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. The built–in 4xfsc PLL circuit allows a subcarrier signal input, from which a 4xfsc clock is generated for video signal processing. This arrangement allows a video signal input of an extended frequency bandwidth. The built–in A/D and D/A converters allow easy connection to analog video circuits.

DESCRIPTION

There are four major functions represented on the block diagram. The first block is the analog–to–digital conversion block. The high speed 8–bit binary A/D converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz, which is four times the color subcarrier frequency. The maximum analog video input is 2.0 V p–p.

The fourth block is a 4xfsc CLK generator. The internal PLL can be phase locked to an external NTSC subcarrier to generate the necessary 4xfsc clock, or selected to process an externally supplied 4xfsc clock.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The input voltage range is determined by the value of the reference voltage inputs, RBT and RTP. This produces a maximum conversion value of 2.0 V p–p maximum video input signal for $V_{CC(AD)}$ of 5 V. A self–bias function generating V_{TP} = 2.5 V, V_{BT} = 0.5 V can be realized by connecting the internal A/D converter reference voltage supply with the A/D converter reference pin. The sampling clock frequency of the A/D converter is 14.3 MHz which is four times the color subcarrier frequency.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the digital value of the clamp level ($04) with the A/D converter output code. The clamp voltage is output by the CL_{out} pin.

Advanced Comb Filter–I

The Advanced Comb Filter–I is a digital comb filter developed for use in the NTSC system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. The clock frequency is 14.3 MHz, which is four times the NTSC subcarrier.

The BK pin is used to select as output either the filtered Y/C signal or the unfiltered composite signal. Table 1 shows the relationship of the BK pin to each output.

Table 1. BK Function

BK Pin	Y_{out}	C_{out}
L	Luminance	Chrominance
H	Composite	Chrominance

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 Vp–p. The sampling clock of the D/A converter is 14.3 MHz.

Clock Generation Circuit

The internal PLL can be selected to operate in either of two modes; an X4 mode used to generate a 4xfsc clock from a normal NTSC color subcarrier, and an X1 mode when a 4xfsc signal is available. An "L" applied to the PLLSEL pin sets the PLL to the X4 mode and an "H" sets it to the X1 mode.

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141624, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141624. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141624, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero,

the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built–in clamp circuit, connect CL_{out} to V_{in} and input signals after ac coupling by using a high–performance, high–frequency capacitor of 1 to 0.1 μF capacitance. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

AD Reference Pin

The RTP and RBT pins have a self–bias function that internally generates V_{TP} = 4.6 V and V_{BT} = 1.55 V. It acknowledges the AD converter analog input dynamic range. A stable performance can be achieved by applying a high–performance frequency capacitor as close as possible to the RTP and RBT pins and bypassing to GND(AD).

A 0.1 μF multi-layer ceramic capacitor and a 10 μF tantalum capacitor are recommended.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected with GND(AD). Select a capacitor which minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the VCR signal to $V_{CC(AD)}$ side is accelerated. When the resistor value is reduced, the shift speed of the VCR signal to GND(AD) is accelerated. If the resistor value is too small at this point, sagging will appear in the VCR signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor value and capacity.

DA Reference

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance frequency capacitor as close to the pin as possible.

A 0.1 μF multi ceramic capacitor is recommended.

Clock Input

The clock frequency input is 3.58 MHz during normal (fsc) mode, and 14.31818 MHz during the other modes. The minimum input level is 1.0 Vp–p. It should be synchronized with the input of the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits so it does not have an effect on other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level except during the digital input comb filtering mode.

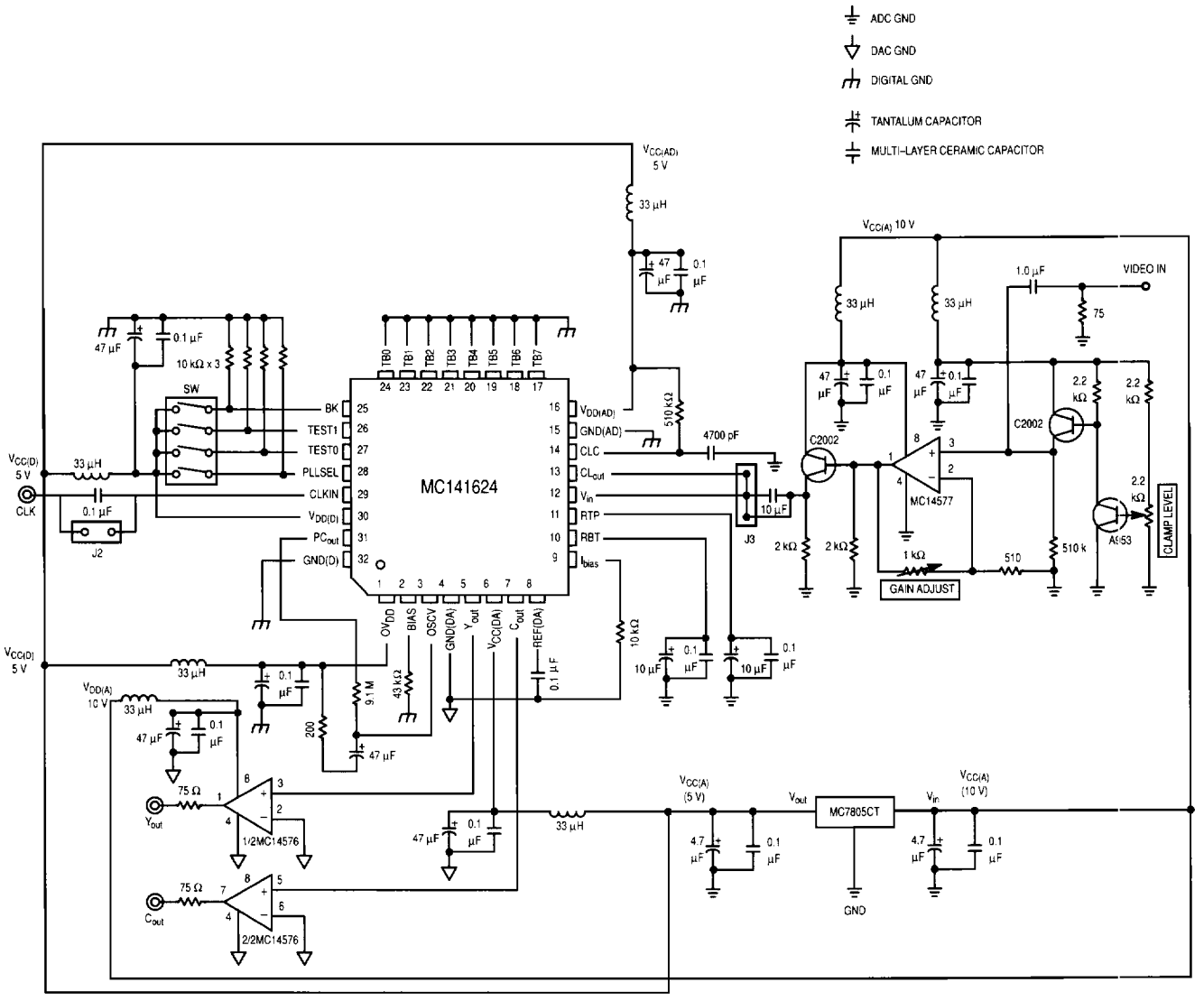
I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

Latch–Up

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ are power supplies, independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

APPLICATION CIRCUIT



EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 6 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 7. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 7. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

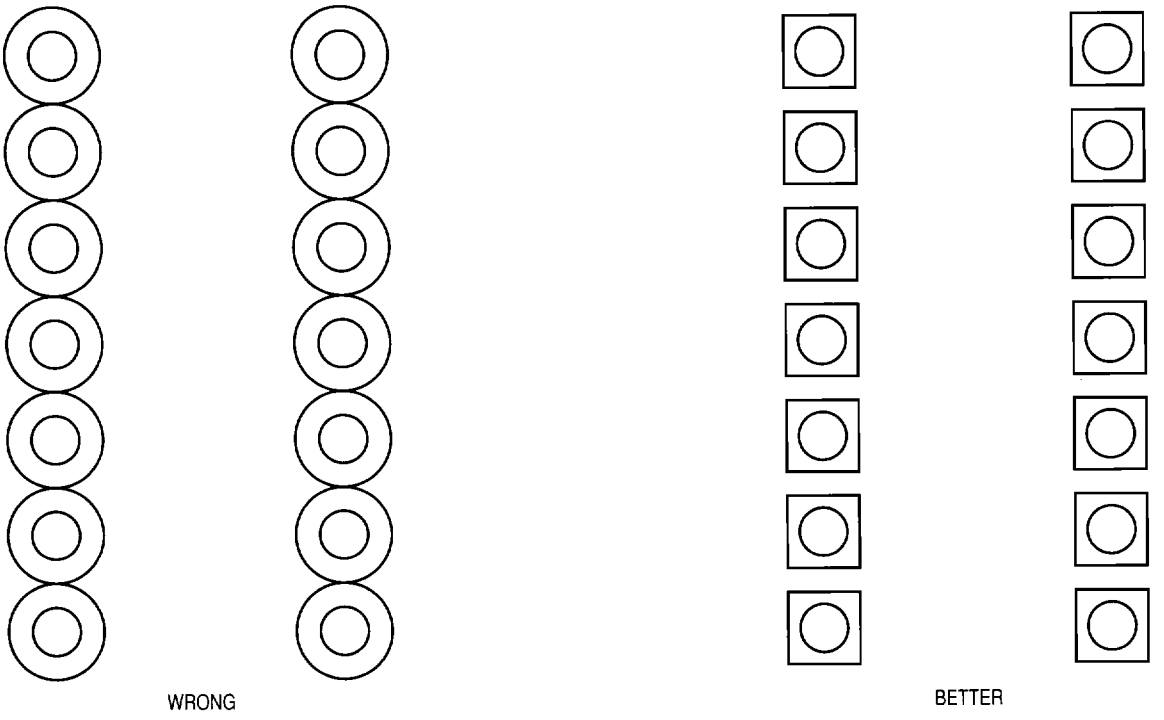


Figure 1.

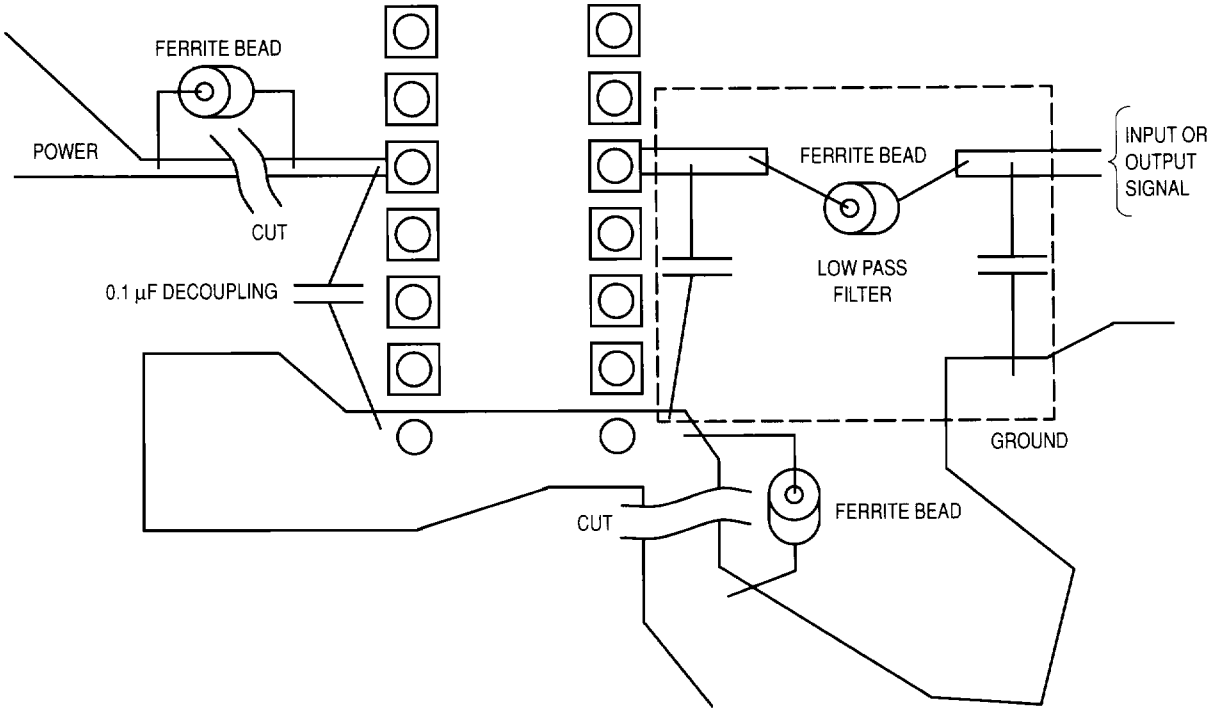
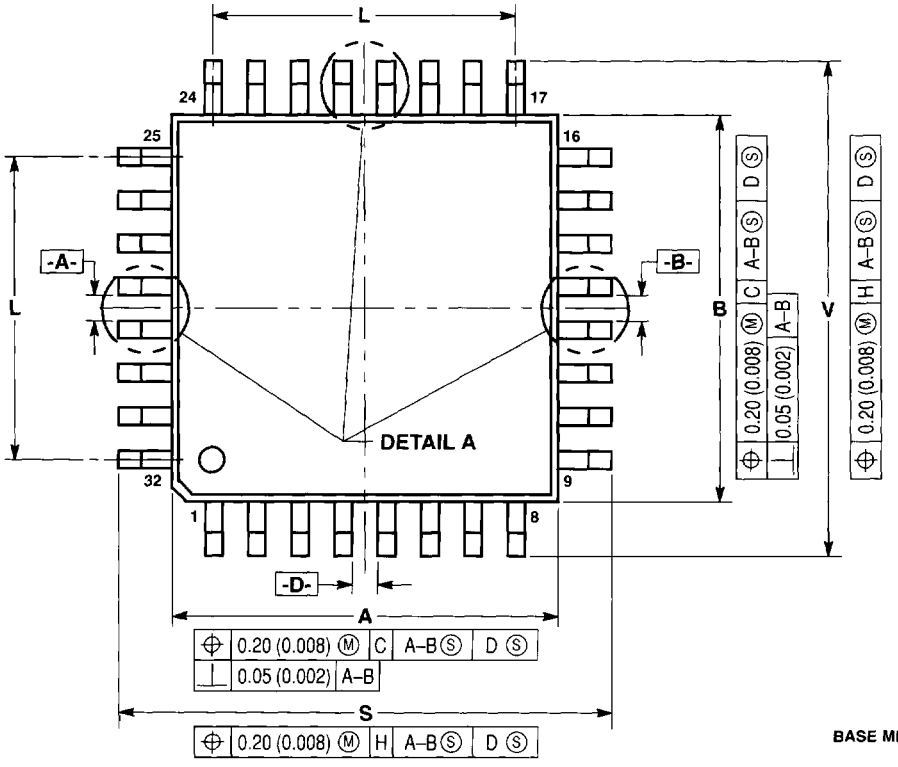
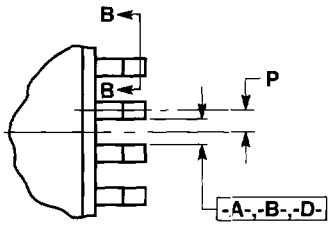


Figure 2.

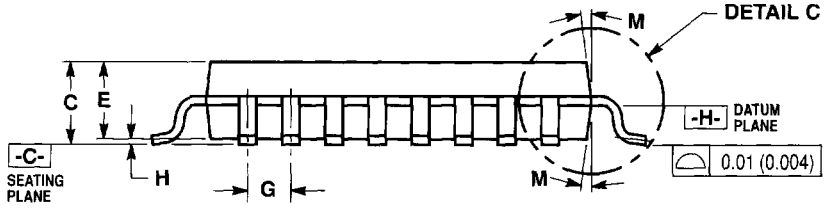
PACKAGE DIMENSIONS

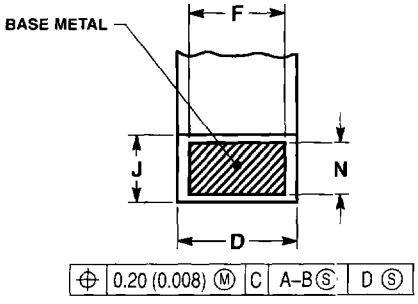
FU SUFFIX
32–LEAD QFP
CASE 873–01



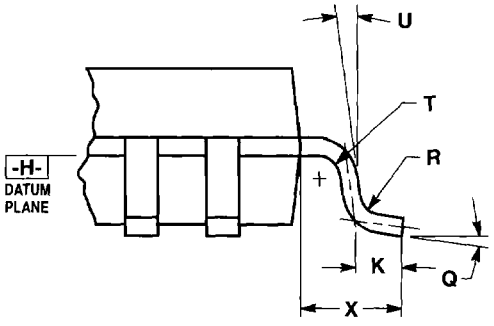


DETAIL A





SECTION B-B
VIEW ROTATED 90° CLOCKWISE



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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◊ 1ATX31846–0 PRINTED IN USA 3/95 IMPERIAL LITHO 12604 5,000 MOS D–A MM YFAMAA

MC141624/D