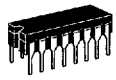
Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

MC10117

The MC10117 is a dual 2–wide 2–3–input OR–AND/OR–AND–Invert gate. This general purpose logic element is designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t_r, t_f = 2.2 ns typ (20%–80%)

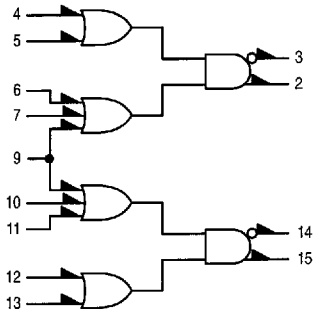


L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

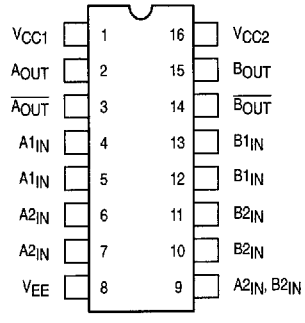
FN SUFFIX
PLCC
CASE 775–02

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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MOTOROLA

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		29		20	26		29	mAdc
Input Current	I_{inH}*	6 9 4		425 560 390			265 350 245		265 350 245	µAdc
	I_{inL}	4	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3	–1.060 –1.060	–0.890 –0.780	–0.960 –0.960		–0.810 –0.700	–0.890 –0.890	–0.700 –0.590	Vdc
Output Voltage Logic 0	V_{OL}	2 3	–1.890 –1.890	–1.675 –1.675	–1.850 –1.850		–1.650 –1.650	–1.825 –1.825	–1.615 –1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	–1.080 –1.080		–0.980 –0.980			–0.910 –0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		–1.655 –1.655			–1.630 –1.630		–1.595 –1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+} t_{4-2-} t_{4+3-} t_{4-3+}	2 2 3 3	1.4 1.4 1.4 1.4	3.9 3.9 3.9 3.9	1.4 1.4 1.4 1.4	2.3 2.3 2.3 2.3	3.4 3.4 3.4 3.4	1.4 1.4 1.4 1.4	3.8 3.8 3.8 3.8	
Rise Time (20 to 80%)	t_{2+} t_{3+}	2 3	0.9 0.9	4.1 4.1	1.1 1.1	2.2 2.2	4.0 4.0	1.1 1.1	4.6 4.6	
Fall Time (20 to 80%)	t_{2-} t_{3-}	2 3	0.9 0.9	4.1 4.1	1.1 1.1	2.2 2.2	4.0 4.0	1.1 1.1	4.6 4.6	

* Inputs 4, 5, 12 and 13 have same I_{inH} limit.
Inputs 6, 7, 10 and 11 have same I_{inH} limit.

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ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}*	6	4				8	1, 16
			9	9				8	1, 16
			4		4			8	1, 16
		I_{inL}	4		9			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	4, 9				8	1, 16
			3					8	1, 16
Output Voltage	Logic 0	V_{OL}	2					8	1, 16
			3	4, 9				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2	9		4		8	1, 16
			3				4	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2				4	8	1, 16
			3	9		4		8	1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		t_{4+2+}	2	9		4	2	8	1, 16
		t_{4-2-}	2	9		4	2	8	1, 16
		t_{4+3-}	3	9		4	3	8	1, 16
		t_{4-3+}	3	9		4	3	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2	9		4	2	8	1, 16
		t_{3+}	3	9		4	3	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2	9		4	2	8	1, 16
		t_{3-}	3	9		4	3	8	1, 16

* Inputs 4, 5, 12 and 13 have same I_{inH} limit.
Inputs 6, 7, 10 and 11 have same I_{inH} limit.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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