

# MP87L92

## Low Voltage CMOS 12-Bit High-Speed Analog-to-Digital Converter with Serial Logic Interface Port



March 1998-3

### FEATURES

- 3.3 V Operation
- 12-Bit ADC with DNL =  $\pm 1$  LSB, INL =  $\pm 2$  LSB
- Sampling Frequency 1 MHz (typ)
- Rail-to-Rail Input Range
- $V_{REF}$  Range: 1.5 V to  $V_{DD}$
- CMOS Low Power: 25 mW (typ)
- Spaced Ladder Taps for Non-Linear Transfer Function Creation
- Binary and Two's Complement Digital Output Mode
- Serial Port
- Underflow Outputs
- Precision Aperture Output
- Latch-Up Proof
- ESD Protection: 2000 V Minimum

### APPLICATIONS

- Instrumentation
- DAS
- Radar
- Medical Imaging
- Ultrasound
- Broadcast and Studio Video
- Magnetic Resonance Signal Acquisition
- Digital Oscilloscopes
- Spectrum Analysis
- Digital Radio

### GENERAL DESCRIPTION

The MP87L92 is a 12-bit 2-step high speed Analog-to-Digital Converter with DNL =  $\pm 1$  LSB and INL =  $\pm 2$  LSB. The MP87L92 contains an internal track and hold which allows for analog input signals as fast as 1 MHz and can convert signals at a 1 MSPS rate.

The MP87L92 operates with a single supply at +3.3 V. Separate pins for reference ladder terminals and power

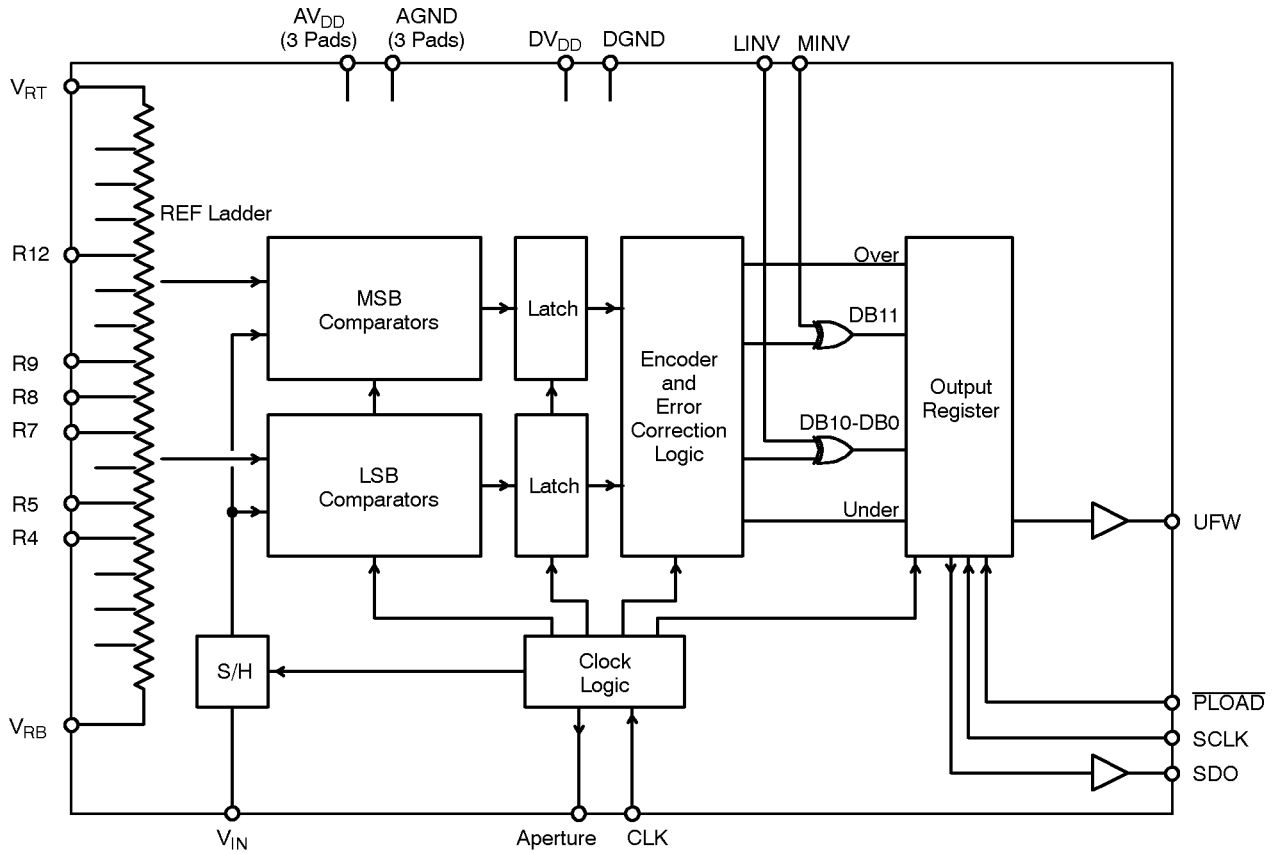
supplies allow flexibility for various  $A_{IN}$ ,  $\Delta V_{REF}$ , and power supply ranges.

Data is presented at the output port every clock cycle after a 2.5 cycle pipeline delay. The digital output port is equipped with a serial data port. LINV and MINV enable binary and 2's complement data formatting. Through the 6 ladder tap pins, transfer function adjustment, linearity, and speed enhancement can be accommodated.

### ORDERING INFORMATION

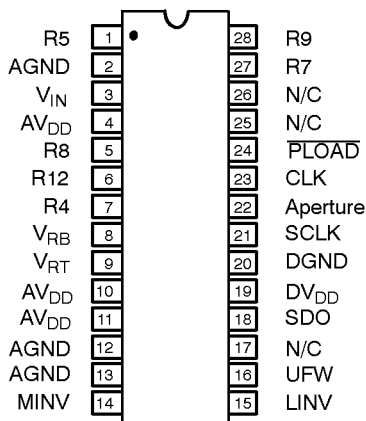
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	-40 to +85°C	MP87L92AS	$\pm 1$	$\pm 3$
PDIP	-40 to +85°C	MP87L92AN	$\pm 1$	$\pm 3$

## SIMPLIFIED BLOCK DIAGRAM

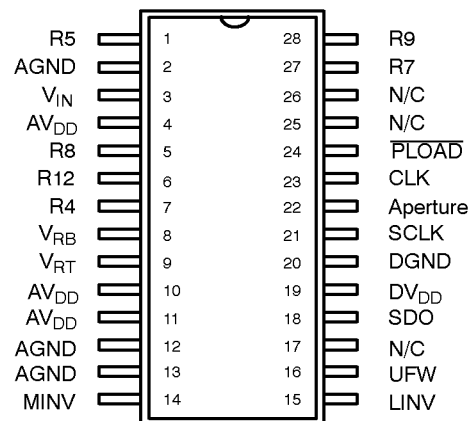


## PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin PDIP (0.600")



28 Pin SOIC (EIAJ 0.335")

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	R5	Ref. Resistor Ladder Tap (5/16 $V_{REF}$ )
2	AGND	Analog Ground
3	$V_{IN}$	Analog Input
4	$AV_{DD}$	Analog Positive Supply
5	R8	Ref. Resistor Ladder Tap (1/2 $V_{REF}$ )
6	R12	Ref. Resistor Ladder Tap (3/4 $V_{REF}$ )
7	R4	Ref. Resistor Ladder Tap (1/4 $V_{REF}$ )
8	$V_{RB}$	Negative Reference
9	$V_{RT}$	Positive Reference
10	$AV_{DD}$	Analog Positive Supply
11	$AV_{DD}$	Analog Positive Supply
12	AGND	Analog Ground
13	AGND	Analog Ground
14	MINV	Invert MSB (Active High)
15	LINV	Invert LSB (Active High)
16	UFW	Underflow Bit
17	N/C	No Connection
18	SDO	Serial Data Out
19	$DV_{DD}$	Digital Positive Supply
20	DGND	Digital Ground
21	SCLK	Serial Clock
22	Aperture	Aperture Delay Sync
23	CLK	Clock
24	$\overline{PLOAD}$	Serial Shift Register Data Load
25	N/C	No Connection
26	N/C	No Connection
27	R7	Ref. Resistor Ladder Tap (7/16 $V_{REF}$ )
28	R9	Ref. Resistor Ladder Tap (9/16 $V_{REF}$ )

## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $V_{DD} = 3\text{ V}$ ,  $FS = 500\text{ kHz}$  (50% Duty Cycle),

$V_{RT} = 3.0\text{ V}$ ,  $V_{RB} = \text{AGND}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	25°C		Max	Units	Test Conditions/Comments
		Min	Typ			
<b>KEY FEATURES</b>						
Resolution		12			Bits	
Maximum Sampling Rate	FS	0.5	1		MHz	
<b>ACCURACY<sup>1</sup></b>						
Differential Non-Linearity	DNL			±1	LSB	Best Fit Line (Max INL - Min INL)/2
Integral Non-Linearity	INL			±3	LSB	
Zero Scale Error	EZS		+20		LSB	
Full Scale Error	EFS		-20		LSB	
<b>REFERENCE VOLTAGES</b>						
Positive Ref. Voltage	$V_{REF(+)}$	2.0		$AV_{DD}$	V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND			V	
Differential Ref. Voltage <sup>3</sup>	$V_{REF}$	2.0		$AV_{DD}$	V	
Ladder Resistance	$R_L$		550		Ω	
<b>ANALOG INPUT</b>						
Input Bandwidth (-3 dB) <sup>4</sup>	BW		5		MHz	
Input Voltage Range	$V_{IN}$	$V_{REF(-)}$		$V_{REF(+)}$	V p-p	
Input Capacitance Sample <sup>5</sup>	$C_{IN}$		50		pF	
Input Capacitance Convert <sup>5</sup>			8		pF	
Aperture Delay from Clock	$t_{AP}$		30		ns	
Aperture Delay from Aperture Signal	$t_{AP}$		0		ns	Aperture pin load 5 pF Measured at 50% point
<b>DIGITAL INPUTS</b>						
Logical "1" Voltage	$V_{IH}$	2.5			V	$V_{IN} = \text{DGND to } DV_{DD}$
Logical "0" Voltage	$V_{IL}$			0.5	V	
Leakage Currents <sup>6</sup>	$I_{IN}$				μA	
CLK, $\overline{OE1}$ , $\overline{OE2}$ , MINV, LINV			10		μA	
Input Capacitance			5		pF	
Clock Timing						
Clock Period	$T_S$	1000			ns	
Rise & Fall Time <sup>7</sup>	$t_R, t_F$		15		ns	
"High" Time	$t_{PWH}$	500			ns	
"Low" Time	$t_{PWL}$	500			ns	
Duty Cycle			50		%	
Serial Register Timing						
Shift Clock Period	$t_{SC}$	80			ns	
Shift Clock to Data Delay	$t_{SD}$		30		ns	
Minimum Pulse Width $\overline{PLOAD}$	$t_S$		50		ns	
Clock ↑ to $\overline{PLOAD}$ ↓ For Valid D11	$t_{CP}$		0		ns	
<b>DIGITAL OUTPUTS</b>						
Logical "1" Voltage	$V_{OH}$	$DV_{DD}-0.5$			V	$C_{OUT} = 15\text{ pF}$
Logical "0" Voltage	$V_{OL}$			0.5	V	$I_{LOAD} = 1\text{ mA}$
Tristate Leakage	$I_{OZ}$		1		μA	$I_{LOAD} = 1\text{ mA}$
Data Valid Delay <sup>2</sup>	$t_{DL}$		100		ns	$V_{OUT} = \text{DGND to } DV_{DD}$

## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C			Units	Test Conditions/Comments
		Min	Typ	Max		
<b>POWER SUPPLIES<sup>8</sup></b> (Tmin to Tmax)						
Operating Voltage (AV <sub>DD</sub> , DV <sub>DD</sub> )	V <sub>DD</sub>	3	3.3	3.6	V	
Current (AV <sub>DD</sub> + DV <sub>DD</sub> )	I <sub>DD</sub>		8	12	mA	
<b>AC PARAMETERS</b>						
Signal Noise Ratio	SNR		66		dB	

**Notes:**

- <sup>1</sup> Tester measures code transitions by dithering the voltage of the analog input (V<sub>IN</sub>). The difference between the measured and the ideal code width (V<sub>REF</sub>/4096) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
- <sup>2</sup> Guaranteed. Not tested.
- <sup>3</sup> Specified values guarantee functionality. Refer to other parameters for accuracy.
- <sup>4</sup> -3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- <sup>5</sup> Switched capacitor analog input requires driver with low output resistance.
- <sup>6</sup> All inputs have diodes to DV<sub>DD</sub> and DGND. Input(s) LINV and MINV have internal pull down(s). Input DC currents will not exceed specified limits for any input voltage between DGND and DV<sub>DD</sub>.
- <sup>7</sup> Condition to meet aperture delay specifications (t<sub>AP</sub>, t<sub>AJ</sub>). Actual rise/fall time can be less stringent with no loss of accuracy.
- <sup>8</sup> AGND & DGND pins are connected through the silicon substrate.

**Specifications are subject to change without notice**

## ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)<sup>1, 2, 3</sup>

V <sub>DD</sub> to GND	5.5 V	Storage Temperature	-65 to +150°C
V <sub>RT</sub> & V <sub>RB</sub>	V <sub>DD</sub> +0.5 to GND -0.5 V	Lead Temperature (Soldering 10 seconds)	+300°C
V <sub>IN</sub>	V <sub>DD</sub> +0.5 to GND -0.5 V	Package Power Dissipation Rating @ 75°C	
All Inputs	V <sub>DD</sub> +0.5 to GND -0.5 V	PDIP, SOIC	1050mW
All Outputs	V <sub>DD</sub> +0.5 to GND -0.5 V	Derates above 75°C	14mW/°C

**Notes:**

- <sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- <sup>3</sup> V<sub>DD</sub> refers to AV<sub>DD</sub> and DV<sub>DD</sub>. GND refers to AGND and DGND.

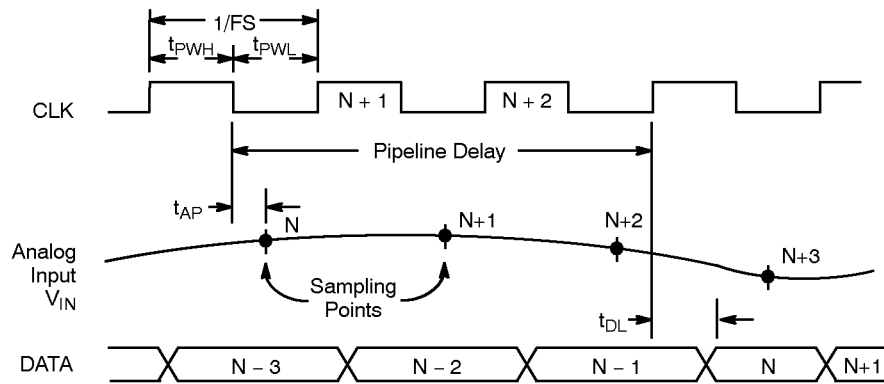


Figure 1. MP87L92 Timing Diagram

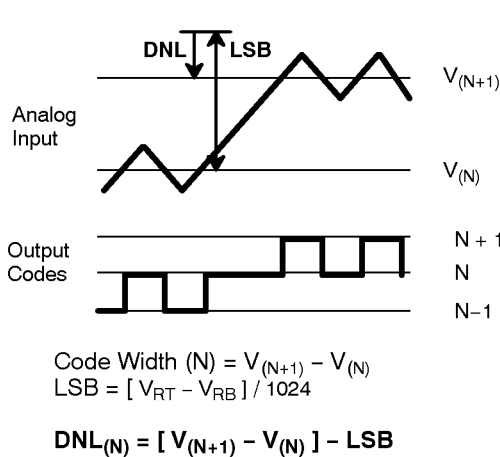


Figure 2. DNL Measurement

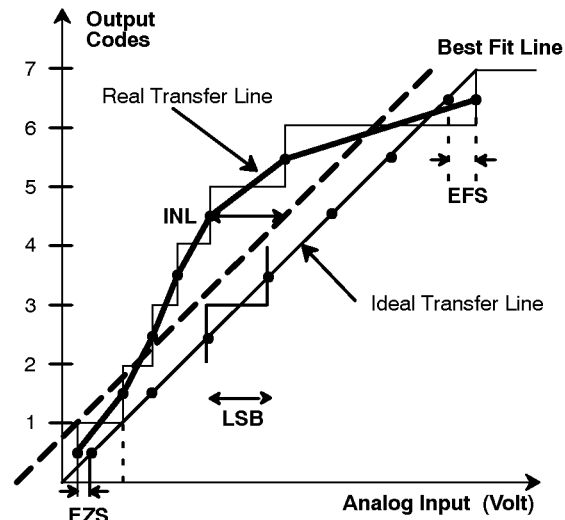


Figure 3. INL Error Calculation

### UFW: Underflow (Output)

This signal indicates when the Analog Input ( $V_{IN}$ ) goes outside the  $V_{RB}$  range, and is normally at a low logic level. When  $V_{IN} < V_{RB}$ , UFW will go high and the data bits will show negative full scale (i.e. all 0's if MINV & LINV are low).

### SDO: Serial Data Output

After the internal shift register is updated using the  $\overline{PLOAD}$  signal, the SDO pin outputs the A/D result starting with the MSB (which appears just after the  $\overline{PLOAD}$  strobe). Each bit is output on the rising edge of SCLK.

### SCLK: Serial Data Port Clock

The SCLK controls the output of the serial port through SDO. SDO is updated on every rising edge of SCLK. The  $\overline{PLOAD}$  signal will override the SCLK signal.

### $\overline{PLOAD}$

Serial data port shift register load: When  $\overline{PLOAD}$  is low (i.e. level triggered not edge triggered), the current parallel data will be loaded into the shift register.  $\overline{PLOAD}$  overrides SCLK. When  $\overline{PLOAD}$  is high, the data can be shifted out through the SDO pin with SCLK.

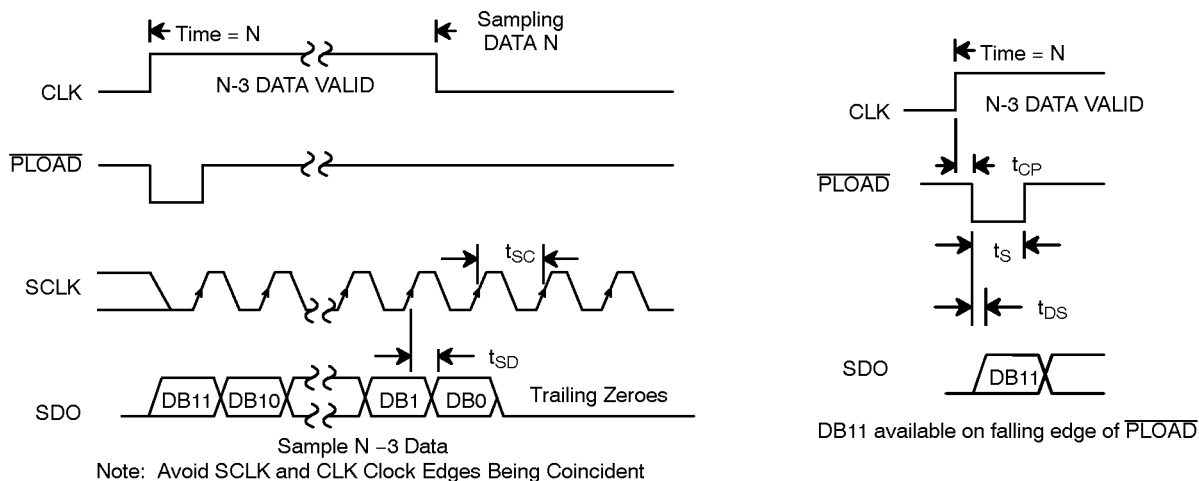


Figure 4. Serial Port Timing Chart  
PHASE = 1

**APERTURE: Aperture Delay Sync (output)**

This signal is high when the internal sample/hold function is sampling  $V_{IN}$ , and goes low when it is in the hold mode (when the

ADC is comparing the stored input value to the reference ladder). The value of  $V_{IN}$  at the high to low transition of APERTURE is the value that will be digitized. A system can monitor this signal and adjust the CLK to accurately synchronize the sampling point to an external event.

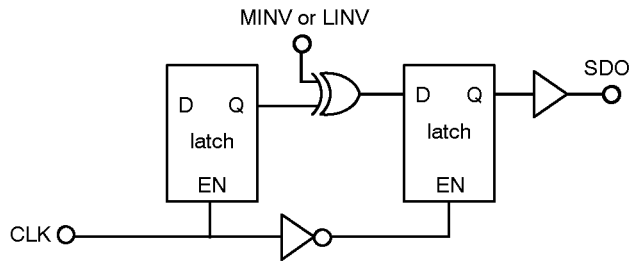
MINV LINV	0 0	0 1	1 0	1 1
$V_{RT}$	111 ... 11 111 ... 10	100 ... 00 100 ... 01	011 ... 11 011 ... 10	000 ... 00 000 ... 01
$V_{IN}$ mid scale	100 ... 01 100 ... 00	111 ... 10 111 ... 11	000 ... 01 000 ... 00	011 ... 10 011 ... 11
$V_{RB}$	011 ... 11 000 ... 01 000 ... 00	000 ... 00 011 ... 10 011 ... 11	111 ... 11 100 ... 01 100 ... 00	100 ... 00 111 ... 10 111 ... 11
	binary	inverted 2's complement	2's complement	inverted binary

Table 1. Output Data Format Truth Table

**MINV & LINV: Digital Output Format (inputs)**

These signals control the format of the digital output data bits DB0 – DB11. Normally both pins are held low so the data is in straight binary format (all 0's when  $V_{IN}=V_{RB}$ ; all 1's when  $V_{IN}=V_{RT}$ ). If MINV is pulled high then the MSB (DB11) will be inverted. If LINV is pulled high then the LSBs (DB0 – DB10) will be inverted. The OFW and UFW bits are not affected by these signals.

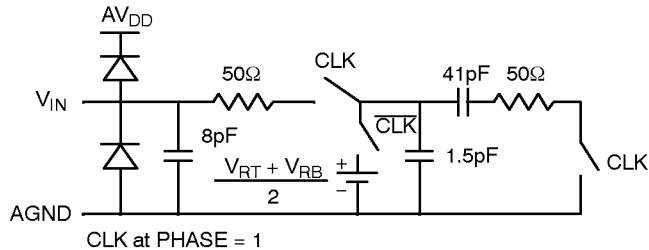
MINV & LINV are meant to be static digital signals. If they are to change during operation they should only change when the CLK is low (assuming PHASE is high; if PHASE is low then these signals should only change when CLK is high). Changing MINV and/or LINV on the wrong phase of the CLK will not hurt anything, but the effects on the digital outputs will not be seen until the output latch of the output register is enabled. MINV and LINV have internal pull down devices. Please see the simplified logic circuit (Figure 5.)



**Figure 5. MINV, LINV Simplified Logic Circuit**

## V<sub>IN</sub> Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V<sub>IN</sub> is sampled at the high to low clock transition. The diagram (Figure 6.) shows an equivalent input circuit.



**Figure 6. Equivalent Input Circuit**

## Reference Ladder Taps

These taps connect to every sixteenth point along the reference ladder; R4 is 4/16th up from V<sub>RB</sub>, R7 is 7/16ths up from V<sub>RB</sub>. Normally R4, R8 and R12 should have 0.1 microfarad capacitors to GND; this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. The internal interconnect resistance from the pin to the ladder is less than 3Ω for the even numbered taps, (i.e. R4,R6, etc.) and is approximately 10Ω for the odd numbered taps.

Alternating the transfer curve may be desirable to make the probability of codes for a certain range of V<sub>IN</sub> be enhanced or minimized.

Sometimes this is referred to as probability density function shaping, or histogram shaping.

For Log shapes, the MP8790 is ideal since it provides 16 segments.

0.8 V maximum per tap is recommended for applications above 85°C.

## APPLICATION NOTES

V<sub>IN</sub> signals should not exceed AV<sub>DD</sub> +0.5V or go below AGND -0.5V. All pins have internal protection diodes that will protect them from short transients (<100μs) outside the supply range.

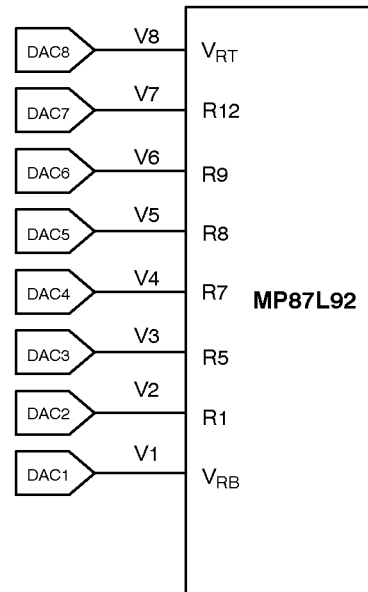
AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (V<sub>DD</sub>) and reference voltage (V<sub>RT</sub> & V<sub>RB</sub>) pins should be decoupled with 0.1 μF and 10 μF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

At least three of the reference tap pins (R4, R8, R12) should be decoupled with 0.1 μF to 1 μF capacitors. This will help stabilize the internal reference voltages thus reducing any INL errors.

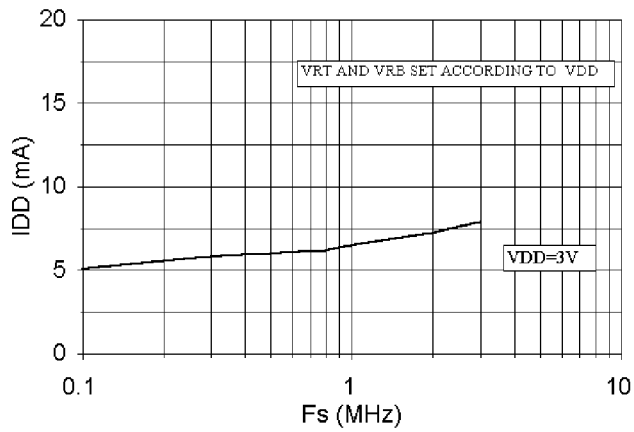
The reference tap pins (R1-R16) can be used to create piecewise linear transfer functions. By forcing custom voltages on these pins, a 16-segment transfer function can be made. See Figure 7.



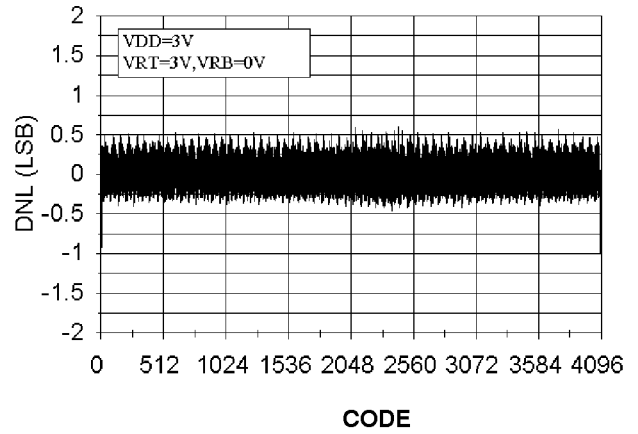
*Only the Ladder detail shown.*

**Figure 7. A/D with Programmed Ladder Control for Creating a Piecewise Linear Transfer Function**

**PERFORMANCE CHARACTERISTICS**



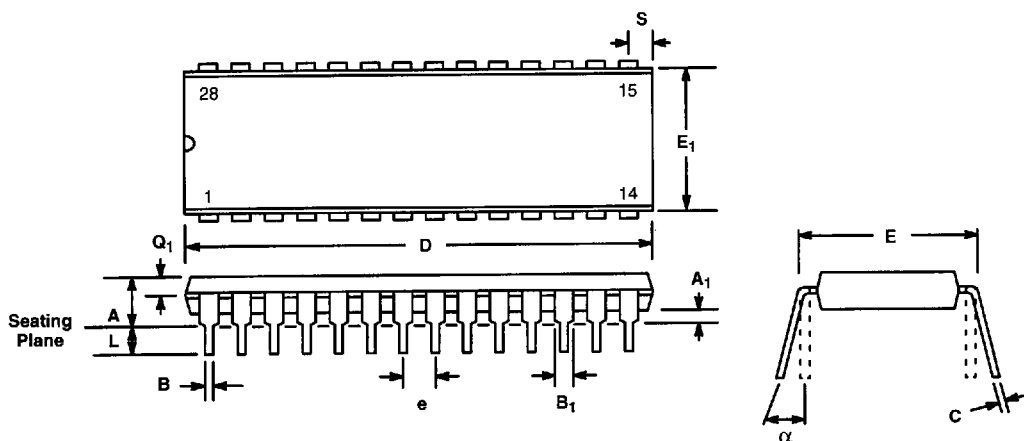
**Graph 1.  $I_{DD}$  vs.  $F_s$**



**Graph 2. DNL Error Plot**

# Package Dimensions

## 28 LEAD PLASTIC DUAL-IN-LINE (600 MIL PDIP) N28

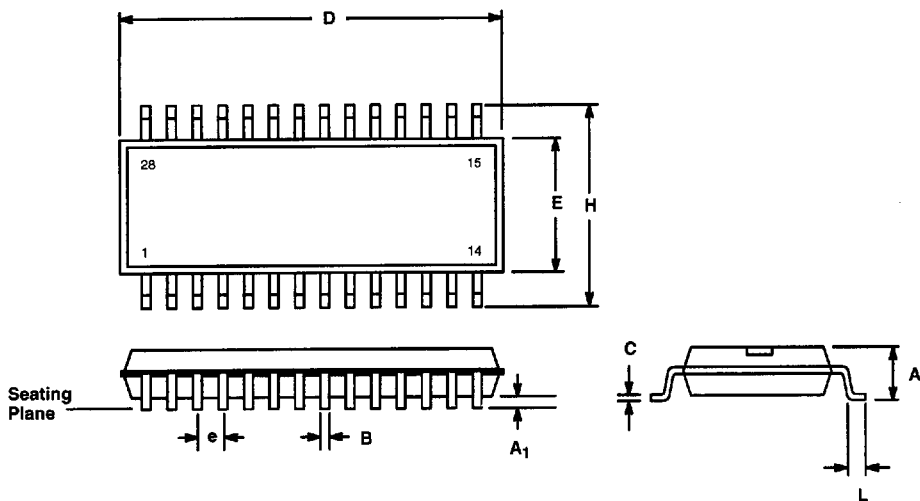


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.232	—	5.893
A <sub>1</sub>	0.015	—	0.381	—
B	0.014	0.023	0.356	0.584
B <sub>1</sub> (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	1.380	1.490	35.05	37.85
E	0.585	0.625	14.86	15.88
E <sub>1</sub>	0.500	0.610	12.70	15.49
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q <sub>1</sub>	0.055	0.070	1.40	1.78
S	0.020	0.100	1.508	2.54

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

# Package Dimensions

## 28 LEAD SMALL OUTLINE (335 MIL EIAJ SOIC) R28



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.60	2.80	0.102	0.110
A <sub>1</sub>	0.2 (typ.)		0.008 (typ.)	
B	0.3	0.5	0.012	0.020
C	0.10	0.20	0.004	0.008
D	17.6	18.0	0.693	0.709
E	8.3	8.5	0.327	0.335
e	1.27 (typ.)		0.050 (typ.)	
H	11.5	12.1	0.453	0.477
L	0.8	1.2	0.031	0.047