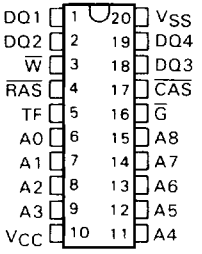
FEBRUARY 1988

- 262,144 × 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

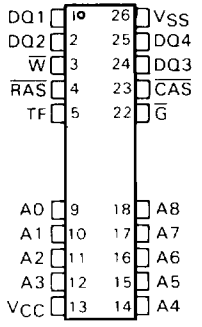
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44C256-12	120 ns	35 ns	60 ns	230 ns
SMJ44C256-15	150 ns	45 ns	75 ns	270 ns

- SMJ44C256 — Enhanced Page Mode Operation
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)
- 3-State Unlatched Output
- Low Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs and Clocks Are TTL Compatible
- High-Reliability Ceramic 20-Pin 300-Mil-Wide DIP or 20/26-Lead Ceramic Surface Mount (CSOJ) Package
- −55°C to 125°C Operating Temperature Range
- Standard and Class B Processing
  - −SM44C256 . . . Standard
  - −SMJ44C256 . . . Class B

JD PACKAGE
(TOP VIEW)



HJ PACKAGE†
(TOP VIEW)



† The packages shown here are for pinout reference only. The HJ package is actually 75% of the length of the JD package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44C256 is a high-speed, 1,048,576-bit dynamic random-access memory organized as 262,144 words of four bits each. It employs state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold, and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

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