

---

# HD49235FS

Digital Signal Processor for CD

# HITACHI

ADE-207-162A(Z)

2nd. Edition  
August 1995

---

## Description

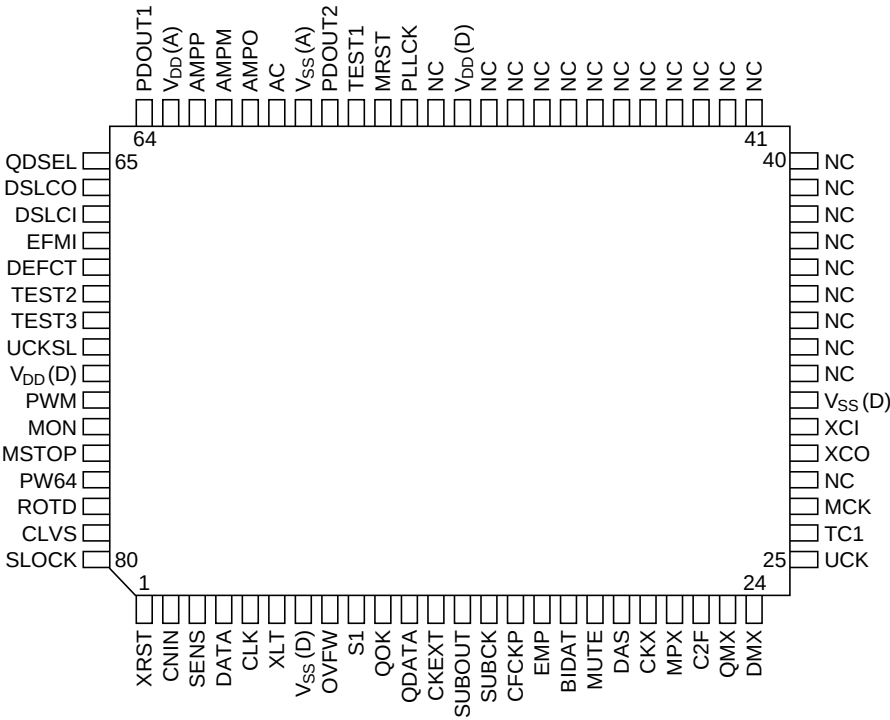
The HD49235FS is a digital signal processor for compact disc (CD) applications.

## Features

- Powerful error correction capability: two-symbol C1 correction and four-symbol C2 correction
- Quadruple-speed reproduction supported (maintaining two-symbol C1 and four-symbol C2 error correction)
- On-chip analog PLL and digital PLL (VCO and phase detector)
- Automatic adjustment of the free-running frequency of the VCO
- Built-in microprocessor interface
- On-chip 80-bit shift registers for Q-code buffering
- Cyclic redundancy check on Q-code values
- Audio output functions: monaural output, single-channel mute, left-right reverse, soft mute, -12-dB attenuation
- 16-kbit RAM on-chip

# HD49235FS

## Pin Arrangement



(Top view)

## Pin Description

| Pin |                     |                           |      |                    |                                                                                        | Polarity |          |
|-----|---------------------|---------------------------|------|--------------------|----------------------------------------------------------------------------------------|----------|----------|
| No. | Symbol              | Name                      | I/O* | Connection         | Function                                                                               | H        | L        |
| 1   | XRST                | X ( $\mu$ -com) reset     | I    | Microprocessor     | Microprocessor interface register reset                                                |          | Reset    |
| 2   | CNIN                | Counter clock input       | I    | Servo IC           | Pulse input for track counter                                                          |          |          |
| 3   | SENS                | Sensor                    | TO   | Microprocessor     | Servo status output                                                                    |          |          |
| 4   | DATA                | Data                      | I    | Microprocessor     | Data input for microprocessor interface                                                |          |          |
| 5   | CLK                 | Clock                     | I    | Microprocessor     | Clock input for microprocessor interface                                               |          |          |
| 6   | XLT                 | X ( $\mu$ -com) latch     | I    | Microprocessor     | Strobe input for microprocessor interface                                              |          |          |
| 7   | V <sub>ss</sub> (D) | V <sub>ss</sub> (digital) | —    |                    | Digital ground                                                                         |          |          |
| 8   | OVFW                | RAM- overflow             | O    |                    | On-chip RAM overflow signal output                                                     |          | Overflow |
| 9   | S1                  | Subcode sync 1            | O    | Microprocessor     | Subcode sync signal (with protection)                                                  |          |          |
| 10  | QOK                 | Q-code OK                 | O    | Microprocessor     | Subcode CRC result output                                                              | OK       | NG       |
| 11  | QDATA               | Q-code data               | O    | Microprocessor     | Subcode Q data output                                                                  |          |          |
| 12  | CKEXT               | Clock-EXT                 | I    | Microprocessor     | Clock input for Q data readout                                                         |          |          |
| 13  | SUBOUT              | Subcode out               | O    | CD graphics        | Subcode data output for CD graphics                                                    |          |          |
| 14  | SUBCK               | Subcode clock             | I    | CD graphics        | Clock input for SUBOUT subcode readout                                                 |          |          |
| 15  | CFCKP               | C&D frame clock out       | O    | CD graphics        | Subcode frame synchronization signal (7.35 kHz at normal speed, synchronized with PLL) |          |          |
| 16  | EMP                 | Emphasis output           | O    |                    | Emphasis on/off status output                                                          | ON       | OFF      |
| 17  | BIDAT               | Biphase date              | TO   |                    | Digital audio interface output                                                         |          |          |
| 18  | MUTE                | Mute                      | I    | Microprocessor     | Audio mute input                                                                       | Mute     |          |
| 19  | DAS                 | Data serial out           | O    | DAC or ROM decoder | Serial data output for audio or ROM                                                    |          |          |
| 20  | CKX                 | Clock X                   | O    | DAC or ROM decoder | Strobe clock output for DAS signal                                                     |          |          |

# HD49235FS

## Pin Description (cont)

| Pin |                     |                           |      |                    |                                                                                              | Polarity |       |
|-----|---------------------|---------------------------|------|--------------------|----------------------------------------------------------------------------------------------|----------|-------|
| No. | Symbol              | Name                      | I/O* | Connection         | Function                                                                                     | H        | L     |
| 21  | MPX                 | Multiplex                 | O    | DAC or ROM decoder | Left/right channel switching signal output (44.1 kHz at normal speed, synchronized with DAS) |          |       |
| 22  | C2F                 | C2 flag                   | O    | ROM decoder        | C2 error flag output                                                                         | Error    |       |
| 23  | QMX                 | Quad multiplex            | O    |                    | 4 × MPX clock signal (176.4 kHz at normal speed, synchronized with DAS)                      |          |       |
| 24  | DMX                 | Double multiplex          | O    |                    | 2 × MPX clock signal (88.2 kHz at normal speed, synchronized with DAS)                       |          |       |
| 25  | UCK                 | μ-com clock               | O    | Microprocessor     | Clock output for microprocessor (8.5 MHz or 17 MHz)                                          |          |       |
| 26  | TC1                 | Test C1 flag              | O    |                    | C1 error flag monitor pin                                                                    |          | Error |
| 27  | MCK                 | Master clock              | O    |                    | Master clock output (33.8688 MHz)                                                            |          |       |
| 28  | NC                  | No connection             | —    | Open or VDD        | Not connected                                                                                |          |       |
| 29  | XCO                 | X'tal clock output        | XO   | Crystal oscillator | Crystal oscillator output                                                                    |          |       |
| 30  | XCI                 | X'tal clock input         | XI   | Crystal oscillator | Crystal oscillator input                                                                     |          |       |
| 31  | V <sub>SS</sub> (D) | V <sub>SS</sub> (digital) | —    |                    | Digital ground                                                                               |          |       |
| 32  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 33  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 34  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 35  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 36  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 37  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 38  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 39  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 40  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 41  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 42  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 43  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |
| 44  | NC                  | No connection             | —    | Open               | Not connected                                                                                |          |       |

## Pin Description (cont)

| Pin |                     |                           |      |                         |                                            | Polarity      |               |
|-----|---------------------|---------------------------|------|-------------------------|--------------------------------------------|---------------|---------------|
|     |                     |                           |      |                         |                                            | H             | L             |
| No. | Symbol              | Name                      | I/O* | Connection              | Function                                   |               |               |
| 45  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 46  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 47  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 48  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 49  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 50  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 51  | NC                  | No connection             | —    | Open                    | Not connected                              |               |               |
| 52  | V <sub>DD</sub> (D) | V <sub>DD</sub> (digital) | —    |                         | Digital power supply                       |               |               |
| 53  | NC                  | No connection             | —    | Open or V <sub>DD</sub> | Not connected                              |               |               |
| 54  | PLLCK               | PLL clock                 | O    |                         | PLL clock output monitor                   |               |               |
| 55  | MRST                | Master reset              | IU   | Open or V <sub>DD</sub> | Master reset of chip                       |               | Reset         |
| 56  | TEST1               | TEST 1                    | IU   | Open or V <sub>DD</sub> | Test pin                                   |               |               |
| 57  | PDOUT2              | Phase detect out 2        | TO   | External RC circuit     | PLL auto-adjust phase detector output      |               |               |
| 58  | V <sub>SS</sub> (A) | V <sub>SS</sub> (analog)  | —    |                         | Analog ground                              |               |               |
| 59  | AC                  | Amp compensation          | A    | External RC circuit     | Amplifier phase compensation pin           |               |               |
| 60  | AMPO                | Amp output                | AO   | External RC circuit     | PLL amplifier output                       |               |               |
| 61  | AMPM                | Amp minus input           | AI   | External RC circuit     | PLL amplifier inverting input              |               |               |
| 62  | AMPP                | Amp plus input            | AI   | External RC circuit     | PLL amplifier non-inverting input          |               |               |
| 63  | V <sub>DD</sub> (A) | V <sub>DD</sub> (analog)  | —    |                         | Analog power supply                        |               |               |
| 64  | PDOUT1              | Phase detect out 1        | TO   | External RC circuit     | PLL EFM phase detector output              |               |               |
| 65  | QDSEL               | Q-data clock select       | IU   |                         | Q data readout mode switching signal input | Internal sync | External sync |
| 66  | DSLCO               | DSL control output        | O    | External RC circuit     | EFM comparator slice level control output  |               |               |
| 67  | DSLCI               | DSL control input         | AI   | External RC circuit     | EFM comparator slice level control input   |               |               |
| 68  | EFMI                | EFM signal input          | AI   |                         | EFM signal input                           |               |               |
| 69  | DEFCT               | Defect                    | I    | Servo IC                | Defect detection signal input              | Defect        |               |
| 70  | TEST2               | TEST 2                    | IU   | Open or V <sub>DD</sub> | Test pin                                   |               |               |

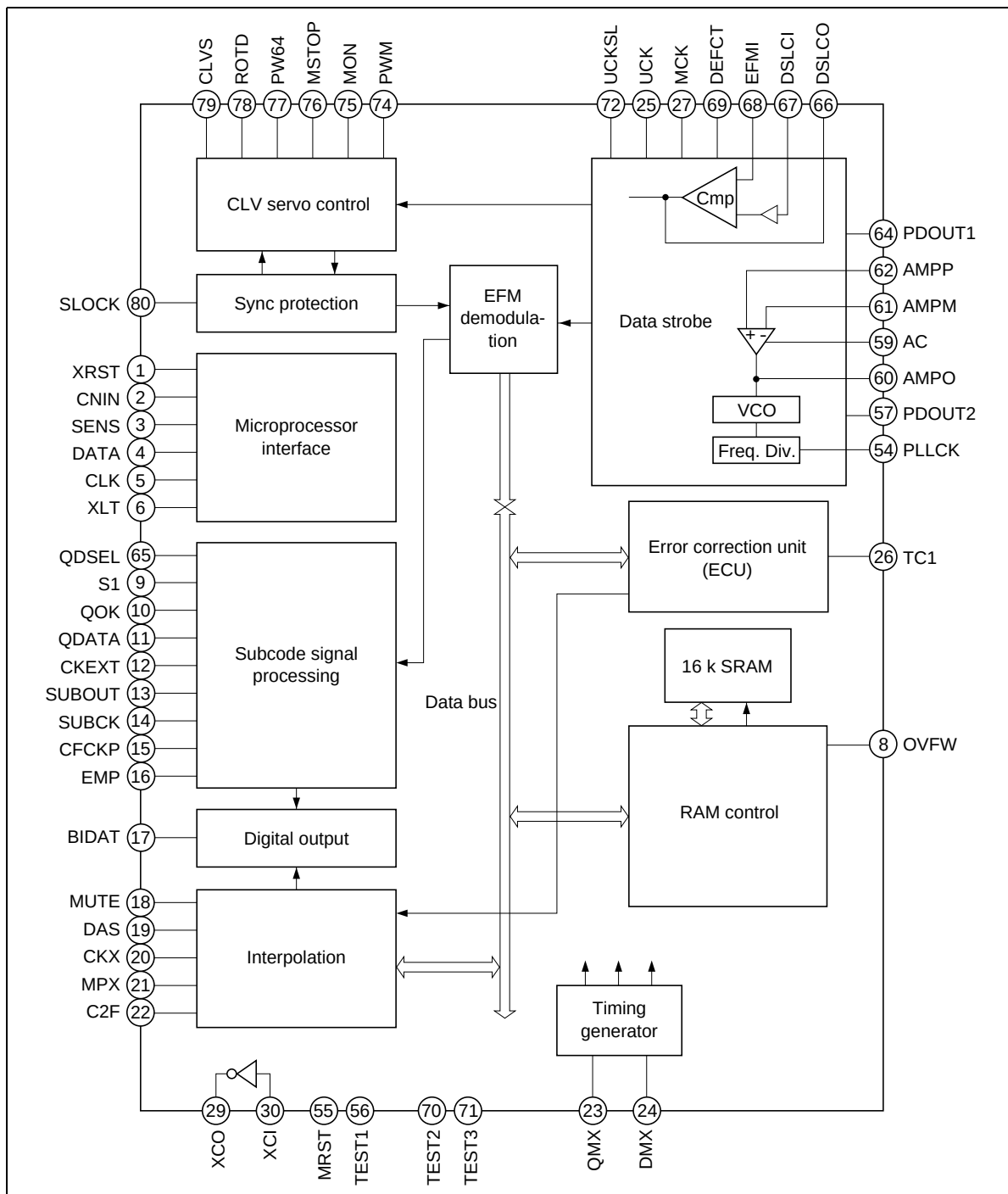
# HD49235FS

## Pin Description (cont)

| Pin |                     |                               |      |                         |                                                              | Polarity    |            |
|-----|---------------------|-------------------------------|------|-------------------------|--------------------------------------------------------------|-------------|------------|
|     |                     |                               |      |                         |                                                              | H           | L          |
| No. | Symbol              | Name                          | I/O* | Connection              | Function                                                     |             |            |
| 71  | TEST3               | TEST 3                        | IU   | Open or V <sub>DD</sub> | Test pin                                                     |             |            |
| 72  | UCKSL               | Microcomputer clock selection | IU   |                         | Microprocessor clock switching signal input                  | 16.9344 MHz | 8.4672 MHz |
| 73  | V <sub>DD</sub> (D) | V <sub>DD</sub> (digital)     | —    |                         | Digital power supply                                         |             |            |
| 74  | PWM                 | Pulse width modulate          | TO   |                         | Constant linear velocity (CLV) control signal for disc motor |             |            |
| 75  | MON                 | Motor on                      | O    |                         | Disc-motor-on status detection output                        | On          |            |
| 76  | MSTOP               | Motor stop                    | TO   |                         | CLV phase control signal                                     |             |            |
| 77  | PW64                | Pulse width 64T               | O    | Microprocessor          | Brake release signal                                         |             |            |
| 78  | ROTD                | Rotate direction              | O    | Microprocessor          | MSB of PWM pin output, for monitoring                        |             |            |
| 79  | CLVS                | CLV status                    | O    | Microprocessor          | Output indicating normal or starting mode of CLV control     | Normal      | Starting   |
| 80  | SLOCK               | Sync lock                     | O    | Microprocessor          | Disc motor rotation lock signal                              | Lock        |            |

Note: \* I—input; O—output; IO—input/output; IU—pulled-up input; TO—three-state output; A—analog pin; AI—analog input; AO—analog output; XI—oscillator input; XO—oscillator output

# Block Diagram



# HD49235FS

## Microprocessor Commands

| Register<br>(Address) | Command               | Data  |       |       |        |         |        |         |         | SENS<br>Pin<br>Output |
|-----------------------|-----------------------|-------|-------|-------|--------|---------|--------|---------|---------|-----------------------|
|                       |                       | D7    | D6    | D5    | D4     | D3      | D2     | D1      | D0      |                       |
| 8 (1000)              | Mode selections       | ROM   | ROMEf | DOOFF | SUBCO  | SLTSW   | 0      | DCOND   | DWIDTH  | Z                     |
| 9 (1001)              | Function selections   | 1     | BI1   | BI0   | WG10TL | SYLCK1  | SYLCK0 | CRCQ    | *       | Z                     |
| A (1010)              | Audio control         | MUTEL | MUTER | MONO  | ATT    | BLGMAIN | BLGSUB | SOFTMT  | SWLR    | Z                     |
| B (1011)              | Track counter setting | TC7   | TC6   | TC5   | TC4    | TC3     | TC2    | TC1     | TC0     | Complete              |
| C (1100)              | CLV control           | AINTV | ATH   | GAIN1 | GAIN0  | SGAIN1  | SGAIN0 | PDGAIN1 | PDGAIN0 | Count                 |
| D (1101)              | CLV kick control      | KICK7 | KICK6 | KICK5 | KICK4  | KICK3   | KICK2  | KICK1   | *       | Z                     |
| E (1110)              | CLV mode              | ED3   | ED2   | ED1   | ED0    | 0       | *      | *       | *       | BRAKE                 |
| F (1111)              | ECU mode              | 0     | 0     | AS0   | *      | *       | *      | *       | *       | Z                     |

Asterisks indicate don't-care bits

### Register 8

| 0      |    | 1                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                       |
|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ROM    | D7 | Audio (with interpolation)                                                                                                                                                                                                                                                                                             | CD-ROM (no interpolation)                                                                                                                                                                                                                                                             |
| ROMEf  | D6 | C2 flag output order: lower first                                                                                                                                                                                                                                                                                      | C2 flag output order: upper first                                                                                                                                                                                                                                                     |
| DOOFF  | D5 | Digital output on                                                                                                                                                                                                                                                                                                      | Digital output off                                                                                                                                                                                                                                                                    |
| SUBCO  | D4 | Subcode data not inserted in DAS signal                                                                                                                                                                                                                                                                                | Subcode data inserted in DAS signal                                                                                                                                                                                                                                                   |
| SLTSW  | D3 | 48-fs clock                                                                                                                                                                                                                                                                                                            | 64-fs clock                                                                                                                                                                                                                                                                           |
|        | D2 | Normal operation                                                                                                                                                                                                                                                                                                       | Illegal setting                                                                                                                                                                                                                                                                       |
| DCOND  | D1 | Condition for switching between digital and analog PLLs: digital PLL when defect detection signal width is 4 frames or more                                                                                                                                                                                            | Condition for switching between digital and analog PLLs: digital PLL when defect detection signal width is 8 frames or more                                                                                                                                                           |
| DWIDTH | D0 | Digital PLL termination timing: <ul style="list-style-type: none"><li>8 frames after fall of defect detection signal if width of defect detection signal width is less than 12 frames</li><li>16 frames after fall of defect detection signal if width of defect detection signal width is 12 frames or more</li></ul> | <ul style="list-style-type: none"><li>4 frames after fall of defect detection signal if width of defect detection signal width is less than 12 frames</li><li>8 frames after fall of defect detection signal if width of defect detection signal width is 12 frames or more</li></ul> |



**Register 9**

|        | 0  | 1                                                                                    |
|--------|----|--------------------------------------------------------------------------------------|
|        | D7 | Illegal setting                                                                      |
|        |    | Normal operation                                                                     |
| BI1    | D6 | 00: Normal play      01: Double-speed play                                           |
| BI0    | D5 | 10: Quadruple-speed play    11: Quadruple-speed play                                 |
| WG10TL | D4 | Sync detection window width: $\pm 10$ T      Sync detection window width: $\pm 19$ T |
| SYLCK1 | D3 | Length of time sync lock state is maintained when sync signal is missing             |
| SYLCK0 | D2 | 00: 2 frames      01: 4 frames<br>10: 8 frames      11: 12 frames                    |
| CRCQ   | D1 | QOK flag is not inserted in QDATA output    QOK flag is inserted in QDATA output     |

**Register A**

|         | 0  | 1                                                          |
|---------|----|------------------------------------------------------------|
| MUTEL   | D7 | Left-channel mute off                                      |
|         |    | Left-channel mute on                                       |
| MUTER   | D6 | Right-channel mute off                                     |
|         |    | Right-channel mute on                                      |
| MONO    | D5 | Stereo                                                     |
|         |    | Monaural                                                   |
| ATT     | D4 | Attenuation off                                            |
|         |    | Attenuation ( $-12$ dB) on                                 |
| BLGMAIN | D3 | 00: Stereo      01: Bilingual, right channel               |
| BLGSUB  | D2 | 10: Bilingual, left channel    11: Bilingual, left channel |
| SOFTMT  | D1 | Soft mute off                                              |
|         |    | Soft mute on                                               |
| SWLR    | D0 | Normal                                                     |
|         |    | Left-right reverse                                         |

- Notes: 1. Priority for mute and attenation as follows.  
 "Mute" port > SOFTMT > MUTE L, MUTE R > ATT
2. In the case of setting "ROM" = 1 (CD-ROM mode), the data of register "A" is ignored and is considered all zero.  
 It is recovered as it were, after setting "ROM" = 0.
3. "BLGMAIN" and "BLG SUB" commands are ignored if "SWLR" = 1, and set stereo.

**Register B**

|                       | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| Track counter setting | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 |
|                       | 128 | 64  | 32  | 16  | 8   | 4   | 2   | 1   |

# HD49235FS

## Register C

|         |    | 0                                                               | 1                                                    |
|---------|----|-----------------------------------------------------------------|------------------------------------------------------|
| AINTV   | D7 | Sync detection count is tested at 32-frame intervals            | Sync detection count is tested at 64-frame intervals |
| ATH     | D6 | Sync must be detected 4 times or more                           | Sync must be detected 8 times or more                |
| GAIN1   | D5 | Speed error (PWM pin output) gain in CLV steady state operation |                                                      |
| GAIN0   | D4 | 00: -6 dB      01: 0 dB<br>10: +6 dB      11: 0 dB              |                                                      |
| SGAIN1  | D3 | Speed error gain and access                                     |                                                      |
| SGAIN0  | D2 | 00: -6 dB      01: 0 dB<br>10: +6 dB      11: 0 dB              |                                                      |
| PDGAIN1 | D1 | CLV phase error (MSTOP pin output) gain                         |                                                      |
| PDGAIN0 | D0 | 00: -6 dB      01: 0 dB<br>10: +6 dB      11: 0 dB              |                                                      |

## Register D

|                  | D7     | D6     | D5     | D4    | D3    | D2    | D1    | D0 |
|------------------|--------|--------|--------|-------|-------|-------|-------|----|
| CLV kick control | KICK7  | KICK6  | KICK5  | KICK4 | KICK3 | KICK2 | KICK1 | *  |
| (PWM duty cycle) | 64/128 | 32/128 | 16/128 | 8/128 | 4/128 | 2/128 | 1/128 | *  |

Asterisks indicate don't-care bits

**CLV Mode** (Register E)

| <b>ED3 to ED0/HEX</b> |   | <b>Mode</b> | <b>Status</b>                |
|-----------------------|---|-------------|------------------------------|
| 0000                  | 0 | STOP        | Motor stop                   |
| 0110                  | 6 | PLAY        | Starting mode                |
|                       |   |             | Normal mode                  |
| 1000                  | 8 | ROT         | Disc motor driven forward    |
| 1001                  | 9 | KICK        | Kick control                 |
| 1010                  | A | BRAKE       | Disc motor driven in reverse |
| 1100                  | C | ACS         | Access mode                  |
| 1110                  | E | START       | Forced starting mode         |
| 1111                  | F | NORM        | Forced normal mode           |

**ECU Mode** (Register F)

| <b>AS0</b> | <b>Mode</b> | <b>Status</b>                                           |
|------------|-------------|---------------------------------------------------------|
| 0          | FULL        | Error correction: C1—two symbols; C2—four symbols       |
| 1          | E4IHD       | C2—four symbol error correction inhibited on track jump |

## Functional Description

### Data Strobe

The main functions of this block are described below.

#### 1. Generation of Basic Crystal Clock

**XCI:** Is the inverter input pin for the crystal oscillator.

**XCO:** Is the inverter output pin for the crystal oscillator.

A 33.8688-MHz crystal oscillator clock signal is generated at the XCI and XCO pins. Figure 1 shows the standard external components when a 33.8688-MHz crystal is used.

#### 2. Generation of Basic PLL Clock

**PLLCK:** This is an output pin used for monitoring the VCO oscillator signal. When the PLL is in lock, the frequency is 4.3218 MHz at standard speed, 8.6436 MHz at double speed, or 17.2872 MHz at quadruple speed.

**PDOUT1:** This is a phase detector output pin, for use in data strobing. This pin is in the high-impedance state in the CLV stop mode. In other CLV modes, this pin outputs the result of phase detection in a phase-locked loop formed with the VCO and the EFM signal input at the EFMI pin.

**PDOUT2:** This is a phase detector output pin, for use in adjusting the free-running frequency of the VCO. In CLV stop mode, this pin outputs a pulse-width modulated waveform equivalent to the phase error in a phase-locked loop formed with the VCO and a crystal-oscillator-derived clock signal. In other CLV modes, this pin maintains a pulse-width modulated output with the same duty cycle as in stop mode.

**AC:** Connect a capacitor for phase compensation of the amplifier.

**AMPO:** Amplifier output pin.

**AMPM:** Inverting input to the amplifier.

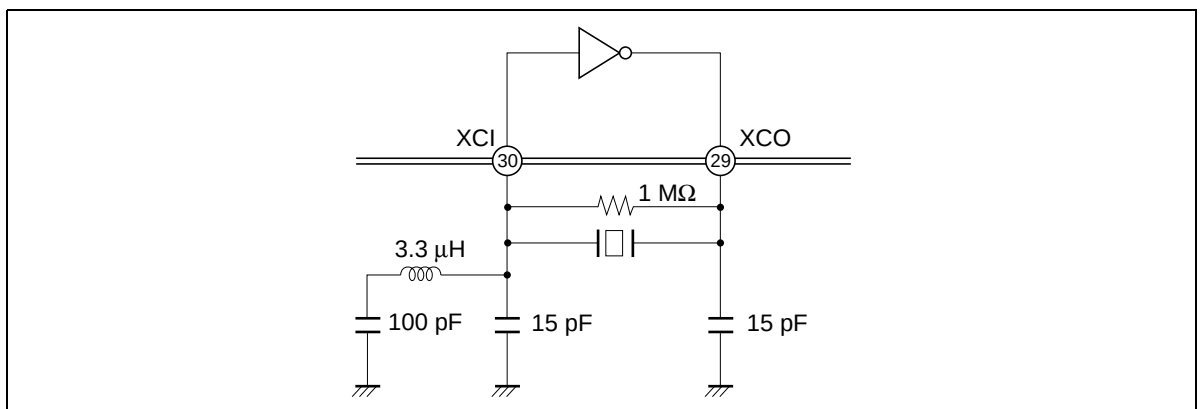


Figure 1 33.8688-MHz Crystal Oscillator Circuit

**AMPP:** Non-inverting input to the amplifier.

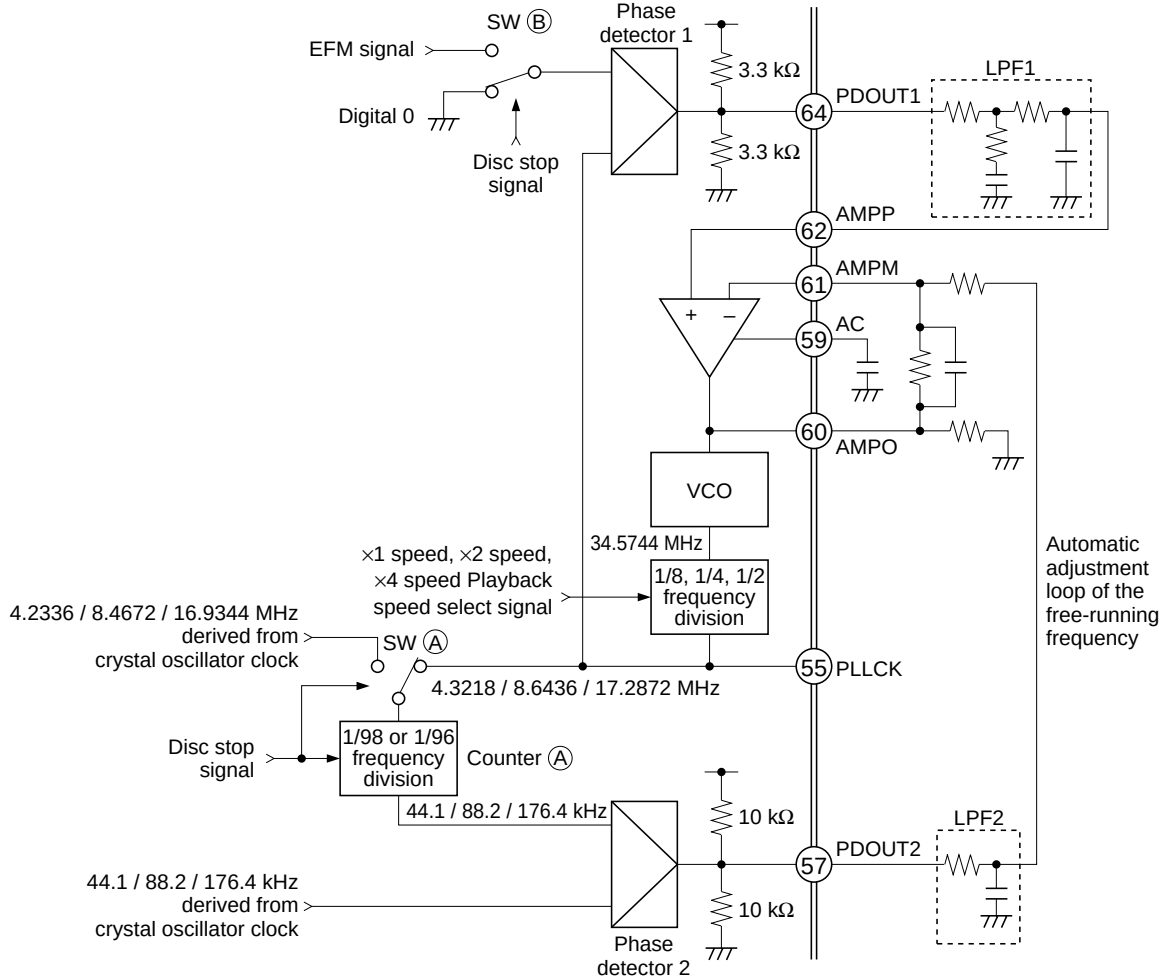
This chip uses a PLL for recovery of the bit clock. A built-in circuit automatically adjusts the free-running frequency of the PLL, so fewer adjustments are required on the production line. The chip can be forced to adjust its own free-running frequency whenever power is turned on or the speed is changed by switching to CLV stop mode. Thus the free-running frequency is always set to the center of the lock frequency range even if changes occur in the VCO and external circuit constants due to aging.

The principle and usage of automatic adjustment of the free-running frequency will be described below.

- a. In automatic adjustment of the VCO free-running frequency, this chip uses the disc stop signal. The disc stop signal is turned on when the microprocessor writes 0000 in bits ED3, ED2, ED1, and ED0 of register E in the chip's microprocessor interface. (See section 6, Microprocessor Interface.)
- b. When the disc stop signal is turned on, counter (A) in figure 2 becomes a divide-by-98 counter, switch (A) is connected to the output from the VCO, and switch (B) is connected to digital 0.

At this time, the circuit for the PDOUT1 output is stopped, so the output of the LPF1 connected to PDOUT1 goes to the fixed DC bias level, which is  $1/2 V_{DD}$ .

The loop formed by PDOUT2 → LPF2 → amplifier → VCO → counter (A) now operates to lock the VCO oscillator frequency to 34.5744 MHz, which is 8 times the standard CD bit rate (4.3218 MHz).



Note: When changing the playback speed, always switch the system to CLV stop mode so that the free-running frequency is adjusted automatically. The period of setting is 30 msec or more. Within five second after turning on power, switch the sytem to CLV stop mode two times or more in an interval from one to two second so that the free-running frequency is adjusted automatically. The period of setting is 30 msec or more.

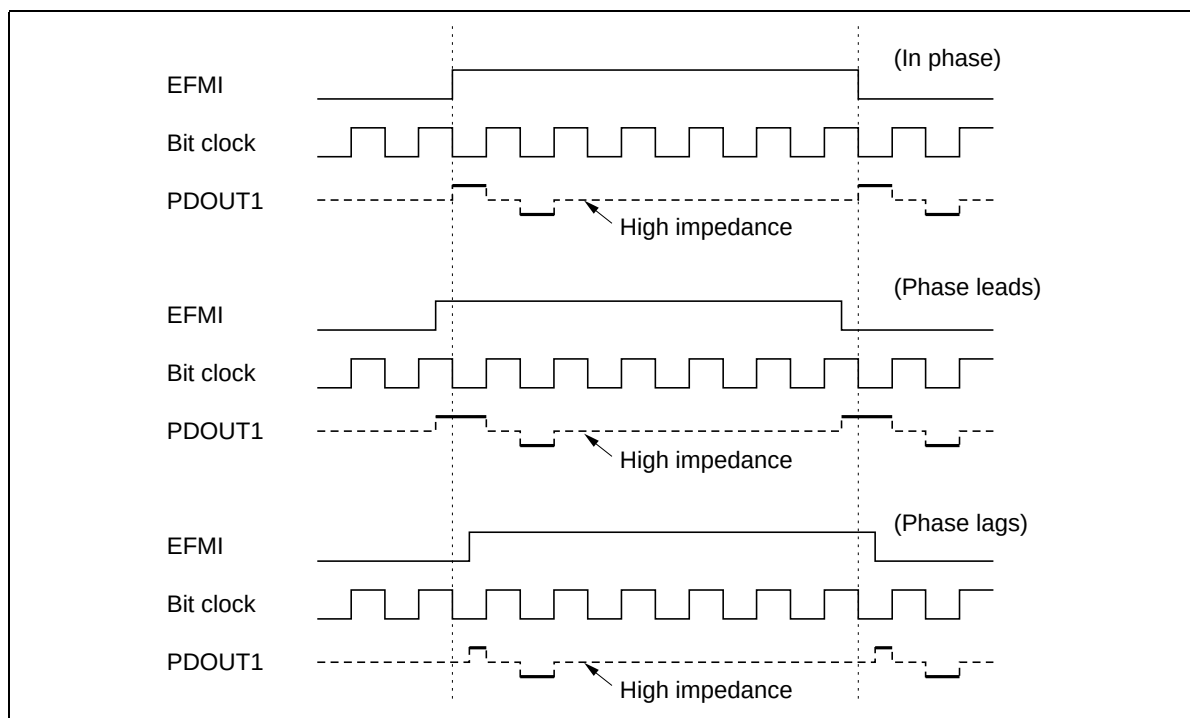
Figure 2

- c. Next, reproduction from the disc will begin. When the microprocessor sends command data to start disc rotation, the disc stop signal is turned off.

Switch (A) is now connected to receive a 4.2336 MHz clock from the crystal oscillator and counter (A) is changed to be a divide-by-96 counter. The counter (A) output is held at 44.1 kHz by switching the divisor. Here, switching is performed on the counter (A) output edge. The phase error existing between the VCO and the crystal oscillator clock (the phase error that was detected at adjustment step 2) is maintained.

- d. When the disc is rotating and reproduction starts, switch (B) is connected to receive the EFM signal. The phase detector PDOUT1 in figure 2 compares the phases of the EFM signal, which was converted to binary by the EFM comparator, and the bit clock and outputs phase comparison information from the PDOUT1 pin.

As shown in figure 3, when the EFM signal is in phase with the clock produced by the VCO, the PDOUT1 output is high and low for equal lengths of time. When the EFM signal leads the on-chip VCO clock, the high length is longer than the low length. When the EFM signal lags the on-chip VCO clock, the high length is shorter.



**Figure 3 Timing of PDOUT1 Output Signal**

## 3. Data Slice Level Output

**EFMI:** This pin inputs the EFM RF signal.

**DSLCO:** This pin outputs an error signal for correcting deviation in the data slice level of the EFM signal. This signal is used as a control signal to keep the data slice level of the EFM signal centered, by forming a negative-feedback loop with the EFM comparator.

**DSLCI:** This pin inputs the above error signal through a low-pass filter to the EFM comparator.

Figure 4 shows the EFM comparator circuit. The EFM RF signal is input through a capacitive coupling, and binarized by comparison with a slice level generated by the DSLC amplifier.

— When not in stop mode

— The DSLCO pin outputs the inverse of the binarized EFM signal. Even if the EFM signal is asymmetrical before slicing, an appropriate slice level is obtained by feeding the dc component of the sliced EFM signal back through an external low-pass RC filter.

— In stop mode

— The DSLCO pin outputs a square wave with a 50% duty cycle and the same period as the output at the MPX pin, and the slice level is kept at  $1/2 V_{DD}$ . This permits rapid optimization of the slice level when the device leaves stop mode, and prevents oscillation by cutting off the loop through the low-pass filter.

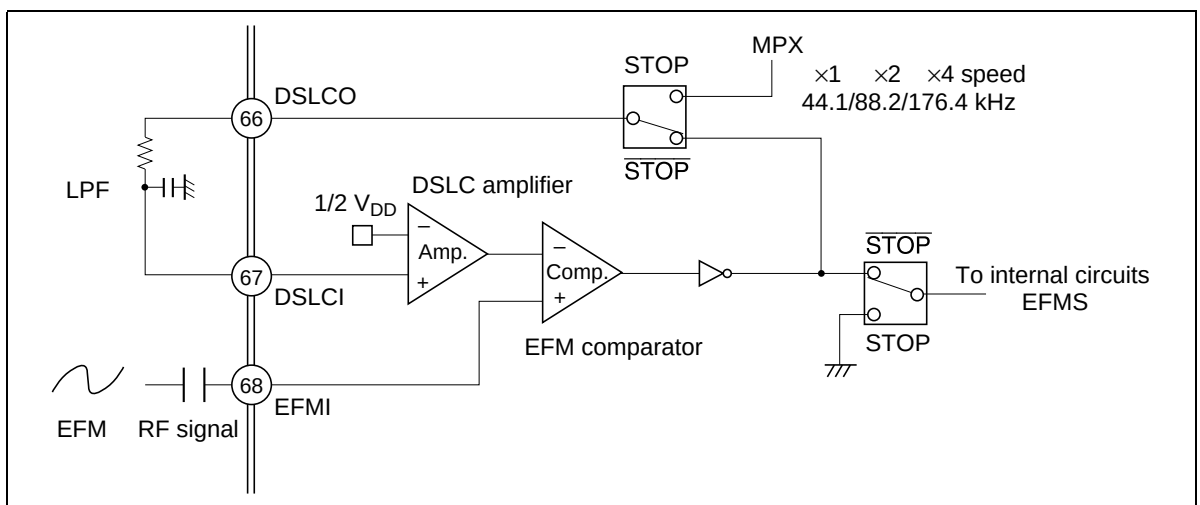
## 4. Control When a Defect is Detected

**DEFCT:** This pin inputs a disc defect detection signal. Both a digital PLL and an analog PLL are provided on-chip. Normally the analog PLL is used, because of its good error-rate characteristic, but when a defect detection signal is received at this pin, the chip switches over to its digital PLL for quick pull-in after the defect disappears. After pull-in, the chip automatically switches back to its analog PLL.

**UCK:** This pin outputs a clock signal for the microprocessor.

**UCKSL:** This pin selects the frequency of the microprocessor clock (UCK). The frequency is 16.9344 MHz when UCKSL is high, and 8.4672 MHz when UCKSL is low.

**MCK:** This pin outputs the master clock (33.8688 MHz).



**Figure 4 EFM Comparator Circuit**



## EFM Demodulation

After being processed in the data strobe block, the EFM signal is converted to NRZ by an NRZ-I conversion using a PLL-synchronized clock signal (PLL clock, 4.3218 MHz when the PLL is locked in standard speed playback mode).

The 24-bit frame synchronization signal is detected from this EFM signal. Operation of the EFM demodulation block is timed according to the occurrence of the frame synchronization signal.

Due to disc defects and other causes, frame synchronization signals may sometimes be detected at false positions in the EFM signal read from the disc. The sync protection block therefore opens a window around the time when the correct synchronization signal is expected, and frame synchronization signals are used for timing purposes only if they are detected within this window.

If the frame synchronization signal is not detected, it is automatically interpolated at the time when the correct frame synchronization signal would be expected to occur. Detection and interpolation of the frame synchronization signal will be described in detail in the description of the sync protection block.

After being converted to NRZ form, the EFM signal is converted to 14-bit parallel data by the EFM demodulation block. This conversion is timed to the occurrence of the above frame synchronization signal.

Next, 14-bit-to-8-bit demodulation is performed: the 14-bit parallel data is fed to the EFM demodulation ROM and converted to 8 bits.

After EFM demodulation, the 8-bit data is separated into subcode data, which is passed to the subcode signal-processing block, and audio data, which is output to the internal data bus. The data bus is connected to the error correction unit (ECU) and the RAM control block.

## Subcode Signal Processing

**S1:** The CD format groups subcode data into 98-frame blocks. Each block begins with two subcode synchronization signals: S0 and S1. In this chip, S0 and S1 are detected in the EFM demodulation block. S0 is delayed by one frame, then ANDed with S1, and the result (S0delay·S1) is output at the S1 pin.

Due to disc defects and other causes, the above S0 and S1 signals may sometimes fail to be detected. The chip accordingly has a divide-by-98 counter that takes S0delay·S1 as its clear input and CFCKP\* as its clock input. When S0delay·S1 is not detected, it is interpolated by this counter. See figure 5.

Note: \* CFCKP is derived from the PLL clock and has a frequency of 7.35 kHz (×1 speed), 14.7 kHz (×2 speed), 29.4 kHz (×4 speed) when the PLL is in lock.

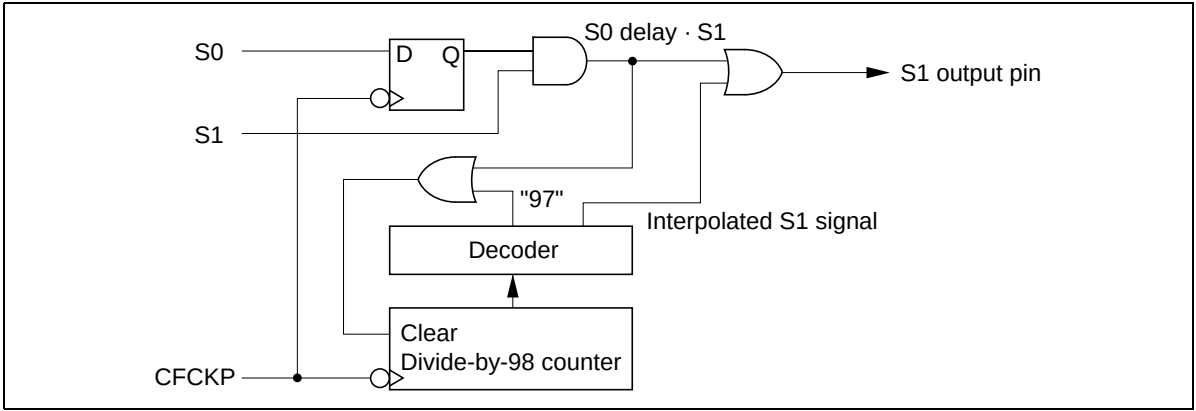


Figure 5 Block Diagram of S1 Signal Detection Circuit

**QDATA:** This is the output pin for the Q subcode data.

**QDSEL:** This pin selects one of the following two modes.

a. Q code buffer mode (selected when QDSEL is low)

When the QDSEL pin is low, the chip uses its 80-bit Q code buffer function, and outputs the Q subcode from the QDATA pin in synchronization with an external clock signal (for example, a clock signal from a microprocessor).

As shown in figure 6, the chip has two 80-bit registers. While Q code data is being written in one register, the Q code can be read from the other register asynchronously, by input of clock signals from the microprocessor at the CKEXT pin. This feature places less of a load on the microprocessor.

To switch between reading and writing of the shift registers, the S1 and QOK signals are ANDed, so before sending clock pulses for input to CKEXT, the microprocessor should check for the fall of S1, then check that QOK is high (indicating that the cyclic redundancy check of the Q data passed).

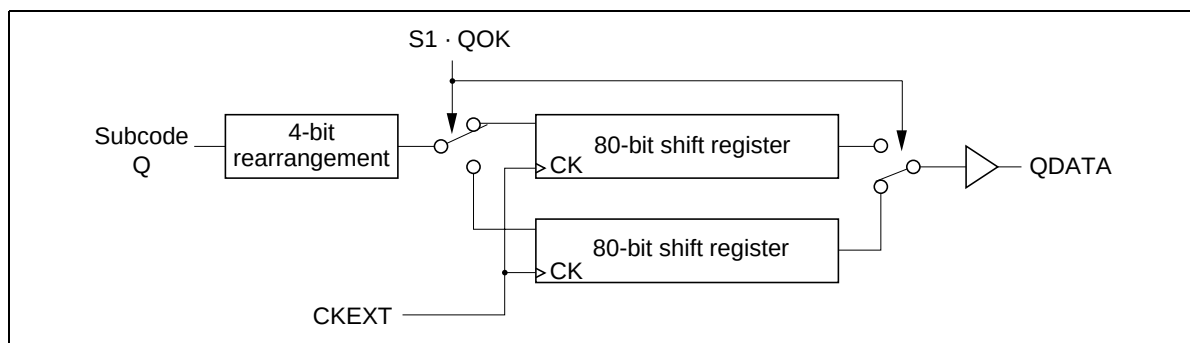
These checks will enable the Q subcode to be read correctly.

The 80-bit shift register is designed to store data in 4-bit nibbles, LSB first. If the microprocessor inputs serial data in LSB-first form, it does not have to rearrange the 4 bits.

Figure 7 shows the timing chart.

b. Q code internal synchronization mode (selected when QDSEL is high)

When the QDSEL pin is high, a Q code strobe clock generated in the HD49235 is output from the CFCKP pin, and the Q code is output from the QDATA pin at a rate of one bit per frame, synchronized with the strobe clock (CFCKP). This is referred to as Q code internal synchronization mode. Figure 8 shows the timing.



**Figure 6 Block Diagram of Q Code Buffer When QDSEL is Low**

**QOK:** The output at this pin indicates whether or not the Q subcode is correct.  
One block of Q subcode data consists of 98 bits, of which 16 bits are parity bits that indicate whether the data read from the disc was correct or in error. An on-chip cyclic redundancy check circuit decides whether the 98-bit data string is correct or not, and outputs the result at the QOK pin. A high-level output indicates OK. Figures 7 and 8 show the output timing.

In modes using the Q code buffer register, when the microprocessor sets the CRCQ bit to 1, QOK is inserted in QDATA at the rise of S1.

See the note in the timing chart shown in figure 7.

**EMP:** This output pin indicates the presence or absence of pre-emphasis. The pre-emphasis signal is detected from the Q subcode and output at the EMP pin. High output indicates audio with pre-emphasis. Low output indicates audio without pre-emphasis.

**SUBOUT:** This pin outputs codes R to W for use in display of graphics.

**CFCKP:** This pin outputs a subcode frame synchronization signal.

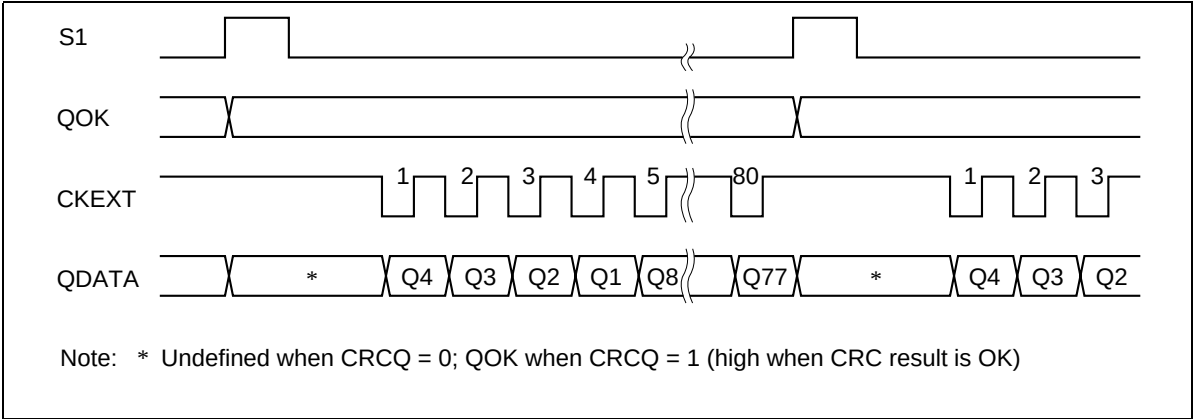


Figure 7 Timing When QDSEL is Low (Q Code Buffer Mode)

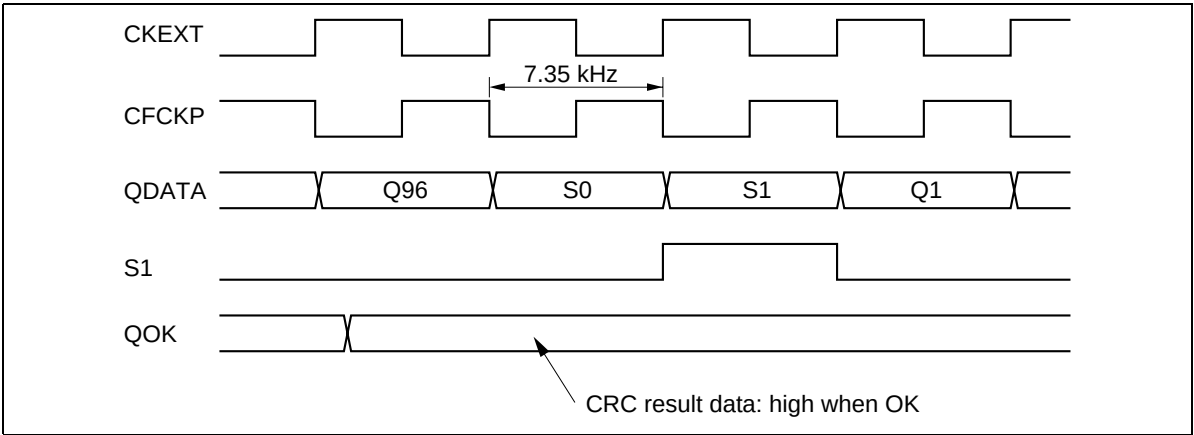


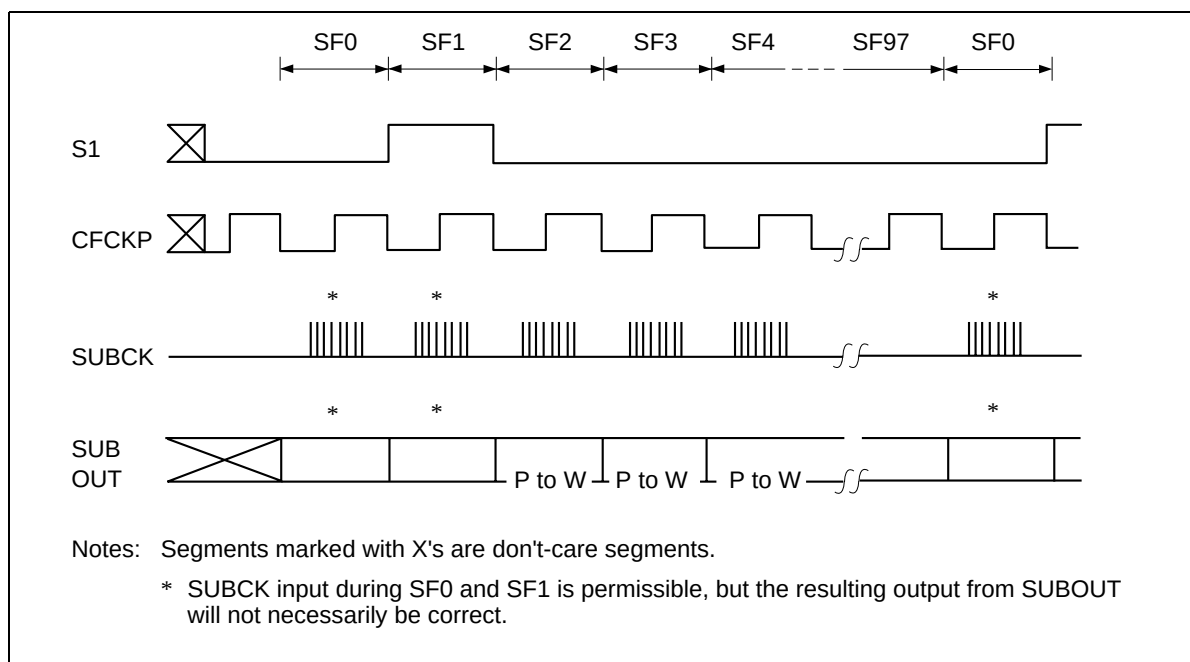
Figure 8 Timing When QDSEL is High(Q Code Internal Synchronization Mode, Standard Speed Playback)

**SUBCK:** This pin inputs a subcode read clock.

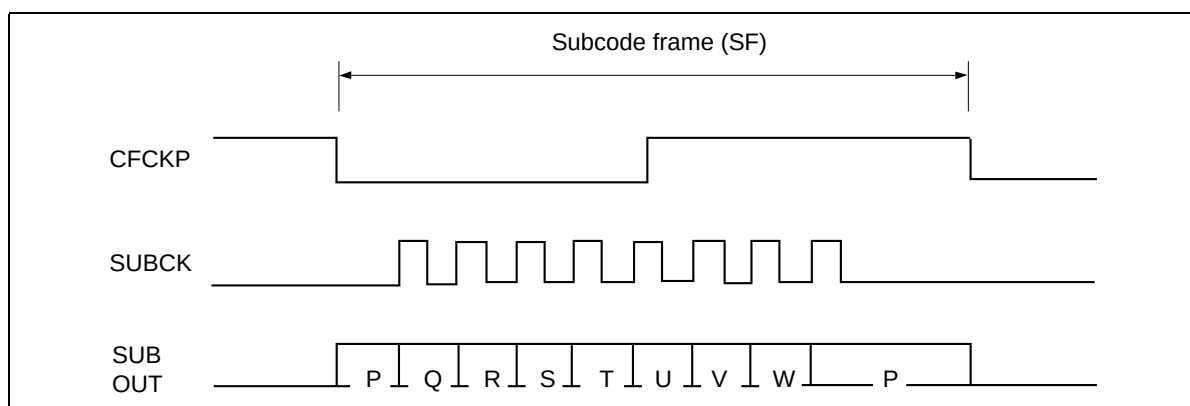
Codes R to W are output together with codes P and Q. The codes are output in order, starting with the P code, as serial data from the SUBOUT pin when read clock pulses are input at the SUBCK pin. Figure 9 shows the timing, which basically conforms to EIAJ CP-2401.

**Signal Configuration:** Figure 9 shows the signals output for use in display of graphics. (SF: subcode frame)

To read the subcode data, eight subcode clock pulses (SUBCK) should be input after the fall of the subcode frame synchronization signal (CFCKP). The data for subcode channel P is output at the fall of CFCKP. Data in channels Q to W is output at the rise of SUBCK. See figure 10.



**Figure 9 Output Timing for Graphics Display (1)**



**Figure 10 Output Timing for Graphics Display (2)**

## Control of 16-kbit On-Chip SRAM

The demodulated EFM data is synchronized with the PLL clock, and its output timing may contain jitter due to disturbances in the CLV servo that controls disc rotation. To absorb the jitter, the demodulated EFM data is stored in the on-chip RAM, then read out in synchronization with a clock signal derived from the crystal oscillator. The RAM capacity sets a limit on the amount of jitter that can be absorbed. In this chip, a delay of  $\pm 5$  frames between RAM read and write would lead to overwriting of existing data. The overwritten data would be destroyed, making the reproduced sound unreliable.

To avoid this, if the read and write base counters get more than  $\pm 5$  frames out of step, the write base counter is set to the value of the read base counter and the frame jitter margin is set to the maximum,  $\pm 5$  frames.

**OVFW:** This pin outputs a high RAM overflow flag signal to indicate that the difference between the read and write base counters exceeded  $\pm 5$  frames and the write base counter was set to the value of the read base counter.

**MUTE:** This pin is used to force the audio data to the mute state.

When MUTE is low, muting is not performed.

When MUTE is high, muting is performed.

When MUTE goes high, the address control circuit is initialized so as to maximize the RAM frame jitter margin at that point. This initialization is performed continuously while MUTE is high. Normal reproduction resumes when MUTE goes low.

## Error Correction Unit (ECU)

The error correction unit can correct two-symbol C1 errors and four-symbol C2 errors.

The results of C1 error correction are flagged by a C1 flag. Since two-symbol errors can be corrected, each C1 correction produces a 2-bit C1 flag. The C1 flag data is written into an internal buffer RAM area and is read out again during C2 correction.

C2 error correction is carried out using the calculated error locations and error values, and the C1 error status and error positions indicated by the C1 error flags.

The interpolation block reads audio data and the corresponding C1 and C2 flags. If it decides from the C1 and C2 flags that the audio data is unreliable, it performs mean-value interpolation or preceding-value interpolation.

**TC1:** This pin outputs a signal indicating whether each frame of data read from the disc contained an error. See figure 11 for the output timing.

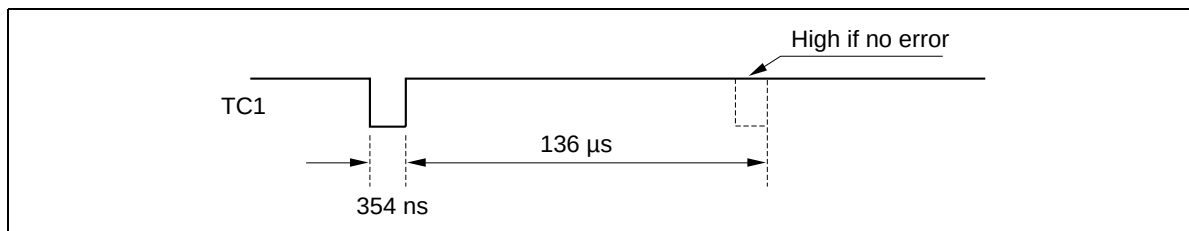


Figure 11 TC1 Timing (Standard Speed Playback)

## Microprocessor Interface

**DATA:** Input pin for receiving microprocessor command data.

**CLK:** Clock input pin for receiving microprocessor command data.

**XLT:** Latch clock input pin for storing microprocessor command data in an internal register after serial input.

**XRST:** Input pin for clearing the microprocessor command registers.

**SENS:** This output pin provides the microprocessor with the following servo information. For details, see the microprocessor command descriptions.

- The SENS signal goes low when the number of pulses input at the CNIN pin reaches a value set by the microprocessor. Alternatively, SENS toggles between low and high each time this value is reached.
- When the constant linear velocity (CLV) servo operates in brake mode, SENS goes low to indicate detection of an interval of 32 T or more. This indicates that braking has operated and the velocity has fallen to 1/3 or less.

**CNIN:** This pin receives track-crossing pulses from the servo IC, so that the number of tracks can be counted.

### 1. Data Transfer Format

The microprocessor interface transfers serial data using three signal lines: XLT, CLK, and DATA. See the timing diagram in figure 12. D11 to D8 specify a register address and D7 to D0 give bit values to be set in that register.

- Notes:
1. When the external reset input signal (XRST) goes low all registers are reset to their default values. See table 1.
  2. Always write 0 in the following register bits:
    - D2 in register 8
    - D3 in register E
    - D7 and D6 in register F
  3. Always write 1 in the following register bit:
    - D7 in register 9

**Table 1      Default Values**

| Register Code | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|----|----|----|----|----|----|----|----|
| 8 (1000)      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 9 (1001)      | 1  | 0  | 0  | 0  | 1  | 1  | 0  |    |
| A (1010)      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| B (1011)      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| C (1100)      | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 1  |
| D (1101)      | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| E (1110)      | 0  | 0  | 0  | 0  | 0  |    |    |    |
| F (1111)      | 0  | 0  | 0  |    |    |    |    |    |

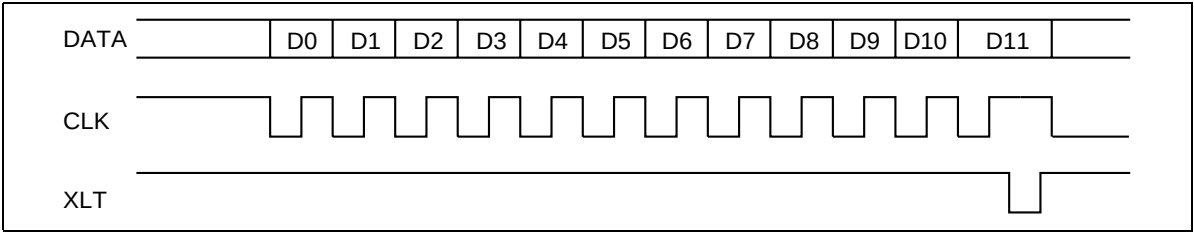


Figure 12 Microprocessor Interface Timing

2. Microprocessor Commands

These commands are summarized in the microprocessor command tables. Further details and notes are given below.

a. Mode Selections (Register 8)

- ROM:** This bit controls whether or not interpolation is performed on audio data output from DAS. When ROM = 0, interpolation is performed (for audio applications). When ROM = 1, interpolation is not performed (for CD-ROM applications).
- ROMEf:** When ROM = 1 (for CD-ROM applications), the upper and lower C2 flag data is output in two 8-bit segments. ROMEf selects which is output first: the upper or lower data. When ROMEf = 0, the lower data is output first. When ROMEf = 1, the upper data is output first.
- DOOFF:** This bit switches the digital audio interface output from pin 17 (BIDAT) on or off. When DOOFF = 0, a signal is output. When DOOFF = 1, the BIDAT pin is in the high-impedance state.
- SUBCO:** This bit selects whether to insert subcode data in the DAS output on the DAC output interface (MPX, CKX, DAS) in 48fs clock mode (when microprocessor command bit SLTSW is 0). When SUBCO = 0, subcode data is not inserted. When SUBCO = 1, subcode data is inserted.
- SLTSW:** This bit selects 48fs clock mode or 64fs clock mode for the DAS output. When SLTSW = 0, DAS data is output in 48fs clock mode. When SLTSW = 1, DAS data is output in 64fs clock mode.
- DCOND:** This bit selects the condition for switching from the analog PLL to the digital PLL when a defect is detected, in terms of the width of the defect detection signal input at the DEFCT pin (pin 69). When DCOND = 0, the width must be at least four frames. When DCOND = 1, the width must be at least eight frames.

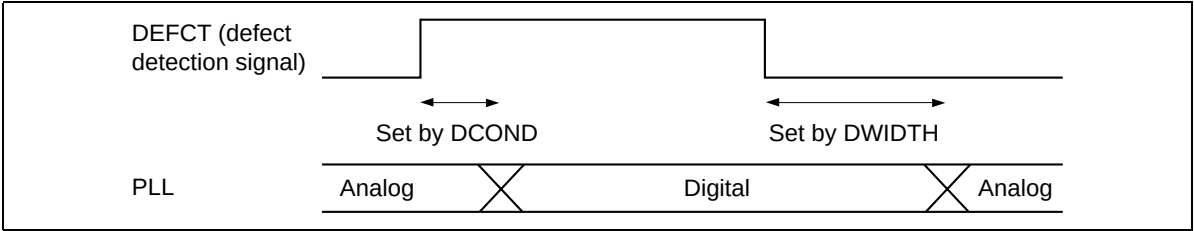


Figure 13 PLL Modes when a Defect is Detected



**DWIDTH:** This bit selects the interval from the high-to-low transition of the defect detection signal until termination of the digital PLL (and return to the analog PLL).

When DWIDTH = 0, termination occurs 8 frames past the fall of the defect detection signal if the defect detection signal width was less than 12 frames, and 16 frames past the fall of the defect detection signal if the defect detection signal width was 12 frames or more.

When DWIDTH = 1, termination occurs 4 frames past the fall of the defect detection signal if the defect detection signal width was less than 12 frames, and 8 frames past the fall of the defect detection signal if the defect detection signal width was 12 frames or more.

b. Function Selections (Register 9)

**BI0 and BI1:** These bits select normal play, double-speed play, or quadruple-speed play.

Note: When changing the playback speed, always switch the system to CLV stop mode so that the free-running frequency is adjusted automatically. The period of setting is 30 msec or more.

**WG10TL:** This bit selects the width of the frame synchronization signal (SYNC) detection window.

WG10TL = 0: The window width is  $\pm 10 T$ .

WG10TL = 1: The window width is  $\pm 19 T$ .

**SYLCK0 and SYLCK1:** These bits select whether the sync protection state is maintained for 2, 4, 8, or 12 consecutive frames in which the frame synchronization signal (SYNC) is not detected.

**CRCQ:** In Q code buffer mode (when the QDSEL signal at pin 65 is low), this bit selects whether or not to insert the QOK flag into the Q code data.

c. Audio Control (Register A)

The audio control commands concerning the DAS output are all ignored in CD-ROM mode, which is selected when the ROM microprocessor command bit is set to 1.

**MUTEL and MUTER:** These command bits mute the left and right channels independently.

Attenuation is carried out in eight steps (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8, 0) with 136  $\mu$ s per step (at standard speed).

Notes: 1. Muting begins as soon as the command is input, without waiting for a zero-crossing point.

2. If the external MUTE signal is high, both channels are muted regardless of these commands.

**MONO:** This bit selects monaural audio output.

Note: When MONO is set to 1, mean-value interpolation is not performed. The only type of interpolation performed is to hold the preceding value.

**ATT:** This bit attenuates the audio output level by -12 dB in six steps (7/8, 6/8, 5/8, 4/8, 3/8, 2/8).

Note: If the external MUTE signal is high, both channels are muted regardless of this command bit.

**BLGMAIN and BLGSUB:** These bits select whether or not to output bilingual audio on the left and right channels. This command is ignored if "SWLR" = 1.

**SOFTMT:** This command bit mutes both the left and right channels simultaneously. Attenuation is carried out in eight steps with 136  $\mu$ s per step (at standard speed).

Note: If the external MUTE signal is high, both channels are muted regardless of this command bit.

**SWLR:** Reverses the left- and right-channel outputs, by reversing DATA from RAM.

Note: Clear this bit to 0 when using DAS subcode output.

## d. Track Counter Setting (Register B)

An internal counter counts the track-crossing signal input at the CNIN pin. When the count reaches the value set in register B, the SENS output inverts.

Depending on the order in which registers B and C are set, tracks are counted in complete mode (once only) or count mode (repeatedly). See the timing diagram in figure 14.

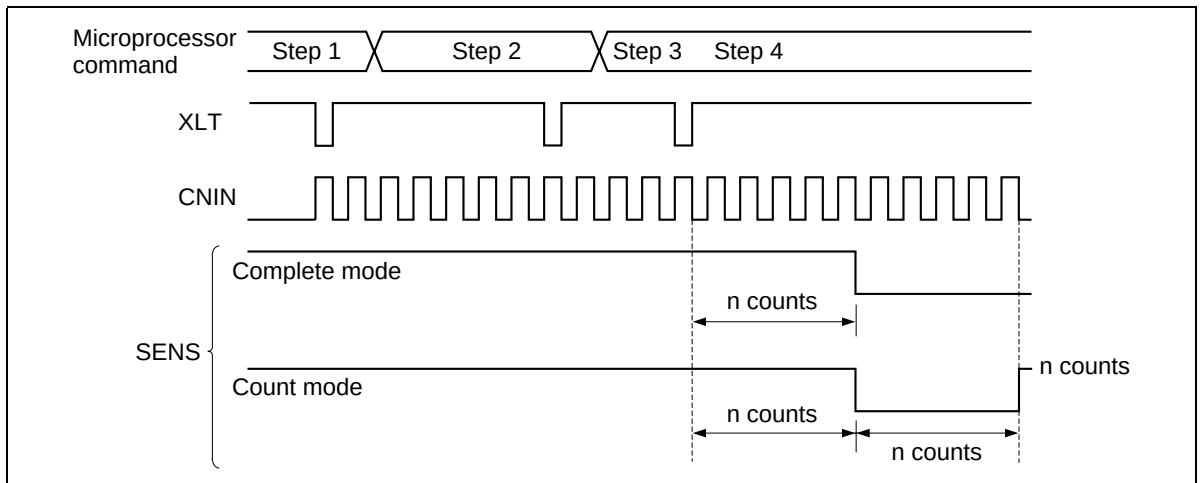
### — Complete mode

Step 1: Set desired values in all registers other than registers B and C.

Step 2: Set register C.

Step 3: Set the count value in register B.

Step 4: Monitor the SENS line at the microprocessor.



**Figure 14 Track Counting**

### — Count mode

Step 1: Same as complete mode.

Step 2: Set the count value in register B.

Step 3: Set register C.

Step 4: Monitor the SENS line at the microprocessor.

- Notes:
1. Do not use the microprocessor interface while the microprocessor is monitoring the SENS line.
  2. If all zeros are written in register B, the count setting is 256.
  3. Do not monitor the SENS pin between steps 2 and 3.

e. CLV Control (Register C)

**AINTV:** When a disc is played in CLV mode, the switchover between the starting servo and normal servo modes is made automatically by testing the number of sync pulses per interval. The AINTV bit selects the length of the interval.

**ATH:** When a disc is played in CLV mode, the switchover between the starting servo and normal servo modes is made automatically by testing the number of sync pulses per interval. The ATH bit selects the threshold number of pulses. Starting servo mode is used if the number of sync pulses detected in the interval selected by AINTV is less than the threshold value selected by ATH. Normal servo mode is used if the number exceeds this threshold. Only sync pulses that are validated by the sync protection function are counted.

**GAIN1 and GAIN0:** These command bits select the gain of the output at the PWM pin in normal CLV servo mode. There are three selections: -6 dB, 0 dB, and +6 dB.

**SGAIN1 and SGAIN0:** These bits select the PWM gain to be one of three values, -6 dB, 0 dB or 6 dB, in start mode.

**PDGAIN1 and PDGAIN0:** These bits select the MSTOP pin output (CLV phase error) gain to be one of three values, -6 dB, 0 dB or 6 dB.

f. CLV Kick Control (Register D)

**KICK7 to KICK1:** When kick control is enabled (by microprocessor command register E) in CLV mode, these bits select the CLV control output pin PWM duty cycle to be one of 128 levels. For example, to set the duty to be 74/128, set bits D7 to D0 in microprocessor control register D to be 1001010 (base 2).

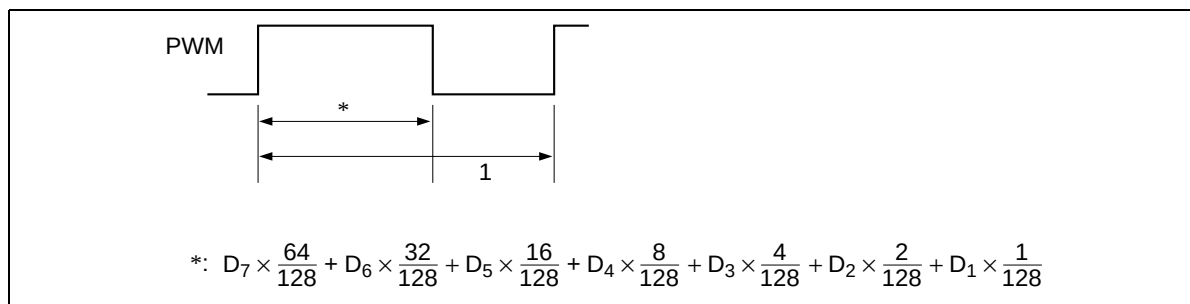


Figure 15 CLV Kick Control Output

g. CLV Mode (Register E)

This register determines the constant linear velocity control mode. Command data written in bits D7 to D4 (ED3 to ED0) of register E selects stop, play, rotate, kick, brake, access, start, or normal mode. For details of these operating modes, see the description of the CLV servo block.

h. ECU Mode (Register F)

The error-correcting capability of the error-correcting unit (ECU) can be selected. Correction when a track jump occurs can be limited to two symbols at the C1 level and three symbols at the C2 level by setting bit AS0 to 1, to reduce the likelihood of false corrections.

### Sync Protection Block

The pulse width of the EFM signal read from the disc is measured, using the crystal oscillator clock as a time base. The pulse width value is used to detect the synchronization pattern consisting of the first 24 bits in each frame, and produce a synchronization pulse named ASYNC.

Due to disc defects and other causes, ASYNC may be detected in an incorrect position, so a divide-by-576 counter\* is used to establish a window, and only ASYNC pulses detected within this window are regarded as valid synchronization pulses (referred to as valid ASYNC pulses). Other synchronization pulses are disregarded. The width of this window can be set to one of two values by the microprocessor command WG10TL as follows.

WG10TL = 0: The window width is set to  $\pm 10T$  ( $\pm 1.7\%$ )

WG10TL = 1: The window width is set to  $\pm 19T$  ( $\pm 3.1\%$ )

Valid ASYNC pulses occur with correct synchronization timing, but they may sometimes be missing, e.g. because of rejection of pulses outside the detection window. Where valid ASYNC pulses are missing, PSYNC pulses are generated by interpolation. Valid ASYNC and PSYNC are the basic constant linear velocity control signals used in the CLV motor control circuit.

When two consecutive valid ASYNC pulses are detected, the chip assumes that it has acquired synchronization lock and drives the SLOCK pin high.

If valid ASYNCS are not detected for a consecutive number of times set by the SYLCK0 and SYLCK1 microprocessor command bits, interpolation is stopped and the SLOCK pin is driven low.

When (SYLCK1, SYLCK0) are (0, 0): if ASYNCS are missing for 2 consecutive times interpolation is stopped and the SLOCK pin goes low.

When (SYLCK1, SYLCK0) are (0, 1): if ASYNCS are missing for 4 consecutive times interpolation is stopped and the SLOCK pin goes low.

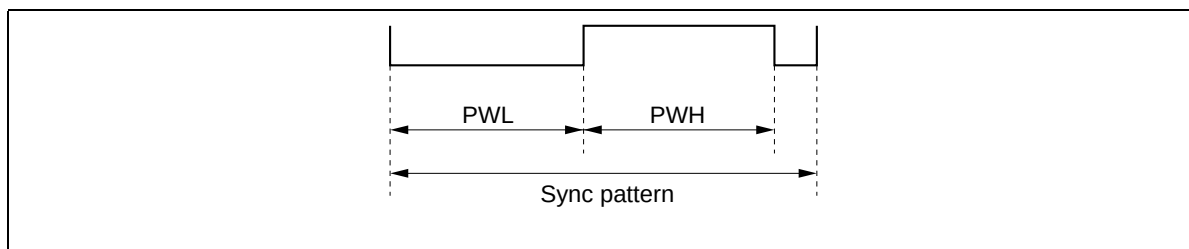
When (SYLCK1, SYLCK0) are (1, 0): if ASYNCS are missing for 8 consecutive times interpolation is stopped and the SLOCK pin goes low.

When (SYLCK1, SYLCK0) are (1, 1): if ASYNCS are missing for 12 consecutive times interpolation is stopped and the SLOCK pin goes low.

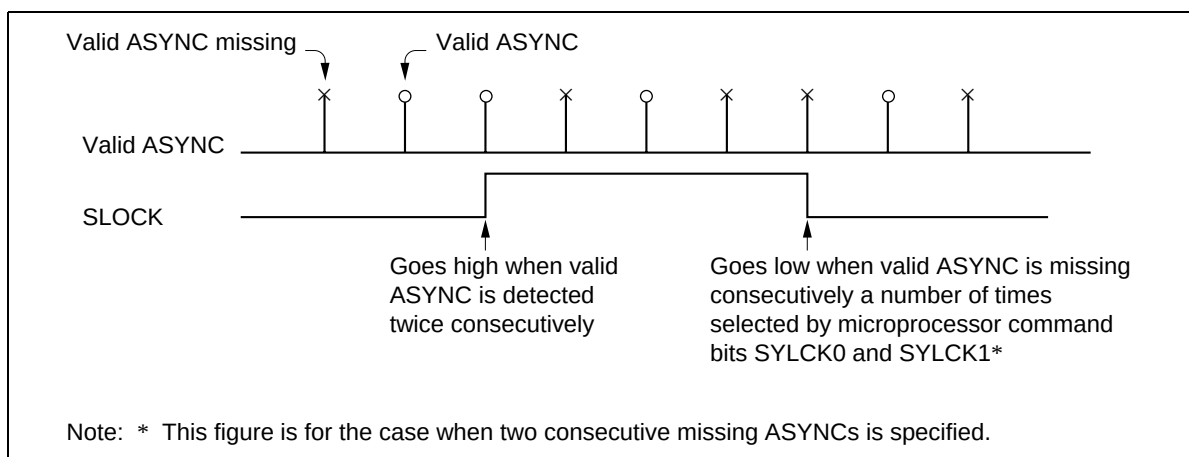
Figure 17 is a timing diagram for the valid ASYNC and SLOCK relationships for the case where detection of two consecutive missing valid ASYNCS was specified by microprocessor command.

Note: \*  $4.2336 \text{ MHz}/576 = 7.35 \text{ kHz}$  (standard speed playback)

**SLOCK:** This output pin indicates whether sync signals were detected correctly during disc playback. This signal goes high when correct sync signals are detected in two consecutive frames, and goes low when sync signals are missing consecutively for the number of times specified by the SYLCK0 and SYLCK1 microprocessor command bits.



**Figure 16 Sync Pattern at Start of Frame**



**Figure 17 Valid ASYNC and SLOCK Relationships**

CLV Servo Control

Compact discs (CDs) are recorded at a constant linear velocity (CLV). This block performs CLV motor control.

**MSTOP:** This CLV phase error output pin either is in the high-impedance state, or outputs a constant low signal, a constant high signal, or a pulse-width modulated waveform with a duty cycle of 0 to 100%, depending on the CLV operating mode.

**PWM:** This CLV velocity error output pin either is in the high-impedance state, outputs a constant low signal, outputs a constant high signal, or outputs a pulse-width modulated waveform with a duty cycle of 0 to 100%, depending on the CLV operating mode.

**MON:** This output signal indicates when the disc motor is on. When the disc motor is on, this pin is at the high level, except in stop mode.

**PW64:** This pin outputs the brake release signal.

**ROTD:** This pin can be used to monitor the most significant bit of the 7-bit (128-step) output at the PWM pin.

**CLVS:** This output pin differentiates between the starting and normal CLV modes. High output indicates normal mode.

Next the operating modes will be described. Table 2 indicates the CLV control output states in each mode.

Table 2 CLV Control Output

| CLV Mode | ED3 to 0 | Outputs Signals |                                                |                       |
|----------|----------|-----------------|------------------------------------------------|-----------------------|
|          |          | MON             | MSTOP (Phase Error)                            | PWM (Speed Error)     |
| STOP     | 0000     | L               | Z                                              | Z                     |
| PLAY     | 0110     | H               | 50% (starting mode)<br>0 to 100% (normal mode) | 0 to 100%             |
| ROT      | 1000     | H               | 50%                                            | H                     |
| KICK     | 1001     | H               | 50%                                            | Set by microprocessor |
| BRAKE    | 1010     | H               | 50%                                            | L                     |
| ACS      | 1100     | H               | 50%                                            | 0 to 100%             |
| START    | 1110     | H               | 50%                                            | 0 to 100%             |
| NORM     | 1111     | H               | 0 to 100%                                      | 0 to 100%             |

1. Stop Mode

This is the state in which the motor is stopped. The free-running frequency of the data strobe VCO is automatically adjusted in this mode.

## 2. Play Mode

This mode is automatically subdivided into a starting mode (rough servo control) and normal mode (fine servo control) according to the rate at which sync signals are detected from the disc. The AINTV and ATH bits in register C (CLV control) select an interval length and threshold value. Starting mode is used if the number of sync signals in the selected interval is less than the threshold value. Normal mode is used if the number exceeds the threshold value. Starting and normal modes operate as follows.

**Starting Mode:** See table 2 for the outputs at the MON and MSTOP pins. The PWM pin outputs a rectangular wave with a duty cycle corresponding to the arithmetic mean of the pulse width on the 11-T low side and 11-T high side in the sync signal detected from the disc. See the PWM output duty cycle characteristic in figure 18.

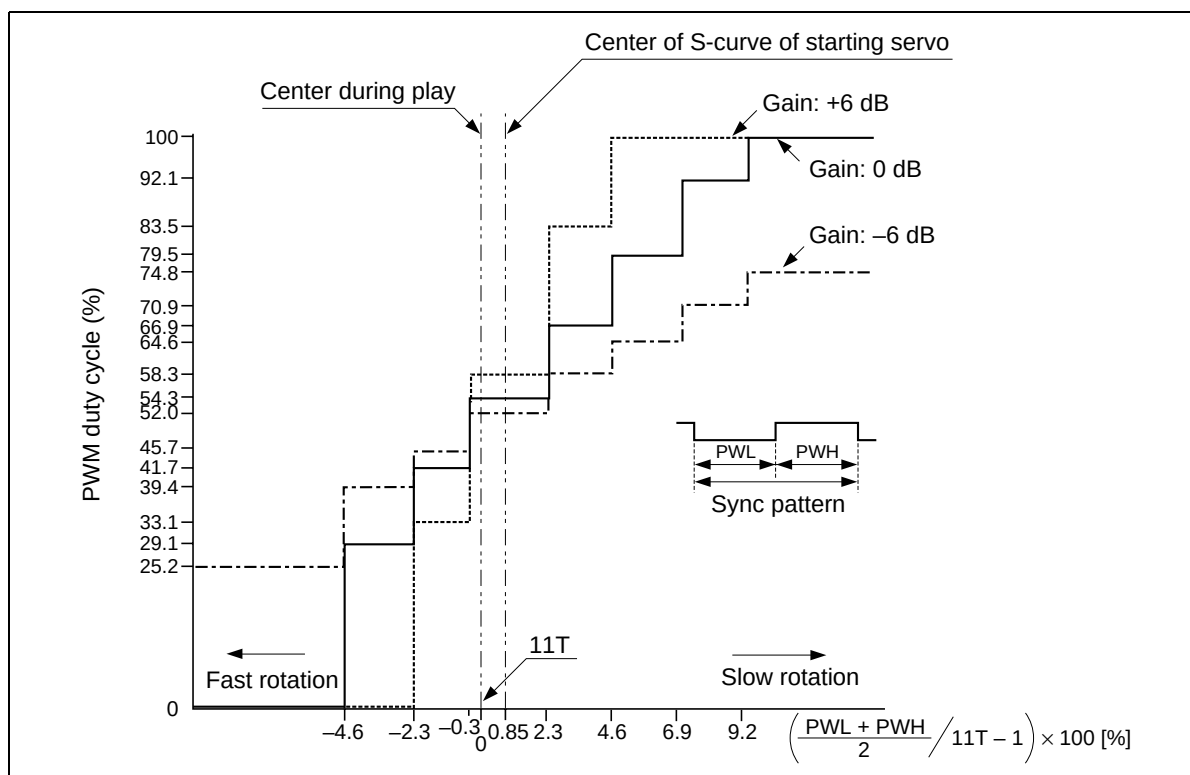


Figure 18 Duty Cycle Characteristic of PWM Output (Speed Error) in CLV Starting Mode

**Normal Mode:** The MON output pin is held high. The PWM pin outputs a rectangular wave with a duty cycle that depends on the length of four cycles of the sync signal reproduced from the disc (four frames). See the PWM output duty cycle characteristic in figure 19. The MSTOP pin outputs a phase error signal obtained by comparing the phase of a signal obtained by prescaling the sync signal by a factor of four (to give a cycle length of four frames) with the phase of an internal reference signal. See the MSTOP output duty cycle characteristic in figure 20.

## 3. Rotate Mode

The MON and PWM outputs are held high. The MSTOP pin outputs a square wave with a 50% duty cycle. This mode is used to force the disc motor to rotate.

## 4. Kick Mode

The MON output pin is held high. The MSTOP pin outputs a square wave with a 50% duty cycle. The PWM pin outputs a rectangular wave with a duty cycle that can be set to any value from 0 to 100% in 128 steps by setting bits KICK7 to KICK1 in microprocessor command register D.

## 5. Brake Mode

The MON output is held high. The MSTOP pin outputs a square wave with a 50% duty cycle. The PWM output is held low. This mode is used to force the disc motor to rotate in reverse. In brake mode, the interval between edges of the EFM signal is measured. If the interval is 32 T or more ( $T = 1/4.3218$  MHz) the SENS output is driven low and the PW64 output is driven low. These outputs can be monitored to find if braking has been effective.

## 6. Access (ACS) Mode

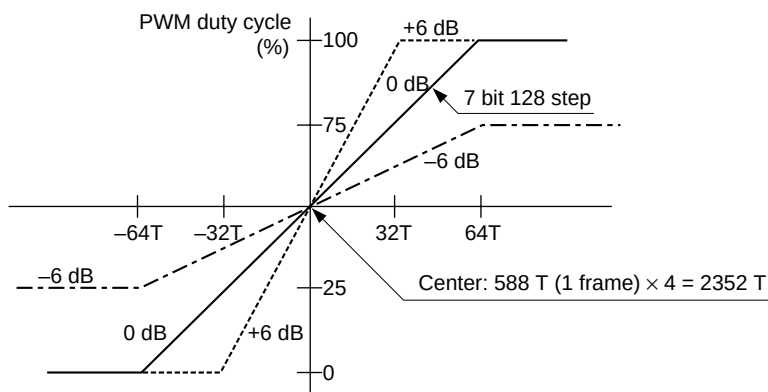
Operation is the same as in the starting submode of play mode. This mode is used in track access.

## 7. Start mode

Operation is the same as in the starting submode of play mode.

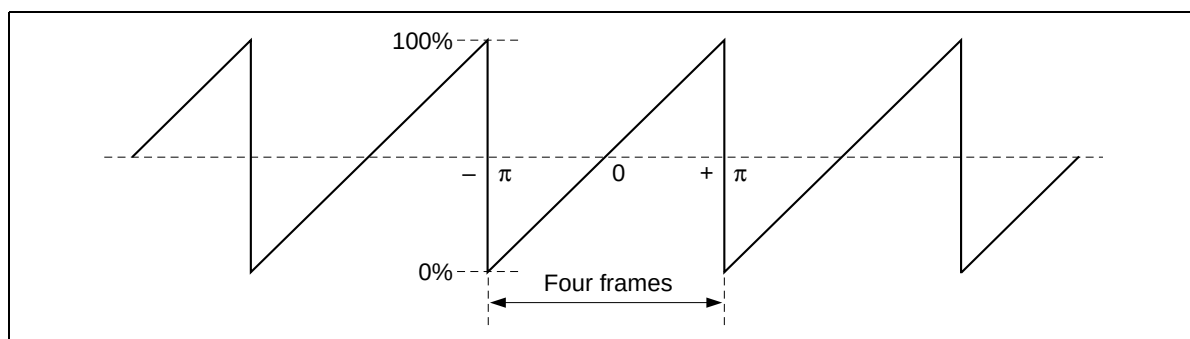
## 8. Normal Mode

Operation is the same as in the normal submode of play mode.

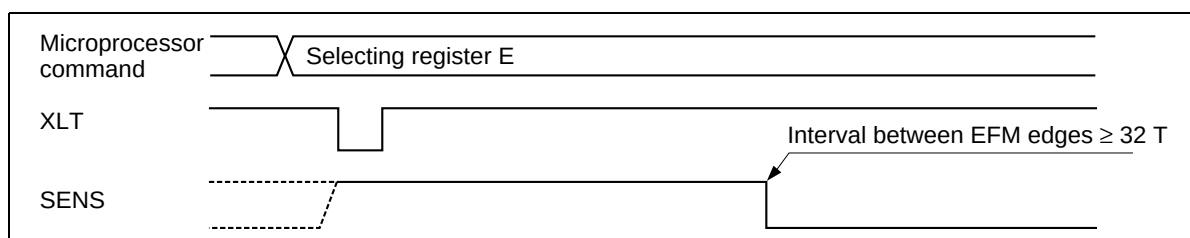


**Figure 19 Duty Cycle Characteristic of PWM Output (Speed Error) in CLV Normal Mode**





**Figure 20 Duty Cycle Characteristic of MSTOP Output for Constant Linear Velocity Control**



**Figure 21 SENS Output in Brake Mode**

## Digital Audio Interface

**BIDAT:** Digital audio interface output pin. The output can be switched on or off by microprocessor command DOOFF (in register 8).

## Interpolation

A microprocessor command SLTSW (register 8) can select the 48-fs or 64-fs clock. Figures 22 and 23 show the output timing. With the 48-fs clock, a microprocessor command SUBCO (register 8) can select whether or not to insert subcode data in the DAS output. Figures 24 and 25 show the output timing.

**DAS:** This pin outputs audio or ROM data. The ROM microprocessor command (in register 8) can select whether or not to carry out interpolation. Preceding-value and mean-value interpolation are carried out. With a 48-fs clock, the data is output MSB first and squeezed to the rear. With a 64-fs clock, the data is output LSB first and squeezed to the rear.

**CKX:** This pin outputs the data transfer clock.

**MPX:** This pin outputs a signal that distinguishes between the left and right channels. With a 64-fs clock, low output indicates the left channel and high output indicates the right channel. With a 48-fs clock, this polarity is reversed.

**QMX:** This pin outputs a clock signal with four times the frequency of MPX.

**DMX:** This pin outputs a clock signal with two times the frequency of MPX.

---

## HD49235FS

---

**C2F:** This output pin goes high to flag data errors that could not be corrected by C2 error correction. C2F is low when there are no such uncorrectable errors. C2F is synchronized to the data output on the DAS line. When audio is selected by the ROM microprocessor command, this signal is output once for every two bytes on the left and right channels. When CD-ROM is selected, the signal is output once per byte (every 8 bits).

See figure 26 for the output timing.

**MUTE:** Selects whether to mute the audio data.

Low: Muting is not performed.

High: Muting is performed.

When MUTE goes high, the address control circuit is initialized so as to maximize the RAM frame jitter margin at that point. This initialization is performed continuously while MUTE is high. Normal reproduction resumes when MUTE goes low.

### Other Pins

**MRST:** Master reset. The HD49235FS chip resets when MRST goes low, and operates normally when MRST is high. This pin has a pull-up resistor, so it can be either left open or connected to  $V_{DD}$ .

**TEST1 to TEST3:** These pins input test control signals. These pins have pull-up resistors, so they can be either left open or connected to  $V_{DD}$ .

**$V_{DD}$ :** Power supply pin.

**$V_{SS}$ :** Ground pin.

**NC:** These pins should be left unconnected. Correct operation is not assured if they are connected.

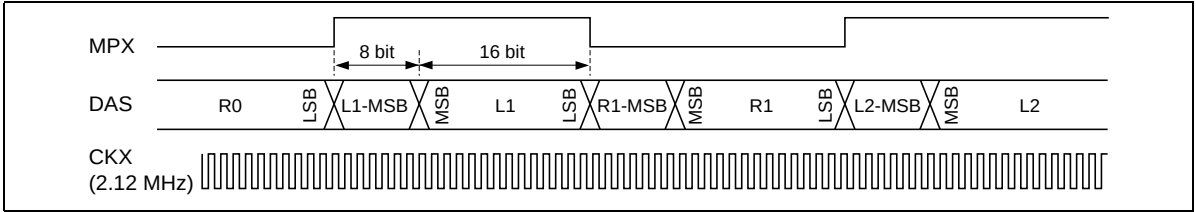


Figure 22 Audio/ROM Data Output Sequence (When 48-fs Clock is Selected):  
DAS Switched at Fall of CKX

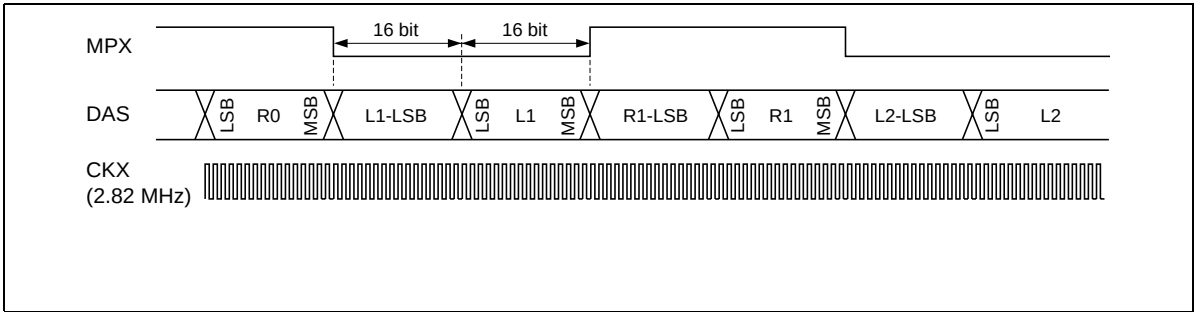


Figure 23 Audio/ROM Data Output Sequence (When 64-fs Clock is Selected):  
DAS Switched at Rise of CKX

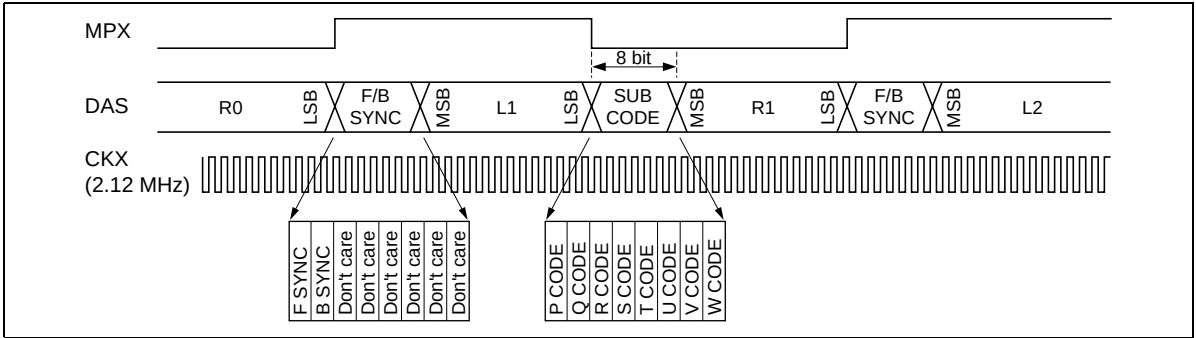


Figure 24 Audio/ROM Data Output Sequence with Subcode Data Inserted (When 48-fs  
Clock is Selected): DAS Switched at Fall of CKX

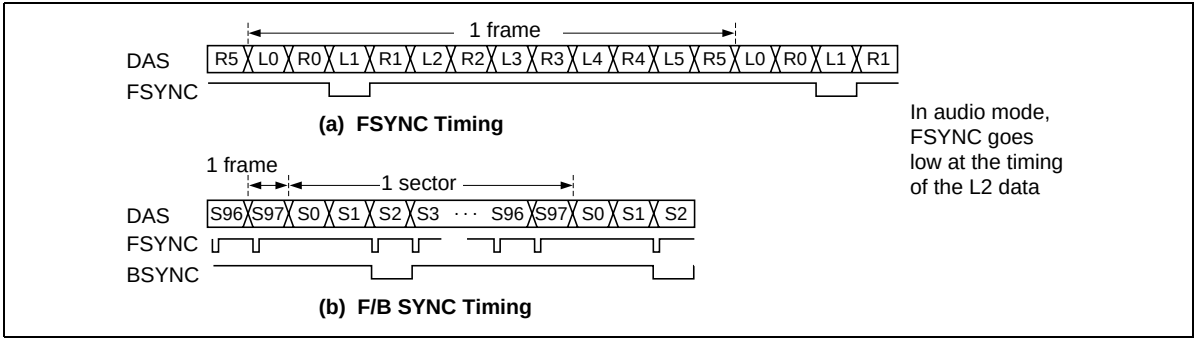


Figure 25 F/B SYNC Signal Timing Diagram

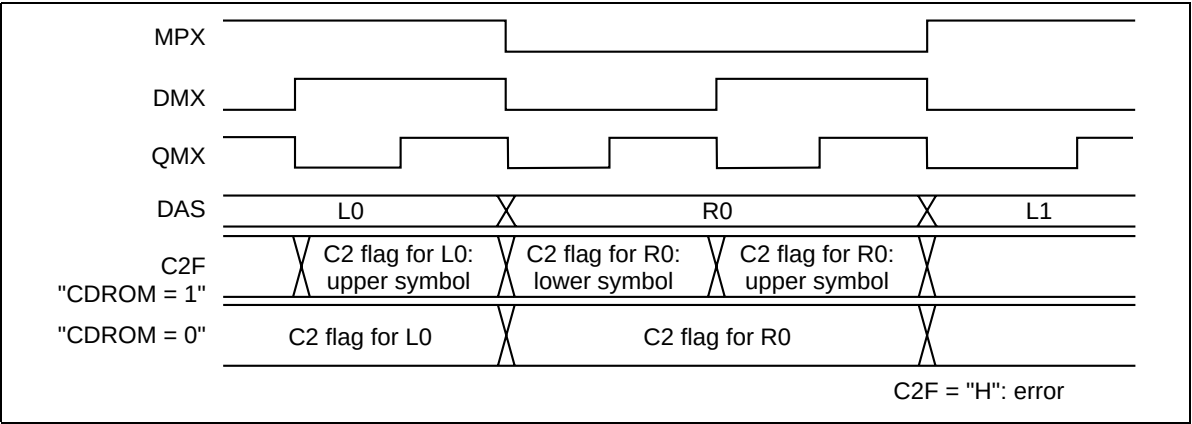


Figure 26 Error Flag Output (Switchable by Upper/Lower-1st Command in ROM Mode)

**Absolute Maximum Ratings** ( $T_a = 25^{\circ}\text{C}$ ,  $V_{ss} = 0\text{ V}$ )

| Item                        | Symbol    | Value                  | Unit               |
|-----------------------------|-----------|------------------------|--------------------|
| Supply voltage              | $V_{DD}$  | -0.3 to +7.0           | V                  |
| Pin voltage*                | $V_T$     | -0.3 to $V_{DD} + 0.3$ | V                  |
| Allowable power dissipation | $P_d$     | 450                    | mW                 |
| Operating temperature       | $T_{opr}$ | 0 to +75               | $^{\circ}\text{C}$ |
| Storage temperature         | $T_{stg}$ | -55 to +125            | $^{\circ}\text{C}$ |

Note: \*  $V_{DD} + 0.3\text{ V} < 7.0\text{ V}$

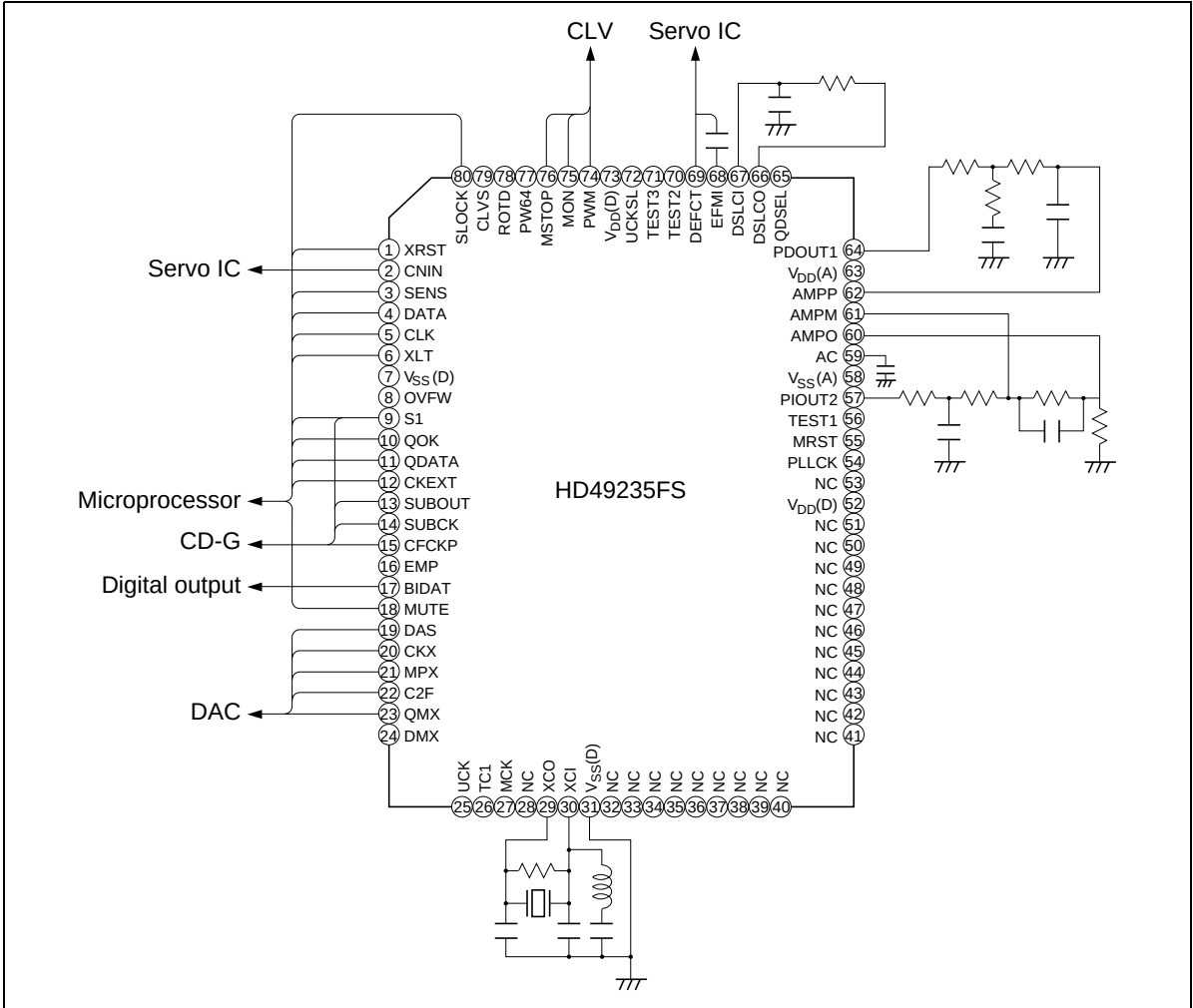
# HD49235FS

## Electrical Characteristics

| Item                         | Symbol    | Min                 | Typ | Max                 | Unit | Test Conditions                                     | Applicable Pin(s) |
|------------------------------|-----------|---------------------|-----|---------------------|------|-----------------------------------------------------|-------------------|
| Operating supply voltage     | $V_{DD}$  | 4.5                 | 5.0 | 5.5                 | V    | Normal-speed, double-speed, or quadruple-speed play | 52, 63, 73        |
| Input voltage (high)         | $V_{IH}$  | $0.7 \times V_{DD}$ | —   | —                   | V    |                                                     | *1                |
| Input voltage (low)          | $V_{IL}$  | —                   | —   | $0.3 \times V_{DD}$ | V    |                                                     |                   |
| Output high voltage 1        | $V_{OH1}$ | $V_{DD}-0.5$        | —   | —                   | V    | $-I_{OH} = 0.6 \text{ mA}$                          | *2                |
| Output low voltage 1         | $V_{OL1}$ | —                   | —   | 0.4                 | V    | $I_{OL} = 0.6 \text{ mA}$                           |                   |
| Input leakage current        | $I_{IL}$  | −5                  | 0   | 5                   | μA   |                                                     | *1                |
| Three-state leakage current  | $I_{TOL}$ | −5                  | 0   | 5                   | μA   | Three-state output pins in high-impedance state     | 3, 17, 74, 75     |
| Input pin pull-up resistance | Rip       | 10                  | 20  | 40                  | kΩ   |                                                     | 55, 56, 65, 72    |
| Amplifier output             | $V_{AO}$  | 2.4                 | 2.5 | 2.6                 | V    | $V_{AP}$ input (at AP pin): 2.5 V                   | 60                |
| VCO output                   | PLLCK     | 4.2                 | 4.7 | 5.2                 | MHz  | Normal speed                                        | 54                |

- Notes: 1. Input pins and I/O pins in input mode (except analog pins): 1, 2, 4, 5, 6, 12, 14, 18, 55, 65, 67, 69, 72.
2. The following output pins, I/O pins in output mode, and three-state output pins: 3, 8 to 11, 13, 15, 16, 17, 19 to 27, 57, 64, 66, 74 to 80

Application External







## Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

## Sales Offices

# HITACHI

### Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

|     |              |   |                                                                                             |
|-----|--------------|---|---------------------------------------------------------------------------------------------|
| URL | NorthAmerica | : | <a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>           |
|     | Europe       | : | <a href="http://www.hitachi-eu.com/hel/ecg">http://www.hitachi-eu.com/hel/ecg</a>           |
|     | Asia         | : | <a href="http://sicapac.hitachi-asia.com">http://sicapac.hitachi-asia.com</a>               |
|     | Japan        | : | <a href="http://www.hitachi.co.jp/Sicd/indx.htm">http://www.hitachi.co.jp/Sicd/indx.htm</a> |

### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel: <65>-538-6533/538-8577  
Fax: <65>-538-6933/538-3877  
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel: <886>-(2)-2718-3666  
Fax: <886>-(2)-2718-8180  
Telex: 23222 HAS-TP  
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel: <852>-(2)-735-9218  
Fax: <852>-(2)-730-0281  
URL: <http://www.hitachi.com.hk>

Copyright © Hitachi, Ltd., 2000. All rights reserved. Printed in Japan.  
Colophon 2.0